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LIFETIME ESTIMATION IN NBT-STRESSED P-CHANNEL POWER VDMOSFETS*

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Abstract. *This paper presents a method for lifetime estimation in negative bias temperature stressed p-channel power vertical double-diffused MOS field-effect transistors (VDMOSFETs). The usage of voltage and temperature models for extrapolation to normal operation voltage and temperature, respectively, is demonstrated. A double extrapolation, along both voltage and temperature axes, which lead to lifetime estimates for any reasonable combination of operation voltage and temperature, has been proposed as well. The proposed method can be applied in estimating the lifetime of any other MOSFETs.*

Key words: *lifetime estimation, NBTI, VDMOSFET*

1. INTRODUCTION

As the dimensions of modern MOS devices have been scaled down, a negative bias temperature instability (NBTI), which is recognised mostly in p-channel MOSFETs operated at elevated temperatures (100-250°C) under negative gate oxide fields in the range 2-6 MV/cm [1-7], has become a serious reliability problem. More drastic reduction of gate oxide thickness than that of operating voltage, has resulted into gradual increase of the effective electric field in the oxide [8], thus enhancing the NBTI (see Fig. 1). Regarding the effects on device parameters, NBT stress-induced threshold voltage shifts are most

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critical and can put a serious limit to a lifetime of p-channel devices with gate oxide thinner than 3.5 nm [4]. Microscopic mechanisms of NBTI are still not well understood, and technology optimization to minimize NBTI is a difficult problem. Therefore, accurate lifetime models are needed to make good prediction of device reliable operation [9-12].

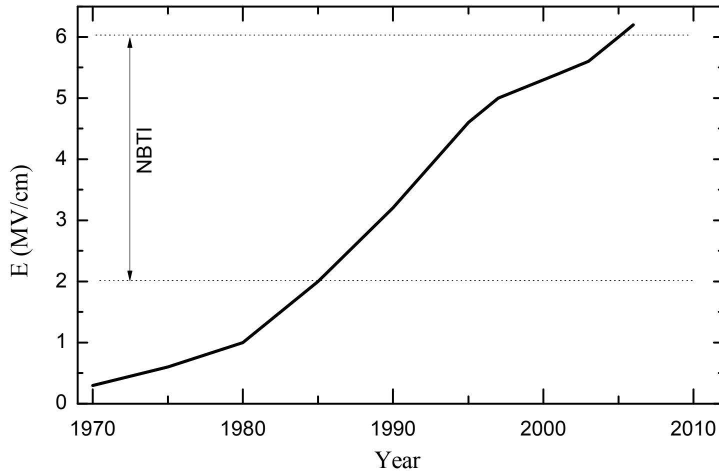

Fig. 1. Evolution of the gate oxide field in CMOS technologies [8]

In spite of device dimensions being generally scaled down, there is still high interest in ultra-thick oxides owing to widespread use of MOS technology for the realisation of power devices [13]. Degradation of power MOSFETs under various stresses (irradiation, high field, temperature, and even hot carrier) has been a subject of extensive research, but very few authors addressed the NBTI in these devices [5-7,11,12,14]. The electric fields and temperatures applied in NBT stressing can be approached to those achieved during the routine operation of power MOSFETs in automotive and industrial applications [6]. Thus, the investigations of NBTI in power MOSFETs are of high importance as well. In this paper, we will analyse the NBT stress-induced threshold voltage shifts in commercial p-channel power VDMOSFETs and apply different models to estimate the device lifetime.

2. EXPERIMENTAL RESULTS

Devices investigated in this study were commercial p-channel power VDMOSFETs IRF9520 built in standard silicon-gate technology with approximately 100 nm thick gate oxide, which were encapsulated in TO-220 plastic packages [15]. They had the initial threshold voltage V_{T0} = - 3.6 V and drain current and voltage ratings of 6.8 A and 100 V, respectively. For the static NBT stress, several sets of devices have been stressed up to 48 hours by applying negative dc voltages in the range 35-45 V to the gate, while drain and source terminals were grounded [7]. For the pulsed bias stress, negative gate voltage pulses (typically 10 kHz, 50 % duty cycle) of the same magnitudes were used. Stressing

under both static and pulsed bias conditions was performed at temperatures ranging from 125 to 175°C.

Experimental setup for NBT stressing and electrical characterization of stressed devices (measurements of transfer *I-V* characteristics) is illustrated in Fig 2. As the accelerated stressing of the above power devices required voltage amplitudes even exceeding 40 V, which were beyond the capabilities of commonly used signal source units [16-18], the inclusion of an external amplifier (booster) between the source unit and the device under test (DUT) was necessary to supply the required stress voltage to DUT. Switches S1 and S2 were used to separate high-voltage stress circuit from the low-voltage measurement circuit (source and drain of DUT were tied to ground during the stress). Gate stress voltage was obtained from the source unit acting either as a dc source or a pulse generator (Tektronix AFG3102), for static and pulsed NBT stress conditions, respectively. Swept gate measurement voltage was provided from the Agilent 6645A source unit, while an Agilent 4156C semiconductor parameter analyzer was used as the source-measure unit for drain biasing and drain current measurements. All the instrumentation, along with the temperature inside the chamber (Heraeus HEP2) and relay switches S1 and S2, have been computer controlled over the IEEE-488 GPIB bus [19].

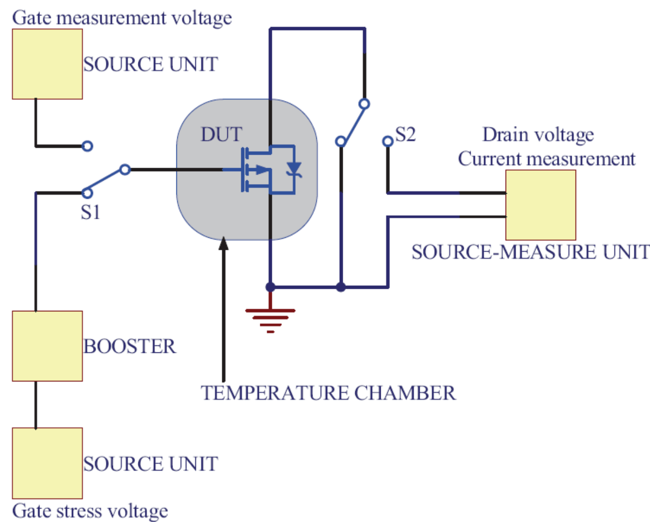

Fig. 2. Block diagram for negative bias temperature stress and measurement of p-channel VDMOS transistors [19]

As an illustration, typical transfer *I-V* characteristics of p-channel power VDMOSFETs measured during the pulsed NBT stressing with V_G = - 45 V at 175°C (f=10 kHz, DTC=50%) are shown in Fig. 3. It can be seen that, as the stressing progressed, the characteristics were being shifted along the V_{GS} axis towards the higher voltage values, while the slope of the characteristics slightly decreased. Since stressing causes degradation which is mostly irreversible, it is important to emphasize that a particular device can be stressed only under specified single stressing condition (T, V_{GS}, static or pulsed stress). Therefore, each particular device from the set of those under investigation should be

stressed under different conditions in order to obtain results for all combinations of stress conditions (T, V_{GS}).

In line with the observed shift of transfer characteristics along the voltage axis, NBT stressing was found to cause significant threshold voltage shifts (ΔV_T). Dependencies of ΔV_T on NBT stress time in devices stressed at several different temperatures with different gate voltages for both static and pulsed stress conditions are shown in Fig. 4.

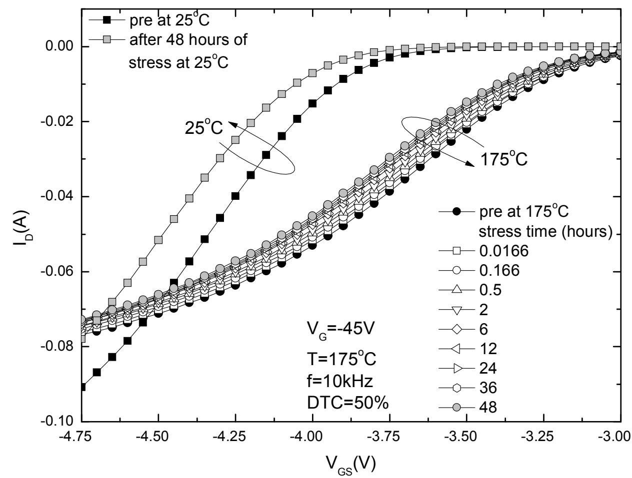

Fig. 3. I_D-V_{GS} characteristics of p-channel VDMOSFETs during the pulsed NBT stressing

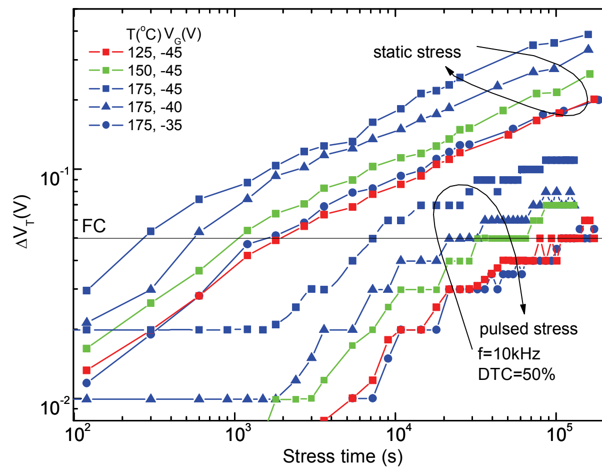

Fig. 4. Threshold voltage shifts in p-channel VDMOSFETs during the static and pulsed (f = 10 kHz, DTC=50%) NBT stressing at different voltage magnitudes and temperatures

As can be seen in Fig. 4, more pronounced shifts are obtained at higher temperatures and/or stress voltages. Also, the pulsed stressing caused generally lesser shifts as compared to static stressing performed at the same temperature with the same magnitude of dc stress voltage.

3. Algorithm for Lifetime Estimation

Our goal in this study was to estimate the lifetime of investigated VDMOSFETs under normal operating conditions (V_{GO}, T_O) using the results obtained by accelerated NBT stressing (V_{GS}, T_S). To estimate the device lifetime it is necessary to choose one of the device parameters affected by the stress, which would be suitable to monitor the level of stress-induced degradation, as well as to define an appropriate failure criterion (FC) as a maximum allowed change of the chosen parameter that is critical for device and/or circuit reliable operation. Threshold voltage has widely been accepted as a well-suited parameter, so in this study we used the experimental results for NBT stress-induced threshold voltage shift as degradation monitor to estimate device lifetime in practical operation by defining FC = ΔV_T = 50mV. The standard procedure of lifetime estimation requires first to extract the values of lifetime the devices would have if operated under the experimental conditions, and then use these experimental lifetime values for extrapolation along the gate voltage axis (voltage models [9,10]) or along the temperature axis (temperature model [11,12]). To estimate the lifetime of investigated VDMOSFETs under normal operating conditions (V_{GO}, T_O) we combined the two procedures by performing two successive extrapolations along the gate voltage and temperature axes, where the latter extrapolation uses the results of the former one as the input data, as shown in Fig. 5 [11,12]. The two successive extrapolations yield a single lifetime projection, τ_o, which can be associated with devices operated under normal conditions (both voltage, V_{GO}, and temperature, T_O). As can be seen in Fig. 5, the above double extrapolation approach can be applied to estimate the lifetime for any reasonable combination of operating voltages and temperatures (V_{GO}, T_O), which means the procedure can be re-done for each combination falling within the entire range of operating voltages and temperatures. The set of results obtained in this way can be used to construct the 3D surface representing the lifetime values corresponding to a full range of device operating conditions, and the overall procedure is illustrated by the flow chart shown in Fig 6. The approach has been applied to our experimental results, and Fig. 7 shows the surfaces representing lifetime projections to a full range of operation in the case of static and pulsed NBT stressed p-channel power VDMOS devices IRF9520, where the threshold voltage shift of 50 mV has been taken as the failure criterion. Similar surfaces can be created for different failure criteria, and can be of help in estimating either the lifetime or maximum allowed voltage and temperature for every single device in the operation environment. Randomly chosen values for operation temperature (118.7^{o}C) and voltage (-25.41 V) are shown in Fig. 7, and their intersections are shown in Fig. 8, where the two lifetime curves (for 10 and 50 years) are also presented as markers. Intersections shown in Fig. 8 can be obtained by data analysis using various graphical software versions. As can be seen in Fig. 8, by using two cursors it is possible to determine the required parameter (lifetime; temperature; voltage) under specified conditions (temperature and voltage; lifetime and voltage; lifetime and temperature), which can be very important in terms of practical applications of these devices. In this

way we can make a simple test whether the investigated devices meet the requirements of circuits where they are to be used in. For example, the lifetime of VDMOS devices considered in this study under random conditions (V_G =-25.41 V, T = 118.7°C) was estimated to be 12.76 years.

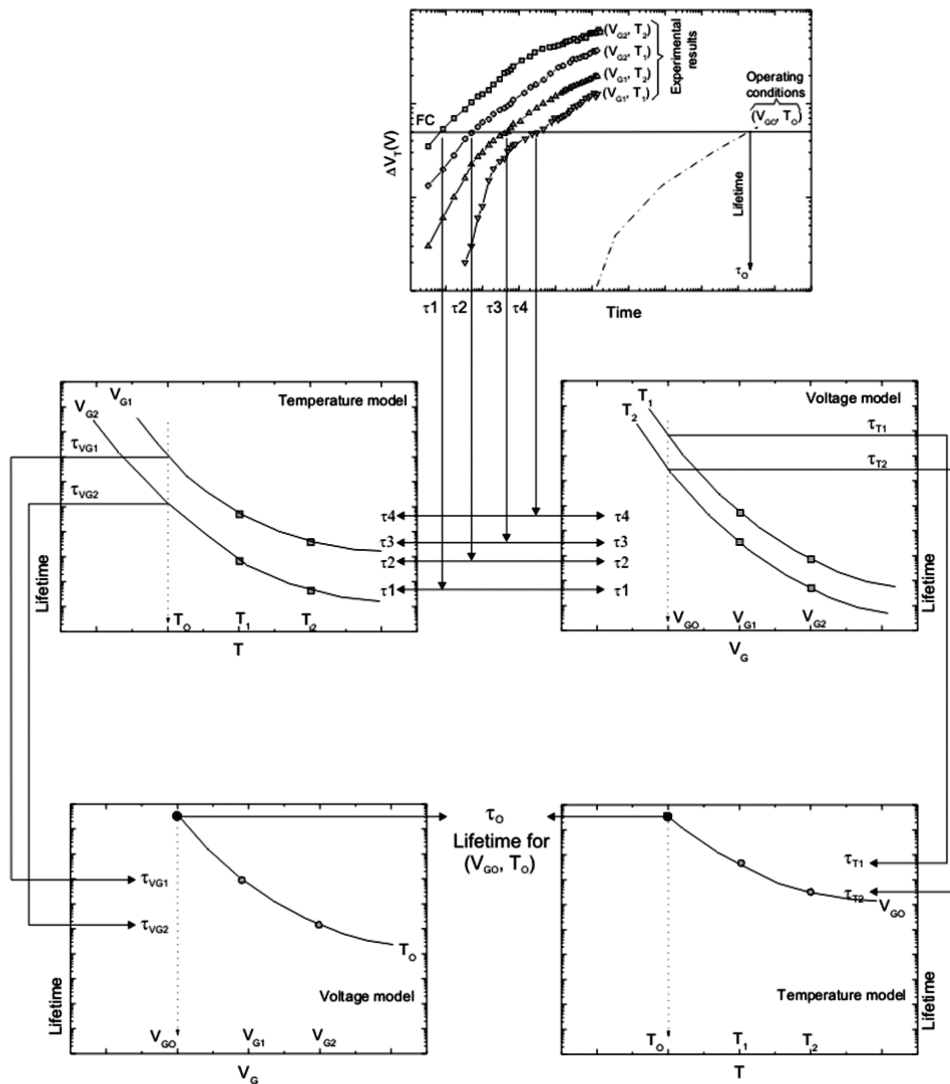

Fig. 5. Graphical illustration of the extrapolation procedure for determination of device lifetime under normal operating conditions

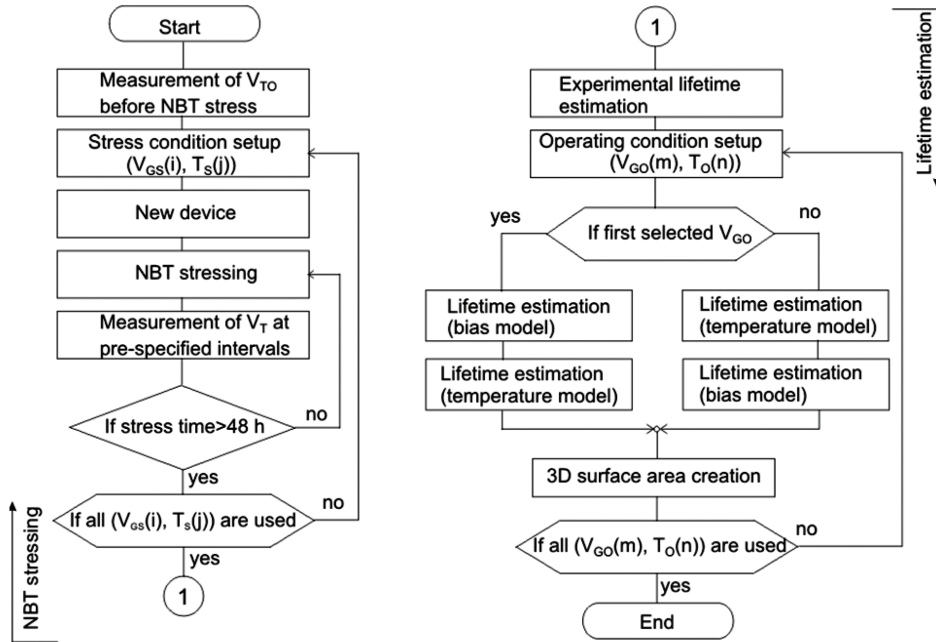

Fig. 6. Flow chart illustrating the procedure of NBTI experiment conduction and determination of the data for creation of 3D surface area that represents the lifetime values corresponding to a full range of device operating conditions

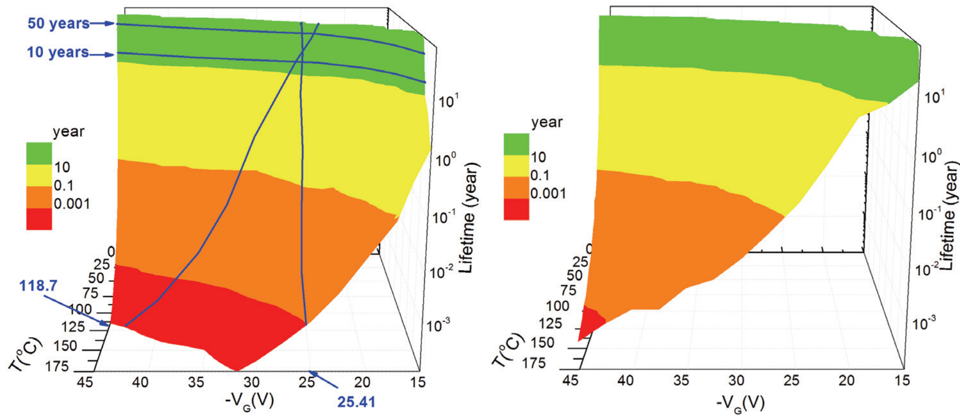

Fig. 7. Surface representing the lifetime estimates in NBT stressed devices (static left and pulsed right) for a full range of operating voltages and temperatures with $\Delta V_T = 50$ mV taken as a failure criterion

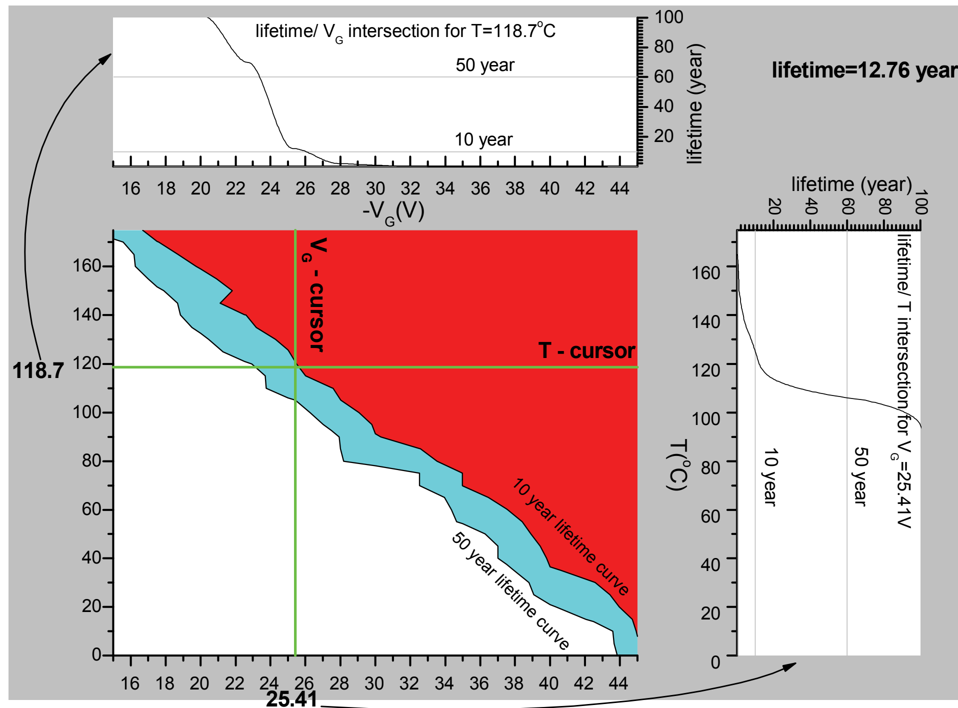

Fig. 8. 3D dependence of lifetime, operation temperature and operation voltage for static NBT stressed p-channel power VDMOSFETs IRF9520

4. Conclusions

The NBT stress-induced threshold voltage instabilities in commercial p-channel power VDMOSFETs, as well as the implications of related degradation on device lifetime have been investigated. The use of voltage and temperature models for extrapolation to normal operation voltage and temperature, respectively, were demonstrated. A new approach in estimating the device lifetime, which assumes double extrapolation along both voltage and temperature axes, was proposed. The proposed approach was shown to yield the device lifetime for any reasonable combination of operating voltages and temperatures, including those falling within the ranges normally found in usual device applications.

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ODREĐIVANJE VREMENA POUZDANOG RADA P-KANALNIH VDMOS TRANZISTORA SNAGE IZLOŽENIH NBT NAPREZANJU

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U ovom radu je predstavljen metod za određivanje perioda pouzdanog rada naponsko temperaturno naprezanih p-kanalnih VDMOS tranzistora snage. Prikazani su naponski i temperaturni model za ekstrapolaciju na radne napone i temperature, redom. Takođe, prikazana je i dvostruka sukcesivna ekstrapolacija, duž naponske i temperaturne ose, koja omogućava određivanje perioda pouzdanog rada za željene vrednosti radnog napona i temperature. Ovaj metod može biti primenjen za određivanje perioda pouzdanog rada bilo kog MOS tranzistora.

Ključne reči: *određivanje vremena pouzdanog rada, NBTI, VDMOSFET*