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MIXED MODE PERFORMANCE OF GAAS UTB-MOSFET WITH EXTRA INSULATOR REGION AND UNDOPED BURIED OXIDE REGION

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Abstract. *Investigation of mixed mode performances for GaAs UTB-MOSFET at nanoscale regime keeping in view of "Beyond CMOS" is the current trend of semiconductor industry. Here it is proposed to modify conventional models by considering an extra Insulator Region (IR) and Undoped Buried oxide Region (UBR) to study the performance related to digital and analog/RF applications. Here a GaAs is considered as the channel material. The IR-UTB-SOI-n-MOSFET has shown promising results with respect to SS, DIBL, f_T and switching speed.*

Key words: *Silicon-On-Insulator, UTB MOSFET, GaAs, DIBL, Analog/RF Performance, Insulator Region.*

1. INTRODUCTION

In recent years, there has been a growing demand of Integrated Circuits (ICs) providing better analog/ RF applications as well as digital functionalities [1]–[3]. The Silicon-On-Insulator (SOI) technology [1], [4], [5] based Fully Depleted (FD) Silicon On Insulator MOSFETs are widely used for mixed mode application ICs as it offers sharp sub-threshold slope, high current drive, high transconductance, reduced parasitic capacitance, and absence of latch-up which are key parameters for digital applications [6]–[8]. Due to high transconductance to drain current (g_m/I_d) ratio and low body factor, the FD-SOI-MOSFETs have been used to design low power circuits to operate at a high and low frequency as

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well as high temperature providing better performance than the conventional MOSFETs [9], [10].

The use of high electron mobility material like GaAs is promising as it has higher saturated electron velocity, higher electron mobility, allowing it to function at much higher frequencies, less noise and be operated at higher power levels than Silicon [11], [12].

Previously it has been shown by Orouji *et al.* [13] that SOI-MOSFETs with an extra Insulator Region (IR-SOI) in which the silicon active layer and drain region consists of an insulator region (HfO_2) provides high electron reliability due to low gate leakage current and low critical electric field. The Self Heating Effect (SHE) which is one of the drawbacks of FD-SOI has been reduced by a new structure Undoped Buried Region MOSFET (UBR-MOSFET) [14].

In this paper, the analog/ RF performance along with some scaling parameters of Ultra Thin Body (UTB) SOI n-channel MOSFET (UTB-SOI-n-MOSFET) has been examined along with UTB-SOI-MOSFET with extra Insulator Region (IR-UTB-SOI-n-MOSFET), UTB-n-MOSFET with Undoped Buried Region under channel (UBR-UTB-SOI-n-MOSFET) and a new structure UTB-SOI-n-MOSFET with extra insulator region and undoped buried region under channel (IR-UBR-UTB-SOI-n-MOSFET) with the help of the device simulator from SILVACO TCAD[15].

2. Device Structure and Simulation Setup

The schematic representation of four different structures UTB-SOI-n-MOSFET, IR-UTB-SOI-n-MOSFET, UBR-UTB-SOI-n-MOSFET and IR-UBR-UTB-SOI-n-MOSFET, which was considered for the 2-D simulation is given in Fig.1. The Effective Oxide Thickness (*EOT*), the gate length (L_G), the GaAs body thickness (t_{GaAs}), the SiO_2 Buried Oxide Thickness (t_{BOX}) and Si Substrate thickness (t_{SUB}) have been taken of 1.1 nm, 60 nm, 10 nm, 50 nm and 100 nm respectively in all the four type of structures. The source extension (L_S) and the drain extension (L_S) have been taken as 70 nm each. The source and drain area are highly doped with n-type donor ions with concentration 10^{20} /cm^3 each to reduce the mobility degradation due to coulombs scattering. The silicon substrate is diffused with p-type acceptor ions with concentration 10^{18} /cm^3 and the GaAs channel region is doped with p-type acceptor ions with concentration 10^{16} /cm^3 to avoid threshold voltage variation[16]. The metal gate work function is set to 4.6 eV during simulation[17].

The structures are calibrated to meet the requirement of International Technology Roadmap for Semiconductors (ITRS) in 45 nm technology node [18]. The 2-D numerical device simulator [15] ATLAS is used for the simulation of the proposed structures. The drain bias is fixed to V_{DD} =1.0 V as per ITRS [19]. To study the Analog/ RF performance the simulation is carried out at the drain to source voltage V_{DS} = 0.5 V (half of the supply voltage i.e. $V_{DD}/2$) [20] with a variable gate to source voltage (V_{GS}) 0 V to 1.0 V. The threshold voltage is obtained by using constant current I_D =10^{-6} A/μm, from I_D~V_{GS} characteristic curve. In the channel region the electron and hole Shockley-Read-Hall [21],[22] generation and recombination lifetime, τ_n and τ_p are set to the value 1×10^{-8} sec each. In material models, Lombardi mobility model [23] is used which considers the effect of transverse electric fields along with doping and temperature dependent parameters

of mobility [24]. The numerical solution used here is based on the drift-diffusion approach [25]. Some other material models have also been used here like the concentration dependent (CONMOB), parallel electric field dependence (FLDMOB) which is required for measuring velocity saturation effect, Shockley-Read-Hall (SRH) and optical [15]. The Fermi-Dirac model helps to get the result close to ideal values by a Rational Chebyshev approximation [19].

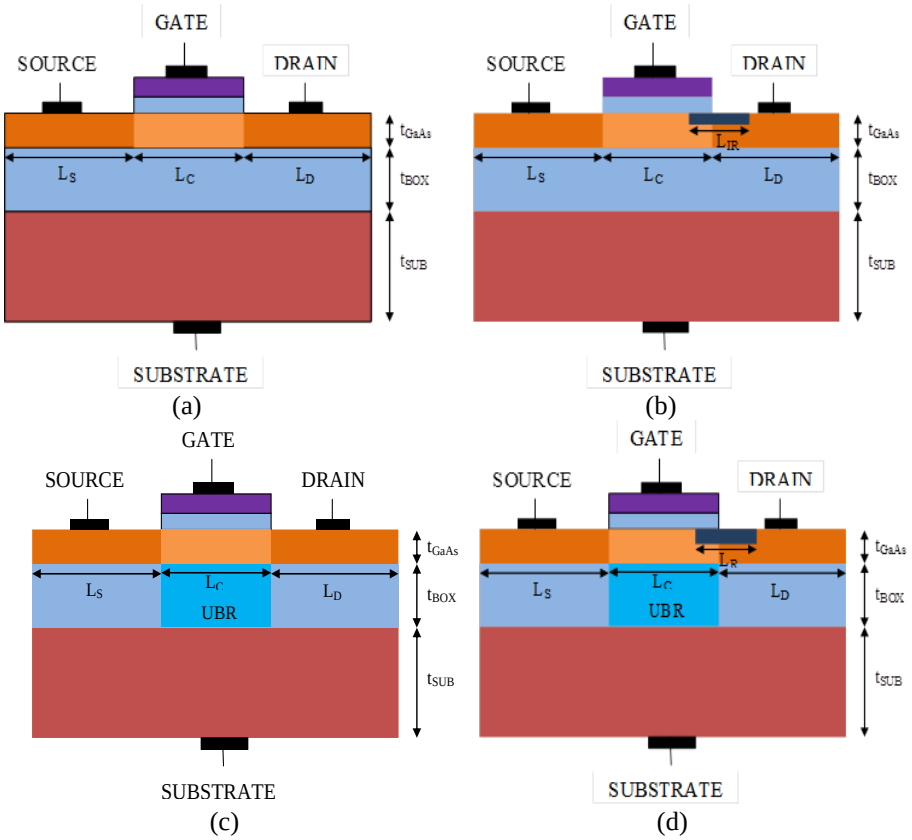


Fig. 1 Schematic Device structures (a) UTB-SOI-n-MOSFET (b) IR-UTB-SOI-n-MOSFET (c) UBR-UTB-SOI-n-MOSFET (d) IR-UBR-SOI-n-MOSFET

Table 1 Structure notation

Notation used in this article	Structure
A	UTB-SOI-n-MOSFET
B	IR-UTB-SOI-n-MOSFET
C	UBR-UTB-SOI-n-MOSFET
D	IR-UBR-UTB-SOI-n-MOSFET

3. RESULT ANALYSIS

As described previously these four types of structures were simulated using 2-D numerical device simulator and the parameters like the on-state drive current (I_{ON}), off-state leakage current (I_{OFF}), I_{ON}/I_{OFF} ratio, threshold voltage (V_{th}) and power dissipation variation were evaluated which are some of the factors affecting the scaling properties of the devices. The surface potential variation with respect to channel length was also observed. The RF/ Analog performance analysis was done by measuring the parameters like transconductance (g_m), total capacitance (C_{Total}), Q-factor and cut-off frequencies (f_T) for the four different structures. A Sub-threshold Slope (*SS*) was calculated by using the following equation [19].

$$SS(mV/dec) = \frac{\partial V_{GS}}{\partial(\log I_D)} \tag{1}$$

Another vital parameter responsible for scaling effect is the Drain Induced Barrier Lowering (*DIBL*) which was also evaluated by the following equation[26].

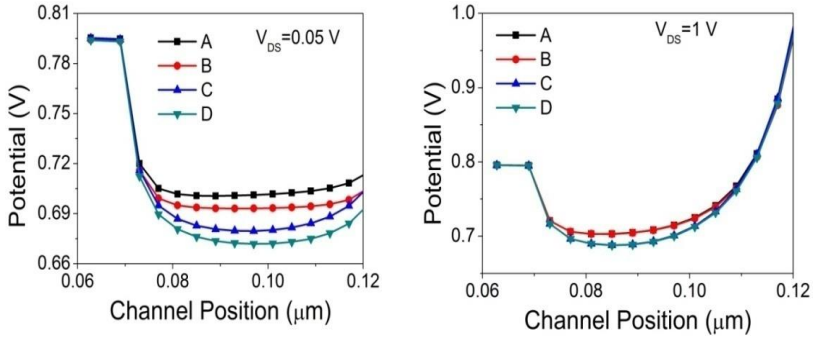


Fig. 2 Surface Potential Variation along channel for A, B, C and D at V_{GS} = 1 V (a) at V_{DS} = 0.05 V (b) at V_{DS} = 1 V

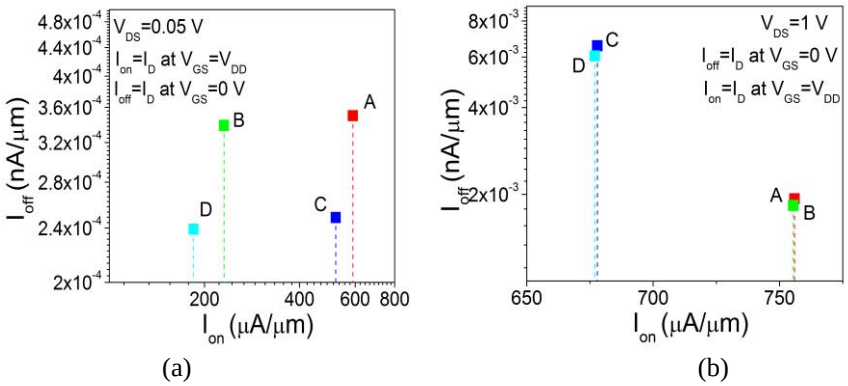


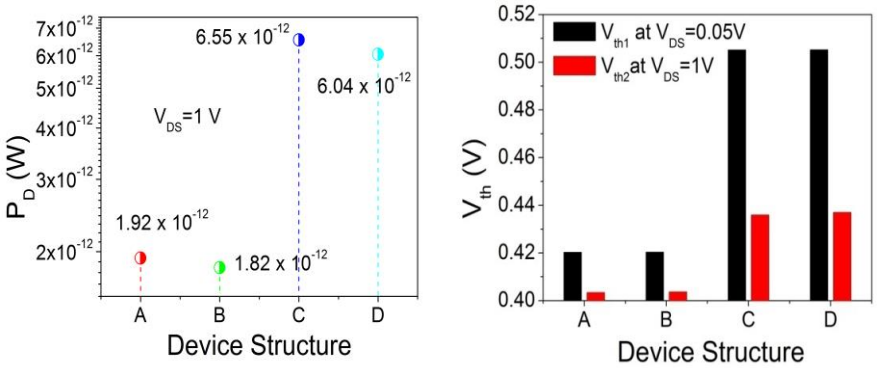
Fig. 3 I_{ON} and I_{OFF} comparison for A, B, C and D (a) at V_{DS} = 0.05 V (b) at V_{DS} = 1 V

$$DIBL = \frac{V_{th1} - V_{th2}}{0.95} \tag{2}$$

Where V_{th1} and V_{th2} are threshold voltages at V_{DS} = 0.05 V and V_{DS} = 1 V.

Fig.2 shows the surface potential variation along the channel of the structures A, B, C and D, where Fig. 2 (a) shows the variation of surface potential along the channel for the four structures at drain to source voltage V_{DS} = 0.05 V and Fig. 2 (b) shows the surface potential variation along the channel for the four structures when V_{DS} = 1 V.

The trade-off between I_{OFF} and I_{ON} has been shown in the Fig. 3 for different structures. Fig. 3(a) shows the I_{ON} and I_{OFF} comparison between A, B, C and D at V_{DS} = 0.05 V and Fig. 3(b) shows the I_{ON} and I_{OFF} comparison between A, B, C and D at V_{DS} = 1 V. At V_{DS} = 0.05 V structure C gives better I_{ON}/I_{OFF} ratio and at V_{DS} = 1 V, structure B shows significant improvement in I_{ON}/I_{OFF} ratio.



(a) (b)

Fig. 4 (a) Static Power Dissipation for A, B, C, and D,
(b) Threshold Voltage Variation at V_{DS} = 0.05 V and V_{DS} =1 V

In the Fig. 4(a), the static power dissipation ($P_D = I_{OFF}$ x V_{DD}) [27] variation with respect to the four type of structures is presented. The structure B provides lower static power dissipation than the other three structures. The Fig. 4(b) provides the threshold voltage variation of the four structures at V_{DS} = 0.05 and V_{DS} = 1 V. The extracted value of threshold voltage, sub-threshold slope, DIBL and static power dissipation are tabulated for all device structures in table 2.

In Fig. 5, the trans-conductance i.e.

$$g_m = \frac{\partial I_D}{\partial V_{GS}} \tag{3}$$

for different A, B, C and D has been given. The Fig. 5(a) and Fig. 5(b) show the g_m variation with I_D for the given four structures at V_{DS} = 0.05 V and V_{DS} = 1 V respectively.

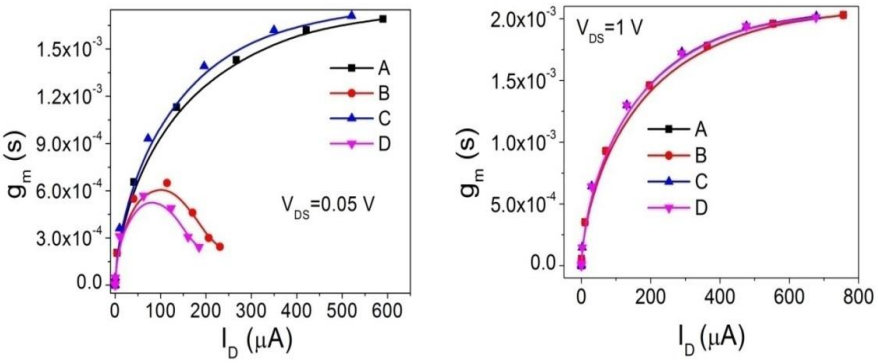


Fig. 5 Trans-conductance (g_m) variation with I_D for A, B, C and D (a) at V_{DS} = 0.05 V (b) at V_{DS} =1 V

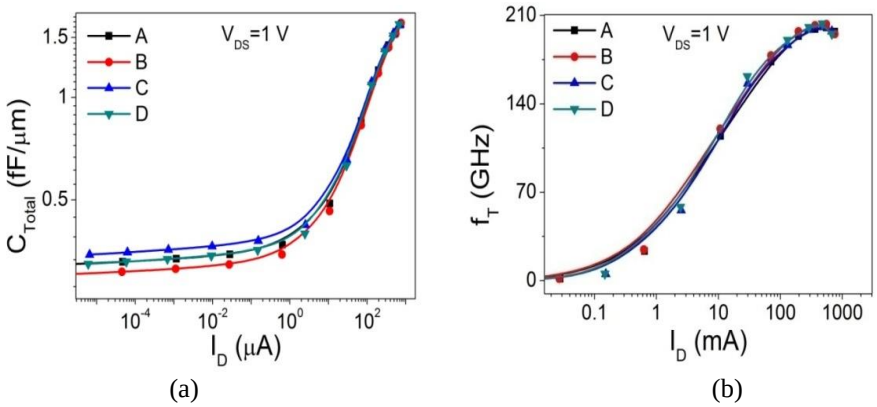


Fig. 6 (a) Total Capacitance (C_{Total}) with I_D for A, B, C and D at V_{DS} =1 V (b) a Cut-off Frequency (f_T) variation with I_D for A, B, C and D at V_{DS} =1 V

In Fig. 6(a), the variation of total capacitance (C_{Total} = C_{gd} + C_{gs}) for A, B, C and D has been given at V_{DS} = 1 V where C_{gd} is parasitic gate to drain capacitance and C_{gs} is the parasitic gate to source capacitance.

Another important parameter, a cutoff frequency (f_T) has been plotted in Fig. 6(b)

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})} \tag{4}$$

The *Q*-Factor (g_m/SS) has been calculated for the four device structures and given in the Table 3.

Table 2 Performance parameters-1

Structure	V_{th1} (V)	V_{th2} (V)	SS1 (mV/dec)	SS2 (mV/dec)	DIBL (mV/V)	P_D (x10^{-12} W)
A	0.420	0.403	69.81	71.95	17.678	1.92
B	0.420	0.404	69.68	71.83	17.589	1.82
C	0.505	0.436	74.11	82.21	72.923	6.55
D	0.505	0.437	74.01	81.90	71.872	6.04

Table 3 Performance parameters-2

Structure	I_{ON1}/I_{OFF1} (x10^{-9})	I_{ON2}/I_{OFF2} (x10^{-8})	C_{Total} (fF/μm)	f_T (x10^{-11} Hz)	Q-Factor
A	1.686	3.920	1.639	2.00	24.21
B	0.681	4.132	1.655	2.03	9.32
C	2.095	1.034	1.629	2.00	23.07
D	0.773	1.120	1.639	2.03	7.68

4. CONCLUSIONS

A comparative performance analysis of a new structure was presented namely a IR-UBR-UTB-SOI-n-MOSFET which contains an extra Insulator Region (IR) at the channel source junction, Undoped Buried Region and having a GaAs under the channel region. The scaling and RF parameters of IR-UBR-UTB-SOI-n-MOSFET have been obtained along with conventional UTB-SOI-n-MOSFET. From the analysis, it has been obtained that the Sub-threshold slope, DIBL, and the static power dissipation are lower for IR-UTB-SOI-n-MOSFET than the other three structures and it also provides better I_{ON}/I_{OFF} ratio. So the above structural change in the device can be a good candidate for switching and low standby operating power application.

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