

## NBT STRESS AND RADIATION RELATED DEGRADATION AND UNDERLYING MECHANISMS IN POWER VDMOSFETS

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**Abstract.** *In this paper we provide an overview of instabilities observed in commercial power VDMOSFETs subjected to irradiation, NBT stress, and to consecutive exposure to them. The results have indicated that irradiation of previously NBT stressed devices leads to additional threshold voltage shift, while NBT stress effects in previously irradiated devices depend on the gate bias applied during irradiation and on the total dose received. This points to the importance of the order of applied stresses, indicating that for proper insight into the prediction of device behaviour not only harsh conditions, but also the order of exposure have to be considered. It has also been shown that changes in the densities of oxide trapped charge and interface traps during spontaneous recovery after each of applied stresses can be significant, thus leading to additional instability, even though the threshold voltage seems to remain stable, pointing to the need for clarifying the responsible mechanisms.*

**Key words:** *Negative bias temperature instability (NBTI), irradiation effects, responsible mechanisms, oxide trapped charge, interface traps, spontaneous recovery*

### 1. INTRODUCTION

Development of advanced electronic industry is based on combining two concepts: More Moore (miniaturization) and More than Moore (diversification), i.e. on combining of System-on-Chip and System-in-Package concepts, thus leading to higher value systems. Second concept includes integration of different devices, such as passives, analog/RF, power devices, sensors and actuators and biochips. Among these, power vertical double-diffused metal oxide semiconductor (VDMOS) transistors exhibit a

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number of advantages, such as high switching speed, high current driving capabilities, high breakdown voltage, high input impedance and high thermal stability, which make these devices attractive for various application in power control in industrial electronics (automation, robotics), auto industry (automotive electronics), nuclear power plants, communication satellites, military and civil airplane industry, and military equipment (tanks, ships, submarines). In many of these applications devices may be subjected to stress or harsh environment conditions. Accordingly, investigation of their reliability and related effects is of high importance [1-11].

Because of its superior switching characteristics which enable operation at high frequencies, the power VDMOSFET is attractive as a switching device especially in communication satellites that require many extremely small, lightweight power supplies for supplying various components, circuits and systems. Namely, high-frequency operation of power supplies enables reduction of their weight and volume through the use of smaller passive components (transformers, choke-coils, and capacitors), so the power VDMOSFETs are suited for these applications. However, during a communication satellite operation of several years, assembled devices can accumulate the total dose up to 100 Gy ( $\text{SiO}_2$ ), while in high orbits this dose can be even 10 kGy ( $\text{SiO}_2$ ) [12]. Therefore, the most important requirement for power VDMOSFETs assembled in electronic systems for application in radiation environment is high radiation tolerance. The ionizing irradiation may cause degradation of power VDMOSFETs electrical parameters, such as threshold voltage shift, reduction of transconductance, increase of leakage currents and reduction of breakdown voltage [13, 14]. Threshold voltage shift ( $\Delta V_T$ ) is the most serious problem in these devices since it may cause change of operation mode from enhancement to depletion in n-channel devices or dramatic reduction of current driving capability in p-channel ones. Threshold voltage shift is known to increase with total dose received and in many investigations it is shown that the main irradiation effects on electrical parameters are caused by the creation of positive gate oxide charge ( $N_{ot}$ ) and interface traps ( $N_{it}$ ) [15].

Besides operation in the irradiation environment, in a number of application devices are routinely operated at high voltage and current levels, which lead to both self heating and increased gate oxide fields [16]. Negative bias temperature instability (NBTI) is a phenomenon that is commonly observed in p-channel devices operated in the temperature range 100-250 °C at negative gate voltages producing gate oxide electric fields 2-6 MV/cm [17-20]. Note that electric fields and temperatures that cause NBTI are typically found during the device burn-in tests [21, 22]. NBT stress may lead to degradation of important electrical parameters of power VDMOSFETs. Among these the negative  $\Delta V_T$  caused by increase of  $N_{ot}$  and  $N_{it}$  is the most serious reliability problem [23]. Note that more significant negative  $\Delta V_T$  is obtained at higher temperatures and/or higher gate voltages, i.e. higher oxide electric fields [24-28].

Although NBTI phenomenon is known for more than a half of the century, the reliability issues associated with NBTI have resurfaced in the past two decades due to convergence of several factors resulting from the device scaling. This is the reason that vast majority of recent extensive investigation of NBTI has been focused on the related phenomena in ultrathin gate dielectrics layers, and only few research groups seem to have addressed the NBTI in thick gate oxides [24, 29, 30]. However, in spite of device dimensions being generally scaled down, there is still high interest in ultra-thick oxides

owing to widespread use of MOS technology for the realization of power devices, so the investigation of NBTI in VDMOSFETs is of high interest.

It should be emphasised that PMOS transistors can be subjected to a single stress, but also in numerous applications to simultaneous or consecutive NBT and irradiation stresses. Namely, if p-channel power devices which exposed to radiation operate at higher temperature or at maximum power, the mechanisms responsible for both radiation effects and NBT instability can be activated. For example, satellite electronic equipment can be exposed to cosmic irradiation during a long time without air convection cooling. So, the active p-channel MOS devices can be irradiated and in the same time exposed to NBT stress, while the back-up devices (which do not operate) are only irradiated.

It is known that irradiation effects and NBT instabilities in power MOS devices have been extensively studied, but they have been investigated separately. Though, the results of elevated temperature effects on the radiation response have been reported in some studies performed in order to estimate the MOS device behaviour in real irradiation environment [31, 32], but the p-channel devices used in those studies were irradiated and/or annealed under the positive gate bias. Regarding the fact that devices which operate in real applications can be stressed and recovered under different conditions and that final effects depend on specific applications and device mission, in this paper we present the results of consecutively NBT stressed and irradiated p-channel power VDMOS transistors. In this way the effects of specific kind of stress in devices previously subjected to the other kind of stress are investigated.

However, for proper understanding of the effects induced by applied stresses, it is important to analyze in detail not only the changes in the electrical parameters, but also the mechanisms responsible for the observed effects. Clarification of behaviour and nature of oxide and interface defects created during and after the stress is very important in order to improve device stability and resistivity to applied stress. That is why this paper is aimed at analysis of reliability problems in power VDMOS transistors caused by NBT stress and radiation, as well as at related degradation and underlying mechanisms. The most vulnerable parts of the VDMOS transistors subjected to extreme, harsh environmental conditions or to the stress are the parts based on dielectrics ( $\text{SiO}_2$  and  $\text{SiO}_2$ -Si interface), as both NBT stress and irradiation of VDMOS transistors lead to creation of oxide and interface defects causing significant degradation of electrical parameters. It is of great interest to know the nature of the defects, and these are still in the focus of many investigations aimed at clarifying responsible mechanisms and improving possibilities of predicting device behaviour in specific application.

## 2. RADIATION EFFECTS

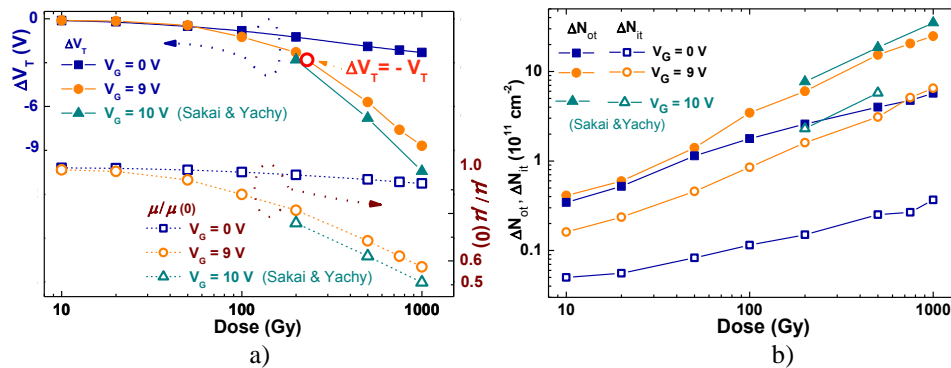
As already mentioned, the threshold voltage shift is, undoubtedly, the most serious problem for irradiated devices since it may cause change of operation mode from enhancement to depletion in n-channel devices (thus leading to faulty operation of switching power supplies), or dramatic reduction of current driving capability in p-channel ones. Even the radiation-hardened devices may fail due to reduction in current-drive capability owing to channel carrier mobility degradation and/or positive  $\Delta V_T$  [33].

The irradiation effects in MOSFETs have been extensively investigated by many researchers in the last decades. In our early study we have examined radiation response of

commercially available n-channel power VDMOSFETs EFL1N10 manufactured by "Ei-Microelectronics", Niš, Serbia, which were realized in a standard Si-gate technology with the hexagonal cell geometry and gate oxide thickness of 100 nm. Gamma radiation was performed in Co-60 source (dose rate 0.04 Gy/s) at room temperature for two groups of the devices (without and with gate bias applied  $V_G = +9$  V). Drains and sources of all devices were grounded during irradiation.

The changes of the threshold voltage and mobility ( $\mu$ ) during the irradiation of the devices [2] are presented in Fig. 1(a), where are also comparatively presented the results for similar devices [34]. Observed significant threshold voltage shift and mobility reduction in the devices were much more pronounced in the case of positive gate bias applied. It should be noted that the similar behaviour of these electrical parameters of the power VDMOS transistors has also been observed by other investigators and it has been generally established as a typical behaviour [14, 15, 33].

The radiation tolerance of the power VDMOS transistors, as a very important requirement, can be determined for the maximum operating positive bias applied as this is the worst case scenario. As can be seen in Fig. 1(a), the threshold voltage shift becomes equal to threshold voltage ( $\Delta V_T = -V_T$ ) at the total dose of about 250 Gy (denoted point at which investigated devices change their operating mode from enhancement to depletion). Therefore, the radiation tolerance of used commercial devices is of about 250 Gy, which is half the value required for their application in communication satellites with life spans of ten years [2].



**Fig. 1** Gamma-irradiation induced (a)  $\Delta V_T$  and  $\mu/\mu_0$ ;  
(b)  $\Delta N_{ot}$  and  $\Delta N_{it}$  in n-channel power VDMOSFETs (EFL1N10).

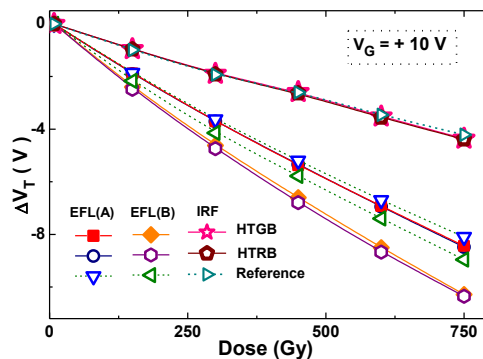
Considering that the main radiation effects on electrical parameters are caused by the creation of both  $N_{ot}$  and  $N_{it}$ , the changes in their densities ( $\Delta N_{ot}$  and  $\Delta N_{it}$ ) are very often analysed and discussed in the literature [8, 15, 33, 35-37]. In Fig. 1(b)  $\Delta N_{ot}$  and  $\Delta N_{it}$  in the devices which were irradiated in our experiment are presented.

It should be emphasized that reliability screening is important in achieving high reliability of VDMOSFETs for application in radiation environment. Screening is normally performed on all devices in order to reduce the possibility of infant mortality. The standard reliability screening for these devices includes „burn-in tests“ (US MIL-STD 883, Test Method 1015), such as: high temperature reverse bias (HTRB), high

temperature gate bias (HTGB) and high temperature storage life (HTSL) stresses [38]. However, it was shown that HTGB stress affects the radiation response in MOS transistors. This was the reason for modification of the standard qualification testing for application of MOSFETs in radiation environment and for imposing the requirement for radiation qualification testing after burn-in (US MIL-STD 883, Test Method 1019). Our results [22, 39, 40] which have shown that burn-in tests could have a significant impact not only on the radiation response of VDMOSFETs, but also on annealing of radiation defects, have confirmed the need for modification of qualification testing.

In the another experiment also commercially available IRF510 (with nominal gate oxide thickness of 100 nm, realized in a standard Si-gate technology) and EFL1N10 devices (from different batches A and B) were irradiated by Co-60 source (dose rate 0.13 Gy/s) at room temperature with gate bias applied  $V_G = +10$  V.

The changes of the threshold voltage and mobility during the irradiation of EFL1N10 (batch A and B) and IRF510 devices [22] are presented in Fig. 2, and Fig. 3, respectively, while underlying changes of  $\Delta N_{ot}$  and  $\Delta N_{it}$  are presented in Fig. 4. In these figures the results for reference devices and for devices subjected to HTRB ( $V_D = 80$  V,  $T = 125^\circ\text{C}$  for 168 h) and HTGB ( $V_G = 20$  V,  $T = 125^\circ\text{C}$  for 168 h) stresses are compared. It can be seen that  $\Delta V_T$  was more pronounced in EFL devices, indicating that IRF devices were better in view of radiation tolerance, while there was almost no difference in mobility reduction.

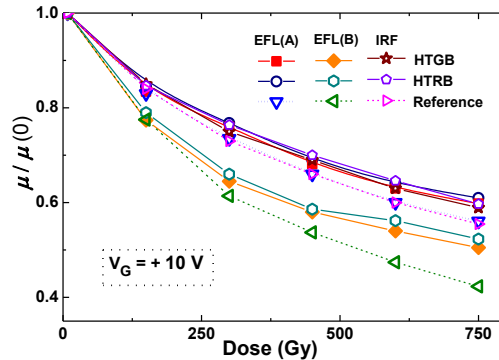


**Fig. 2** Gamma-irradiation induced  $\Delta V_T$  in EFL-batch A, EFL-batch B and IRF n-channel power VDMOSFETs in HTRB and HTGB stressed and reference devices [40].

It can be seen that there was almost no difference between the HTRB and HTGB stress effects on radiation response of investigated devices. The results which suggested that radiation response appeared to be almost independent of device pre irradiation stress biasing were obtained also for field -oxide MOSFETs [41]. As can be seen in Figs. 2 and 3,  $\Delta V_T$  during irradiation was slightly larger in HTRB stressed devices, while the mobility reduction was slightly larger in HTGB stressed ones. Similar behaviour of  $\Delta V_T$  was obtained for irradiated field-oxide MOSFETs [41].

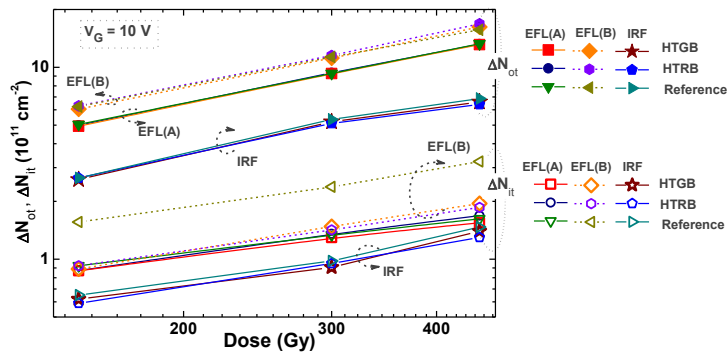
As can be seen from Fig. 4, the build-up oxide trapped charge appeared to be almost independent of device pre irradiation stress. On the other hand, the build-up of interface traps was somewhat less pronounced in the stressed device. For explanation of such behaviour of  $\Delta N_{ot}$  and  $\Delta N_{it}$  the chain of mechanisms, in which the diffusion of hydrogen

related species (originating either from package inside or gate oxide adjacent structures) from the bulk of the oxide towards the interface, has been proposed.



**Fig. 3** Gamma-irradiation induced  $\mu/\mu_0$  in EFL-batch A, EFL-batch B and IRF n-channel power VDMOSFETs in HTRB and HTGB stressed and reference devices [40].

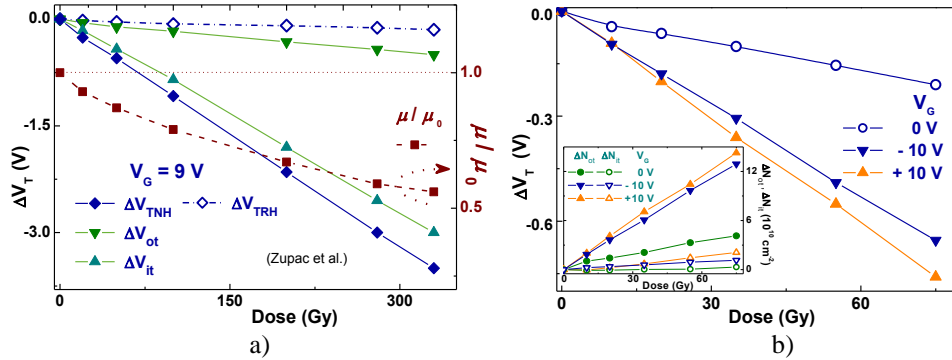
In many investigations of p-channel power MOSFETs radiation response, the role of  $\Delta N_{ot}$  and  $\Delta N_{it}$  were also emphasized. In Fig. 5(a) the radiation induced threshold voltage shift ( $\Delta V_{TNH}$ ) and degradation of the hole mobility  $\mu/\mu_0$  in non-hardened IRF9130 and threshold voltage shift in radiation hardened FRM9130 ( $\Delta V_{TRH}$ ) p-channel power MOSFETs are presented [14].



**Fig. 4** Gamma-irradiation induced  $\Delta N_{ot}$  and  $\Delta N_{it}$  in EFL-batch A, EFL-batch B and IRF n-channel power VDMOSFETs in HTRB and HTGB stressed and reference devices [40].

Also, in the Fig. 5(a) the contributions of the gate oxide charge ( $\Delta V_{ot}$ ) and interface traps ( $\Delta V_{it}$ ) to the  $\Delta V_{TNH}$  (for non-hardened devices) are presented. Devices were irradiated at room temperature by Co-60 gamma-ray source (dose rate of 0.2 Gy(Si)/min), with gates biased at  $V_G = +9$  V, while source and drain terminals were grounded. Unlike the non-hardened devices,  $\Delta V_{TRH}$  of hardened devices is small for total dose below 400 Gy and mobility degradation is less than 4%. Both gate oxide charge ( $\Delta N_{ot} = \Delta V_{ot} C_{OX}/q$ ) and

interface traps ( $\Delta N_{it} = \Delta V_{it} C_{OX}/q$ ) are positive, that gives rise to negative  $\Delta V_{TNH}$ , i. e.  $\Delta V_{TNH} = \Delta V_{ot} + \Delta V_{it}$ .



**Fig. 5** Gamma-radiation induced (a)  $\Delta V_{TNH}$  and  $\mu/\mu_0$  in non-hardened and  $\Delta V_{TRH}$  in hardened p-channel power MOSFET; (b)  $\Delta V_T$  and corresponding  $\Delta N_{ot}$  and  $\Delta N_{it}$  (in inserted figure) in commercial p-channel power VDMOSFETs.

In Fig. 5(b) the radiation induced  $\Delta V_T$  and behaviours of corresponding buildup of  $\Delta N_{ot}$  and  $\Delta N_{it}$  (in inserted figure) in commercially available IRF9520 p-channel power VDMOSFETs irradiated at different gate bias applied are presented. Although irradiation conditions and obtain results will be discussed in detail in Sect. 4, it should be mentioned that significant negative  $\Delta V_T$  induced by radiation also increases with total dose received and depends on gate bias applied.

### 3. NBT STRESS EFFECTS

NBT stress-induced threshold voltage instabilities in commercial power VDMOSFETs, as well as the implications of related degradation on device lifetime have been extensively investigated in our research in the last decade [27, 42-44]. Although in many experiments devices have been subjected to various NBT stress (static or pulsed) and annealing conditions [9, 23, 25, 45, 46, 48-52], in this section a part of results obtained during static NBT stress and annealing is presented, with attention to insight into the NBTI as a result of sequential NBT stress and bias annealing steps.

In these investigations commercial p-channel power VDMOSFETs transistors IRF9520 (with current and voltage ratings of 6.8 A and 100 V) were used. These devices were built in standard silicon-gate technology with 100 nm thick gate oxide. Devices have been stressed up to 2000 hours by applying negative voltages (30 – 45 V) to the gate, with drain and source terminals grounded, at temperatures ranging from 125 to 175 °C. Important details of used equipment for stress, annealing and measurement will be described in Sect. 4.

During NBT stresses  $\Delta V_T$  of investigated p-channel power VDMOSFETs was more significant in the cases of higher stress voltage and/or temperatures [25]. The underlying phenomenon leading to the observed  $\Delta V_T$  in the stressed devices is the stress-induced buildup of  $\Delta N_{ot}$  and  $\Delta N_{it}$ . Typical time dependencies of stress induced buildup of  $\Delta N_{ot}$  and

$\Delta N_{it}$  for different stress voltages at the temperature of 150 °C and for different stress temperatures at stress voltage of -40 V are presented in Fig. 6, while corresponding  $\Delta V_T$  are presented in inserted figures. In these figures the results for NBT stressed devices during 2000 hours are presented. Analysis has shown that  $\Delta V_T$  time dependencies follow the  $t^n$  power law, but with three different phases (that depends on the parameter  $n$ ), which is indicated by the dashed lines (in inserted figures). In the first phase, parameter  $n$  depends on bias as well as on temperature, and varies from 0.4 to 1.14. In the second phase parameter  $n$  is almost independent on bias and temperature, and equals approximately 0.25 as obtained in all earlier NBTI investigations [17, 24, 53, 54]. This phase begins earlier in devices stressed at higher voltages and/or temperatures, and might be even expected that the first phase disappears under more severe stress conditions. In the third (long stress) phase parameter  $n$  again becomes bias and temperature dependent, varying from 0.25 to 0.14.

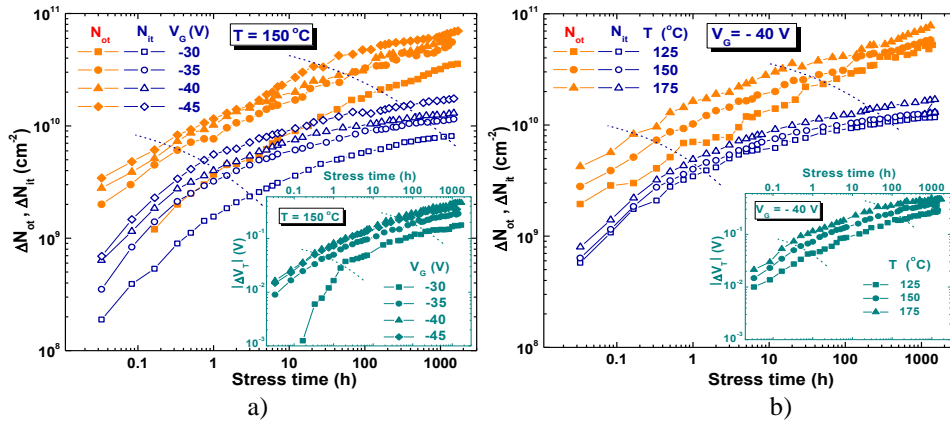
Also, in Fig. 6 could be observed that the buildup of  $\Delta N_{ot}$  is more significantly pronounced than that of  $\Delta N_{it}$  for each specific combination of temperature and stress voltage in all three stress phases. In addition, it could be seen that  $\Delta N_{it}$  rapidly increases in the early phase, but slows down in the second phase and tends to more rapidly saturate than  $\Delta N_{ot}$ . It should be emphasized that the strong correlation between time dependence of  $\Delta V_T$  and corresponding  $\Delta N_{ot}$  in all cases (all combinations of temperatures and stress voltages) was observed. On the other hand, such correlation between  $\Delta V_T$  and  $\Delta N_{it}$  time dependencies was not observed. This disagreement becomes more noticeable as the NBT stressing advances into the second phase and, especially, further into the third phase. Therefore, time dependence of  $\Delta V_T$  in investigated p-channel power VDMOSFETs seems to be mostly affected by NBT stress induced buildup of oxide trapped charge, which does not appear to be consistent with most of literature data emphasizing dominant role of stress induced interface traps [17, 24, 53].

In addition, it was shown that the effects of post-stress annealing (at various voltages and/or temperatures, during various time intervals), provided after each phase of NBT stress (1<sup>st</sup> - 3<sup>rd</sup>), depend not only on temperature and gate bias conditions, but also on status of the gate oxide and SiO<sub>2</sub>-Si interface, immediately after the stress [46]. Namely, observed effects were affected by the densities of stress-induced  $N_{ot}$  and  $N_{it}$  and their spatial and energy distributions, number of potential trapping sites and quantities of reacting species available after the stress, quantity and distribution of new defects possibly created by preceding stress, etc.

Besides that, in order to further disclose the effects of post-stress and intermittent annealing on degradation associated to NBTI, another experiment, in which devices were subjected to a five step sequence, was performed. In this experiment, commercial p-channel IRF9520, and n-channel IRF510 power VDMOSFETs were also used. IRF510 transistors were also built in standard silicon-gate technology with 100 nm thick gate oxide. The experiment included three NBT stress steps interchanging with two bias annealing steps. Namely, one week of NBT stressing with gate voltage of -40 V at  $T = 150$  °C was followed by one week of annealing without or with the gate bias applied, also at 150 °C. After that, NBT stress and annealing were repeated, followed by final NBT stress. Devices were annealed without or with gate bias applied ( $V_G = +10$  V or  $V_G = -10$  V).



It was shown that annealing with negative gate bias applied did not affect noticeably  $\Delta N_{ot}$  and  $\Delta N_{it}$ , while annealing performed under the zero and positive gate bias removed the portion of stress induced oxide charge, but created a new interface traps over to those that have been created during the preceding NBT stress. Observed effects were more pronounced in the case of positive gate bias applied. Therefore, evolutions of  $\Delta V_T$  in p- and n-channel power VDMOSFETs and corresponding evolutions of  $\Delta N_{ot}$  and  $\Delta N_{it}$  in p-channel transistors obtained during NBT stress and annealing under the positive gate bias applied are presented in Fig. 7 and Fig. 8, respectively. In these figures can be observed that majorities of the changes occurred only in an early stage of the annealing steps, as well as of NBT stresses.

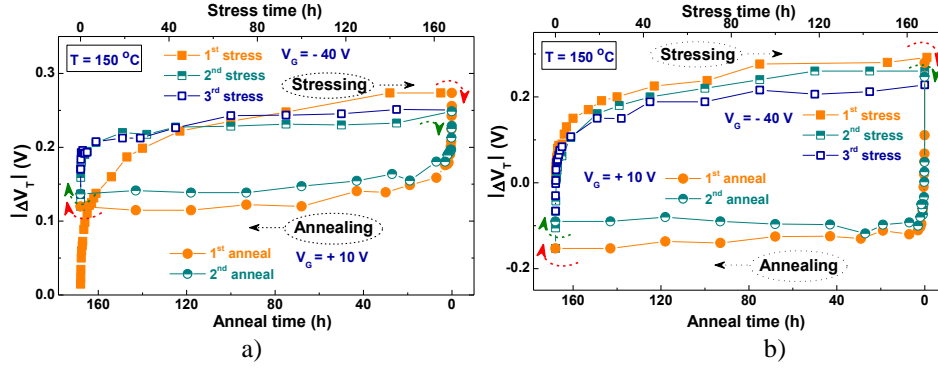


**Fig. 6** Time dependence of  $\Delta N_{ot}$  and  $\Delta N_{it}$  (and  $\Delta V_T$  at inserted figure) for different: (a) stress voltages at the same temperature ( $150^\circ\text{C}$ ); (b) stress temperatures for the same stress voltage ( $V_G = -40\text{ V}$ ).

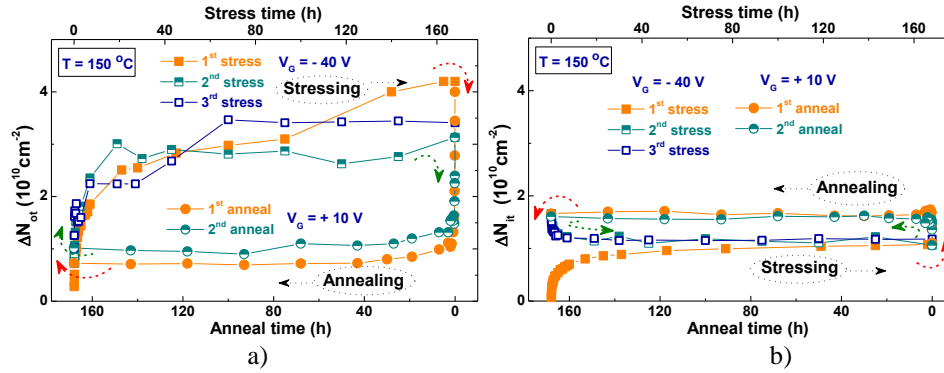
In Fig. 7 it can be seen that evolutions of  $\Delta V_T$  were similar in both types (p- and n-channel) of transistors, and that overall variations of  $V_T$  over the entire stress and anneal sequence were greater in n-channel ones. Besides that, in Fig. 7(a) ( $\Delta V_T$  in p-channel transistor) it can be seen that  $V_T$  was significantly recovered, but the initial stress-induced  $\Delta V_T$  did not fall below 100 mV after both annealing. During repeated NBT stress the major portion of  $\Delta V_T$  induced by the initial NBT stress is also quickly restored. The changes of  $\Delta V_T$  tend to decrease on each new repetition of annealing, indicating that there is a non-reversible component of  $\Delta V_T$ , which resulted from the portion of non-annealed stress-induced oxide-trapped charge and interface traps and new created interface traps.

In Fig. 8 it can be seen that the shapes of  $\Delta N_{ot}$  mostly follow the shapes of  $\Delta V_T$  over the complete sequence. This suggests that charge trapping/detrapping processes occurring in oxide bulk could be of primary importance for NBTI in power VDMOSFETs. It should be emphasized that although recovery of  $V_T$  during annealing was observed, it does not seem to be a true device recovery because only  $\Delta N_{ot}$  decreases while  $\Delta N_{it}$  simultaneously increases. This increase could be ascribed to a reversed drift direction of positively charged species. It should be emphasized that similar to radiation induced degradation, degradation induced by NBT stressing in power VDMOSFETs might be associated with gate oxides as reservoirs of hydrogen related species required for both passivation and

depassivation processes occurring at the SiO<sub>2</sub>-Si interface during and after the stress. Accordingly, some elements of the approach applied in standard model of irradiation damage [15, 23, 55, 56] might be reasonable in considering the NBTI in power VDMOSFETs.



**Fig. 7** Evolution of  $\Delta V_T$  in power VDMOSFETs during complete sequence of NBT stressing and positive bias annealing steps in: (a) p-channel and (b) n-channel.



**Fig. 8** Evolution of (a)  $\Delta N_{ot}$  and (b)  $\Delta N_{it}$  in p-channel power VDMOSFETs during complete sequence of NBT stressing and positive bias annealing steps.

Also, in Fig. 8 it can be observed that the changes of  $\Delta N_{ot}$  and  $\Delta N_{it}$  tend to decrease during each new repetition, indicating that non-reversible components of  $N_{ot}$  and  $N_{it}$  tend to increase. Namely, the repetition of NBT stress after annealing re-created the annealed portion of  $N_{ot}$ , while removed the reversible component of  $N_{it}$ . It is interesting that interface traps created during each annealing are almost completely removed during following NBT stress. The second and the third NBT stresses actually lead to decrease of  $N_{it}$  to value approximately equal to one after the first stress. In this way  $\Delta N_{it}$  remains almost on the same value as it was after the first NBT stress. Besides, it could be noticed that the values of  $\Delta N_{ot}$  are significantly higher than that of  $\Delta N_{it}$  after each NBT stress. On the other hand, the values of  $\Delta N_{ot}$  after annealing become almost the same as values of  $\Delta N_{it}$  after NBT stresses, at these experimental conditions.

The observed changes could be ascribed to the available oxide trapped charge and interface trap precursors, as well as to the presence of hydrogen species that significantly contribute to the observed  $\Delta V_T$ ,  $\Delta N_{ot}$  and  $\Delta N_{it}$  evolution.

#### 4. CONSECUTIVE RADIATION AND NBT STRESS EFFECTS

The devices used in the investigation of consecutive irradiation and NBT stress were also the commercial p-channel power VDMOSFETs IRF9520, whose important properties were presented in Sect. 3. In this investigation two different experiments were performed: 1) after NBT stress the samples were irradiated (NBT-RAD experiment) and 2) after irradiation samples were NBT stressed (RAD-NBT experiment). In the first experiment NBT stress was followed by spontaneous recovery (24 hours), irradiation, by another spontaneous recovery (168 hours) and by thermal annealing. In the second experiment irradiation was followed by spontaneous recovery (24 hours), NBT stress, another spontaneous recovery (168 hours) and by thermal annealing. In both experiments, all stresses and recoveries, as well as thermal annealing were done under the same conditions. During NBT stresses and irradiations the source and drain were grounded. NBT stressing was performed in thermally stable Heraeus chambers at 175 °C (168 h) with device gates biased at  $V_G = -45$  V.

Chosen voltage value of -45 V enables to observe notable  $\Delta V_T$  within a reasonable period of time. Namely, stressing of these devices with gate voltage within the range found in manufacturer's data sheet (maximal gate voltage -20 V), would lead to small degradation which would be notable after a long period (thousands of hours) [16]. Chosen voltage value of -45 V exceeds the range of gate voltages allowed for application in the investigated devices, but it is within the range of gate voltages used for NBT stress experiments on these power devices. Regarding the choosing of temperature, significant device degradation at room temperature can be observed only at stress voltages which are just few volts below the gate oxide breakdown voltage (70 V), and can be ascribed to tunnelling effects [57], while at  $T > 175$  °C, backward interface reactions can be activated [58]. It should be mentioned that in this study the NBT stressing was limited to 168 h with the aim of shortening the experiment. Therefore the combination of bias and temperature value, as well as NBT stress duration was chosen in order to obtain optimal conditions for this investigation.

The irradiation was performed at Department of Radiation and Environmental Protection at Institute for Nuclear Sciences, Vinča, Serbia. The devices were gamma irradiated by Co-60 (dose rate of the source was 0.5 Gy(SiO<sub>2</sub>)/min) up to a total dose of 75 Gy (total duration of 150 min). The devices were irradiated without gate voltage applied, and with applied positive (+10 V) and negative (-10 V) gate voltage. The chosen voltage value of 10 V enables to enhance irradiation effects, and to simulate real cases of biased device in the working conditions. Besides that, the chosen total dose of 75 Gy (relatively low compared to very high doses that could be achieved in the devices assembled in satellites) provides to avoid that radiation effects in devices significantly surpass and masks the NBT stress effects. In addition, the thermal annealing (the final phase in both experiments), of all devices, was performed at  $T = 175$  °C during 168 hours without any bias applied. Both spontaneous recovery were carried out at room temperature of  $T = 25$  °C, also, without any bias applied.

In order to detect and monitor the degradation during all phases of experiments, each one was interrupted after certain, predefined periods to measure the device transfer  $I_D$ - $V_{GS}$  characteristics. The highly precise source measurement units (SMUs) Keithley 237 (for drain biasing and drain current measurement) and Keithley 2400 (for sweeping the gate voltage), both controlled by PC over IEEE 488 GPIB were used for devices electrical characterization. It should be noted that all measurements were performed at room temperature.

In Figs. 9 and 10 are presented  $\Delta V_T$  in p-channel power VDMOSFETs during the NBT stress - irradiation and irradiation - NBT stress experiment, respectively. All devices subjected to initial NBT stress in NBT stress-irradiation experiment follow the same degradation curve of  $\Delta V_T$ . On the other hand, irradiation of virgin devices (in irradiation - NBT stress experiment) has induced significant negative  $\Delta V_T$ , which increased with total dose received and were dependent on the gate bias applied. In the case of zero bias applied, the value of  $\Delta V_T$  was the lowest, while at gate bias applied of 10 V it was significantly more pronounced. At the same  $\Delta V_T$  was somewhat more pronounced in the case of positive bias applied ( $V_G = +10$  V) than at negative bias applied ( $V_G = -10$  V) [11].

The underlying changes of  $\Delta N_{ot}$  and  $\Delta N_{it}$ , determined by the commonly used subthreshold midgap technique [59], during the NBT-RAD experiment are presented in Fig. 11, while underlying changes of  $\Delta N_{ot}$  and  $\Delta N_{it}$ , during the RAD-NBT experiment are presented in Fig. 12 [60].

It should be mentioned that the microscopic origin of the NBTI related degradation as well as radiation related degradation was extensively investigated. Namely, the changes of oxide trapped charge and interface traps, which lead to corresponding threshold voltage shift, could be explained by numerous models of the responsible mechanisms for these changes during NBT and gamma radiation stress, as well as during the annealing of stressed devices. In many models changes of  $\Delta N_{ot}$  and  $\Delta N_{it}$  are the result of electro-chemical processes that occur in the gate oxide and at SiO<sub>2</sub>-Si interface. These electro-chemical processes and underlying reactions are based on the charge traps precursors existing in the gate oxide and at SiO<sub>2</sub>-Si interfaces. Some models include reactions at SiO<sub>2</sub>-Si interface involving holes and their transport through the oxide. Besides that there are models which can properly explain results obtained in the investigations of NBTI and radiation degradation, which are based on transport of hydrogen species ( $H^\bullet$ ,  $H^+$ ,  $H_2$ ,  $OH^\bullet$ ,  $H_2O$ ,  $H_3O^+$ ). The presence of hydrogen species is associated with the presence of hydrogen as a common impurity in MOS devices. The result in this investigation can also be explained by mentioned models.

Mechanisms responsible for NBT stress induced changes of  $\Delta N_{ot}$  and  $\Delta N_{it}$  are bias dependent and thermally activated [9, 16, 20, 23, 24, 26-29]. Interpretations of mechanisms responsible for degradation, very often, include various forms of model based on the assumption that previously passivated defects at SiO<sub>2</sub>-Si interface release hydrogen species which diffuse into the oxide and leave the interface traps [17, 19, 53, 61]. In these models dispersive hydrogen species motions were proposed, due to various assumptions related to trap controlled hydrogen migration in the oxide [62-65].

In many investigations of NBTI, there were proposals that interface trap creations could be reaction controlled mechanism rather than diffusion controlled one [18]. Generation of positive charge in the oxide bulk due to hole trapping has been reported in addition to generation of interface traps [18, 62, 63].

Although there was a controversy on the role of trapped charge in NBTI [18], numerous studies suggested that hole trapping dominantly contributes to degradation [20, 66, 67]. This might lead to the proposal of a new charge trapping model, which makes connection between the NBTI degradation and the creation of switching oxide traps, and that is consistent with recovery data showing dispersion over the wide range of time.

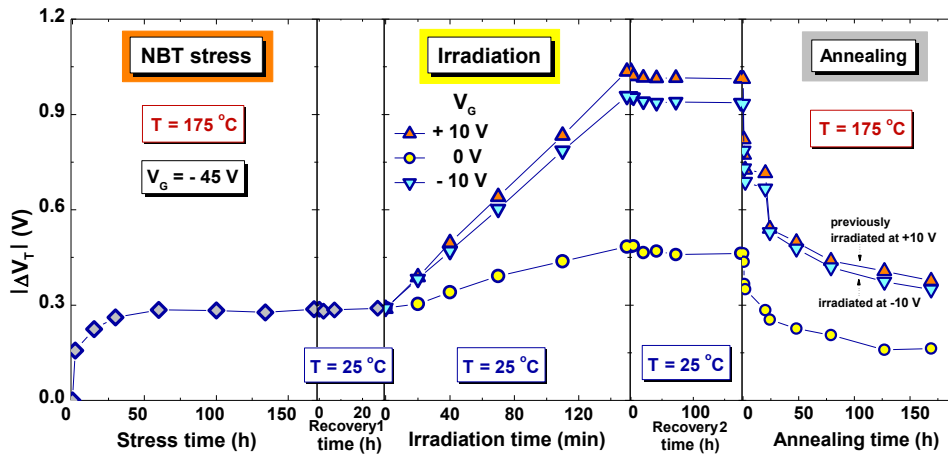


Fig. 9 Behaviour of  $\Delta V_T$  in p-channel power VDMOSFETs (IRF9520) during the NBT stress-irradiation experiment [11].

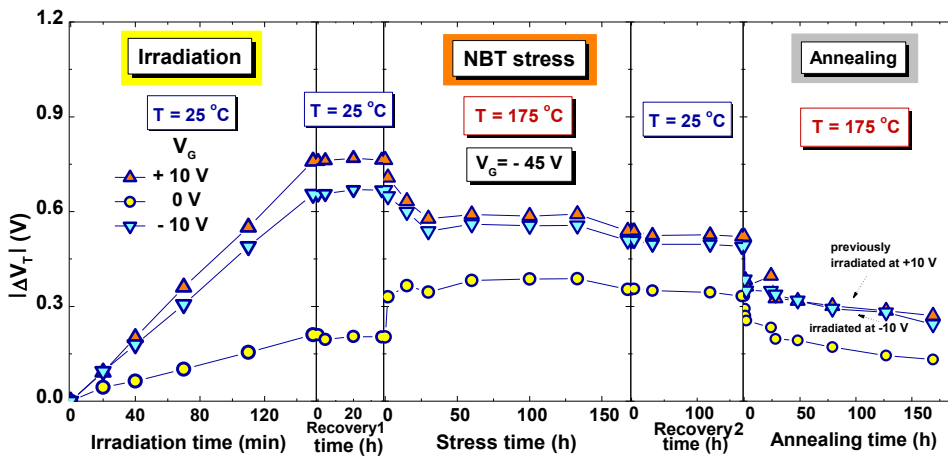


Fig. 10 Behaviour of  $\Delta V_T$  in p-channel power VDMOSFETs (IRF9520) during the irradiation-NBT stress experiment [11].

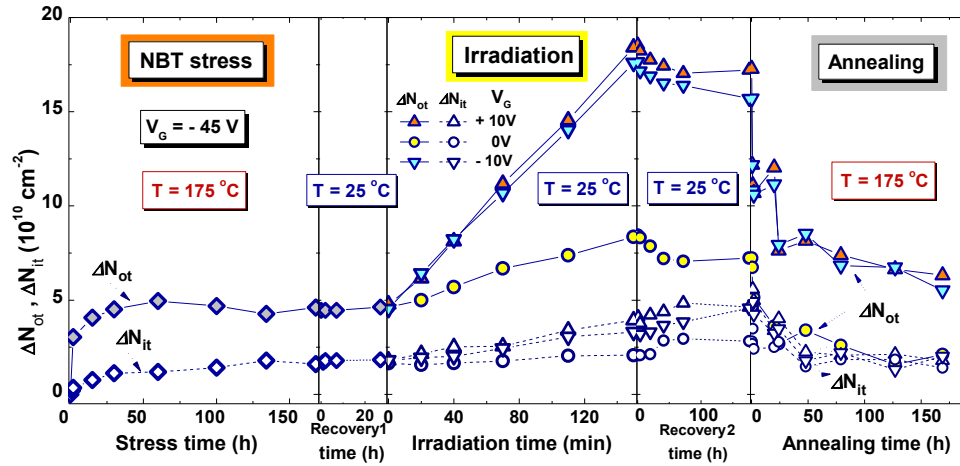


Fig. 11 Behaviours of  $\Delta N_{ot}$  and  $\Delta N_{it}$  in p-channel power VDMOSFETs (IRF9520) during the NBT stress-irradiation experiment [60].

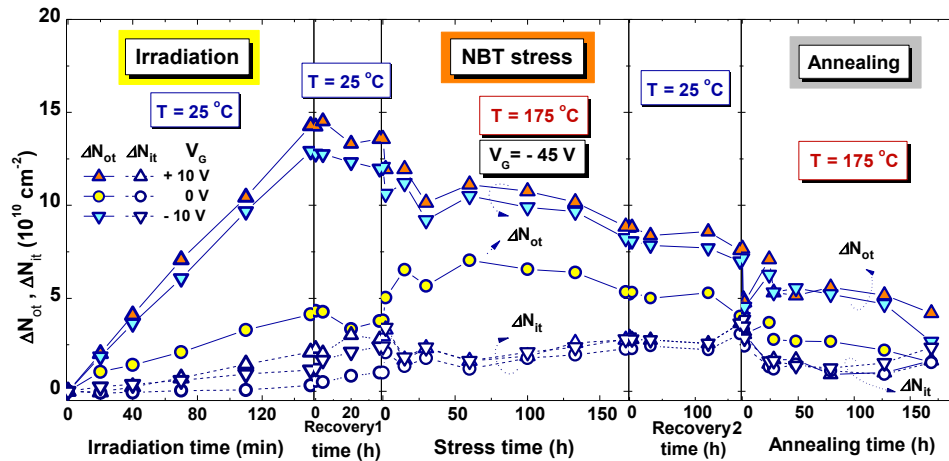
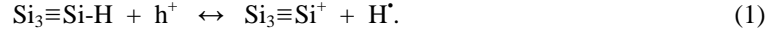


Fig. 12 Behaviours of  $\Delta N_{ot}$  and  $\Delta N_{it}$  in p-channel power VDMOSFETs (IRF9520) during the irradiation-NBT stress experiment [60].

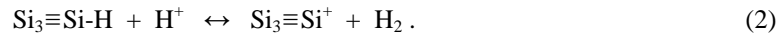
The results obtained in our investigations, in power VDMOSFETs, signify that major contribution to NBTI in these devices also originates from the oxide trapped charge. The other important feature of NBTI in power VDMOS devices is additional generation of interface traps in devices annealed under the positive gate bias. It is important to note that our results indicate strong bias dependence of the processes which occurred during both stress and annealing. This suggests that one or more kind of charged species could be involved. The holes induced and/or accumulated under the gate oxide have to be among them, as negative gate bias stress resulted into significant threshold voltage shift. We also believe that hydrogen, as a most common impurity in MOS devices, which is widely considered as the primary agent of instabilities associated with radiation damage [55, 56], hot carrier injection, and high electric field stress [68, 69], has to be considered in BTI as well.

## 5. UNDERLYING MECHANISMS

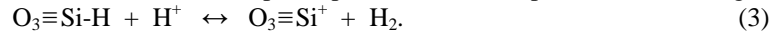
During NBT stress high electric field at elevated temperature in the presence of holes ( $h^+$ ) may cause dissociation of weak Si-H bonds at the interface thus leading to creation of interface traps and hydrogen atoms:



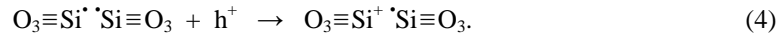
Released highly reactive hydrogen atoms ( $\text{H}^\cdot$ ) could react with holes from the channel and create hydrogen ions ( $\text{H}^+$ ). The holes originate from the channel owing to applied high negative gate bias of -45 V. Created hydrogen ions may dissociate Si-H bonds at the interface, thus creating additional interface traps:



Alternatively, hydrogen ions could drift away, due to applied high negative gate bias, from the interface into the oxide bulk and participate in creation of positive oxide charge:



Buildup of oxide charge under the high negative oxide field can be also explained by hole trapping at oxygen vacancy defects near the interface:

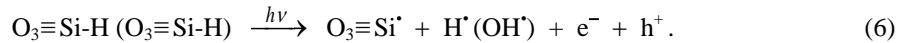
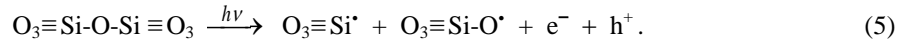


It should be mentioned that oxide-trapped charge and switching traps (interface traps and near interface oxide traps so-called “border traps” [70]) are all positive in the case of p-channel MOS transistor and thus contribute to a negative  $\Delta V_T$ .

In Fig. 11 (NBT-RAD) it can be observed that during NBT stress the increase of  $\Delta N_{ot}$  was more pronounced than  $\Delta N_{it}$  and that these values were not affected notably by the subsequent spontaneous recovery at 25 °C, as the temperature was too low to activate any process of relevance for the phenomena under the investigation. Because of that the changes of  $\Delta V_T$  were not affected notably by the subsequent spontaneous recovery.

Regarding the ionizing radiation, the knowledge acquired during many years of microelectronic devices testing [15, 71, 72] has been successfully implemented in explaining the impact of ionizing radiation on VDMOSFETs, and an appropriate model of responsible electrochemical process was proposed in [2]. The essence of the model is an assumption that weak bonds between silicon and oxygen atoms in the oxide structure (as well as the bonds in the defects between silicon atoms and hydrogen/hydroxyl groups and/or atomic clusters containing hydrogen) and near the oxide-silicon interface would be broken due to irradiation.

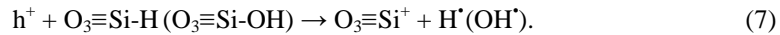
Namely, high energy (MeV magnitude) ionizing irradiation breaks not only weak Si-H and Si-OH bonds in the oxide, but also the regular Si-O-Si bonds and generates electron-hole pairs in the gate oxide structure:



Although some of these pairs recombine, most of the generated electrons, however, quickly escape from the oxide, while most of the holes (which are weakly mobile) get captured in the oxide volume on oxygen vacancy defects  $\text{O}_3\equiv\text{Si}^\cdot\text{Si}\equiv\text{O}_3$ , contributing to creation of positive oxide trapped charge over a reaction identical to (4).

When the gate is positively biased, the electrons almost immediately [35] remove through the gate, while when the gate is negatively biased, the electrons remove through the semiconductor. In the case of higher electric field applied more unrecombined holes remain trapped in the oxide which leads to higher oxide trapped charge. Small difference between irradiation effects obtained for positive gate bias and negative gate bias can be explained by small difference (due to different surface potential) between the corresponding values of electric field in the oxide, which affects the removal of electrons.

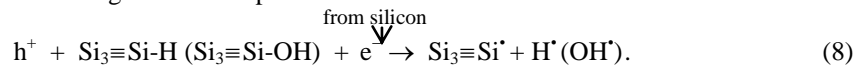
It should be mentioned that a fraction of the holes may dissociate weak Si-H and Si-OH bonds and can be trapped again in the oxide contributing to oxide trapped charge increase:



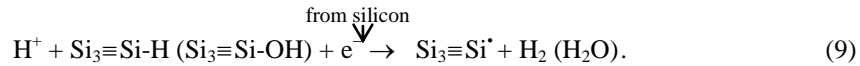
Also, a fraction of the holes could be trapped at oxide defects, such as oxygen vacancies, also contributing to oxide trapped charge increase over a reaction identical to (4).

As mentioned before, holes can react with hydrogen atoms forming the ions. These hydrogen ions also could contribute to the oxide trapped charge increase [56].

Released holes could dissociate weak  $Si_3\equiv Si-H$  and  $Si_3\equiv Si-OH$  bonds which exist at the interface creating interface traps:



Similarly, hydrogen ions could contribute to creation of interface traps:



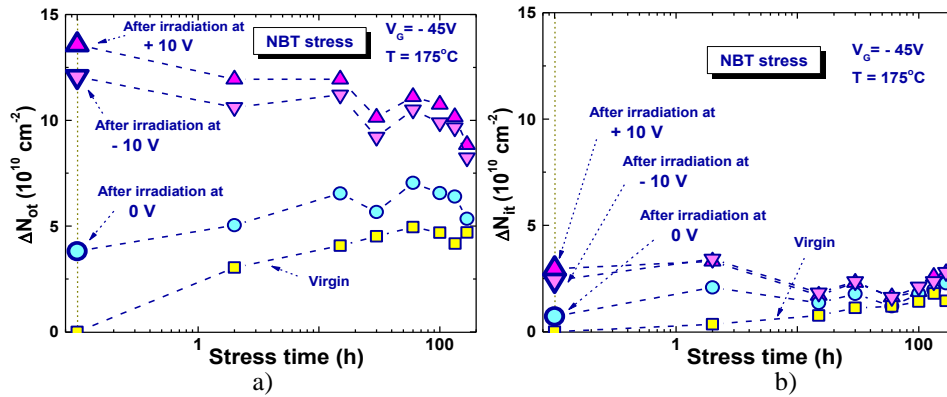
In Fig. 12 (RAD-NBT) it can be seen that the values of  $\Delta N_{ot}$  are significantly higher than those of  $\Delta N_{it}$  after irradiation and that all changes were the smallest in the case of irradiation without gate bias applied. Also, it can be seen that both  $\Delta N_{ot}$  and  $\Delta N_{it}$  were somewhat more pronounced in the case of a positive gate bias applied. The reason for these differences is found in the electric field dependence of irradiation effects [12, 35]. It should be emphasized that post-radiation spontaneous recovery resulted in a decrease of  $\Delta N_{ot}$  and an increase of  $\Delta N_{it}$  (Fig. 12), although it seems that  $\Delta V_T$  remained stable (Fig. 10).

In NBT stress-irradiation experiment (Fig. 11), the irradiation applied after NBT stressing has produced the additional significant increase of  $\Delta N_{ot}$  and  $\Delta N_{it}$  (leading to additional negative  $\Delta V_T$  presented in Fig. 9) which were slightly lower, but almost the same to those previously observed in irradiated virgin devices during the first step of the irradiation-NBT stress experiment (Fig. 12). This suggests that radiation effects probably were not noticeably affected by NBT stress-induced degradation. Such behaviours can be explained by relatively low temperature (room temperature) and relatively low electric field applied during irradiation, as well as relatively low total irradiation dose.

However, for the effects observed during the NBT stress applied after irradiation (in irradiation-NBT stress experiment) two mechanisms might be responsible. The first one is activation of electrochemical reactions contributing to NBTI, which leads to additional creation of oxide charge and interface traps, and the second one is annealing of irradiation-induced oxide charge due to high temperature (175°C) applied. In order to compare the obtained values of  $\Delta N_{ot}$  and  $\Delta N_{it}$  in Figs. 13 their behaviours during NBT stress of virgin (Fig. 11) and previously irradiated (Fig. 12) devices are presented.



In devices previously irradiated without gate bias applied, the amount of radiation-induced defects was rather small while the number of available defect precursors remained rather high. Therefore, during the NBT stress applied after irradiation additional defects were created. This caused further increase of threshold voltage shift. On the other hand, in devices previously irradiated at positive or negative gate bias, the amount of irradiation-induced defects was much higher and their decreasing during the subsequent NBT stress was actually dominant over the new defect creation. Decreasing of oxide trapped charge and interface traps led to the decrease of threshold voltage shift.



**Fig. 13** Comparative presentation of (a)  $\Delta N_{ot}$  and (b)  $\Delta N_{it}$  during NBT stress for investigated devices (virgin and previously irradiated).

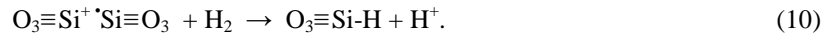
Also, in order to compare obtained values of  $\Delta V_T$  in Fig. 14 behaviours of  $\Delta V_T$  during NBT stress of virgin (Fig. 9) and previously irradiated (Fig. 10) devices are presented [60]. It can be seen that the difference in  $\Delta V_T$  established after irradiation between devices irradiated with positive and negative gate bias applied, decreased very fast at the beginning of the NBT stressing step (within about 24 hours) to a level that remained almost unchanged until the end of NBT stress.

It should be noted that the second spontaneous recovery generally causes a small decrease of  $\Delta V_T$  in the first period in all devices. During the rest of the spontaneous recovery  $\Delta V_T$  remains almost unchanged in NBT-RAD experiment (Fig. 9), while slightly decreases in RAD-NBT experiment (Fig. 10). As in the case of the first spontaneous recovery,  $\Delta V_T$  seems also to be relatively stable during the second spontaneous recovery in both experiments. Despite this, it was observed decrease of  $\Delta N_{ot}$  and increase of  $\Delta N_{it}$  in both experiments (Figs. 11 and 12).

In Figs. 7, 8, 11 and 12 it can be seen that during annealing (last step)  $\Delta V_T$ ,  $\Delta N_{ot}$  and  $\Delta N_{it}$  significantly decreases and that this decrease is more pronounced in devices subjected to NBT-RAD experiment. Although the conditions of NBT stress, irradiation and annealing have been the same in both experiments, the final values of  $\Delta V_T$ ,  $\Delta N_{ot}$  and  $\Delta N_{it}$  were found to depend on the order of stress steps, and were generally lower in RAD-NBT experiment. Such obtained values are the result of two high temperature steps after irradiation in RAD-NBT experiment which have been applied (NBT stress and annealing, both at  $175^\circ C$  for 168 h), so more defects were annealed. In NBT-RAD experiment, only

one thermal annealing step was applied after irradiation that resulted in higher final values. Namely, in NBT-RAD experiment the defects induced by NBT stress and by radiation have been subjected to thermally annealing (175°C) for 168 h, while in RAD-NBT experiment only NBTI defects have been subjected to thermally annealing (175°C) for 168 h, but radiation defects have been subjected to high temperature (175°C) twice as much. More pronounced and faster decrease of all values ( $\Delta V_T$ ,  $\Delta N_{ot}$  and  $\Delta N_{it}$ ) in the initial period of annealing could be ascribed to higher values of created defects after previous steps. The obtained results undoubtedly point to the importance of the order of applied stresses.

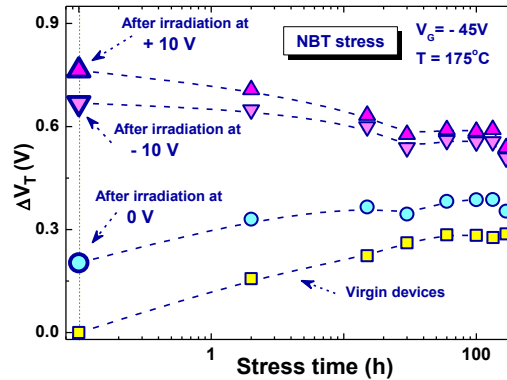
During annealing the devices were not biased, and annealing is strongly thermally supported, as observed by comparing two last steps in the experiments (spontaneous recovery and annealing). The mechanisms during annealing are thermally activated, so the diffusion of neutral species like hydrogen molecules from the areas of high concentrations in oxide toward lower concentrations near the interface could lead to decrease of  $\Delta N_{ot}$  and  $\Delta N_{it}$ . Namely, hydrogen molecules could be cracked at charged oxide traps ( $O_3\equiv Si^+$  and  $O_3\equiv Si^+ \cdot Si\equiv O_3$ ) leading to neutralization of positive oxide traps followed by the  $H^+$  ions releasing [55] over the reverse reaction (3) and:



The decrease of interface traps during the annealing might be also attributed to the hydrogen species (molecule  $H_2$  and highly reactive atom  $H^*$ ) involved in reactions [20]:



Observed threshold voltage decrease is in agreement with comparable published results [73] (power MOS, 105 nm gate oxide, annealed at 175°C), and also fits to Switching-Oxide Traps model used originally as so-called HDL model in interpreting irradiation effects and later in NBTI phenomena [12, 20, 30, 55, 56].



**Fig. 14** Comparative presentation of  $\Delta V_T$  during NBT stress of virgin devices and previously irradiated devices.

## 6. CONCLUSIONS

The main features of independent NBTI and irradiation effects in p- and n-channel, as well as consecutive NBTI and irradiation effects in p-channel power VDMOSFETs have been reviewed. It was shown that experimental results of consecutive stresses complement the results of research of independent NBTI and irradiation effects. The obtained results were analysed in terms of underlying mechanisms. This investigation is shown as important in assessing the device behaviour in real working conditions (where devices are simultaneously under negative bias, irradiation and selfheating). It was shown that radiation induced degradation of previously NBT stressed devices practically was not affected by previous NBT stress. However, previously irradiated devices with and without gate bias applied have shown different behaviours. Devices previously irradiated without gate bias have been further degraded by NBT stress, while devices previously irradiated with gate bias have been partially recovered by NBT stress, due to high temperature introduced by NBT stress. The obtained results undoubtedly point to the importance of the order of applied stresses, indicating that for proper insight into the prediction of device behaviour not only harsh conditions, but also the order of their possible applications have to be considered.

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