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AN INTELLIGENT POWER MOSFET DRIVER ASIC CIRCUIT WITH ADDITIONAL INTEGRATED SAFETY OPERATION FUNCTIONALITY

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Abstract. *This paper presents an extension to the previously presented conference paper [1] a power MOSFET driver ASIC with intelligent driving algorithm approach of the power modern MOSFET devices. The intelligent driving algorithm concept proposes a realization of power MOSFET gate driving with controlled source/sink current of the power MOSFET driver circuit. Such approach enables higher control of the power MOSFET operation behavior, especially during switching events.*
Additionally to the previously published work this paper presents implementation of the intelligent driving algorithm and driver safety operation functions on a single integrated ASIC circuit. The paper concludes with presentation of some functions of the manufactured ASIC circuit in CMOS technology.

Key words: *MOSFET driver, driving algorithm, ASIC, safety functions*

1. INTRODUCTION

Common awareness of preserving a clean environment and trends for low energy consumption affect our daily lives in many ways. One such example could also be recognized in the increasing trend of implementation of different types of modern electrical motor controllers in various applications (e.g. electrical cars). The implementation of electrical motor controllers offers higher conversion efficiency of electrical energy to mechanical energy (e.g. movement, rotation), especially if standard propulsion driving systems using fossil fuels are replaced.

A large assortment of different motor controllers for various drive applications exists on the market. The motor controllers are designed for many kinds of voltage/current ratings where their power ratings vary from several watts up to several megawatts. In many applications the speed control of the attached electrical motor through the use of pulse-

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width modulation (PWM) is achieved. At this point it also must be mentioned that other driving control algorithms [2], [3], [4] exist. Their selection and implementation depends on the application. In such motor controllers power semiconductor devices (e.g. MOSFET, IGBT) switching frequencies from several kHz up to 20 kHz are usually used.

For battery power electrical drive systems, used in electrical cars and other light facilities vehicles, power MOSFET devices dominate due to their high switching current capabilities and low voltage operation. MOSFET devices with their low on-state resistance R_{DSon}, low freewheel diode forward voltage VSD, acceptable low switching power losses, and acceptable low temperature dependence are desired due to low operating voltage, even with the requirement of handling high switching current densities power.

In order to handle high current densities the topology of connecting several power MOSFET drivers in parallel is commonly used. In addition to the aforementioned power MOSFET device electrical properties, the power controller designer must also be familiar with the mechanisms of power loss sources. The analysis of power MOSFET device power loss sources under various operating conditions are described in more detail in [5], [6], [7], [8] and many other papers.

The power losses of switching a MOSFET device can be divided into two parts. The part of the power losses originate from the situation when a device operates in static conditions (R_{DSon}, leakage, V_{DS}). The second part of total power losses contributes power losses when the power device is being switched and can be defined as dynamic power losses.

The static power losses are correlated with the power MOSFET device electrical properties, which are defined by the manufacturer's process capabilities and can be recognized in devices' datasheet. Additionally, the device's electrical properties and operation mode, a non-neglectable part of power loss contribution can also originate from packaging and ambient temperature. As described in papers [9], [10], [11], analyzing the influence of the package to the power losses and power MOSFET performance.

The dynamic part of the total power loss scheme needs to be studied from case to case in more detail since there are many factors influencing the power device efficiency. Major part of the dynamic losses is depended on the connected power device switching characteristics. An important contribution to the overall dynamic part of the total power loss origin from the driver circuit operation analyzed in [13], [14] and also how efficient the power device is being switched.

This paper should be considered as a continuation of the previously published work [1] where some design ideas and techniques of the intelligent power MOSFET driver were addressed. The previous work described in [1] was mostly focused on the analysis of various influences on the power MOSFET device parameters which directly and indirectly influence on the introduced switching algorithm. Additional to this the paper also introduces some additional functionality which would increase safety level of the system where such power MOSFET driver would be implemented.

This paper presents implementation of a proposed intelligent driving algorithm in a form of an integrated circuit – ASIC and introduces some simulation and measurements results of the prototyped integrated circuit.

2. POWER MOSFET SWITCHING

The power MOSFET device is a voltage-controlled device where the connected gate signal controls the device operation mode. Many different power MOSFET devices with various voltage/current/power ratings, static and dynamic properties, technology, package etc. are available on the market. The selection of the power MOSFET device strongly depends on the power MOSFET's operation mode and end application. Consequently, the designer must also consider how adequate control over the power MOSFET device will be achieved.

There are many automotive applications with a power MOSFET device, such as various inverters/converters (e.g. DC-AC). The complete system operation requires an engine control unit (ECU) where a microcontroller or DSP is usually employed. The power available on the I/O pin is limited because the microcontrollers are low voltage and low power devices. Drivers usually have to be positioned between the microcontroller output pin and the power MOSFET control pins (gate). In other words, the driver can be defined as an electrical circuit which provides conditioned signals with adequate electrical energy for the efficient driving of the connected power MOSFET device.

When selecting a driver for controlling a power MOSFET device, or even several power MOSFETs connected in parallel, the designer has to consider many parameters which can influence the switching performance and consequently the performance characteristics of the target application.

2.1. MOSFET device parameters

The simulation circuit shown in Fig. 1 was used for obtaining the simulation results presented in Fig. 2. Simulations were perfomed in SPICE environment.

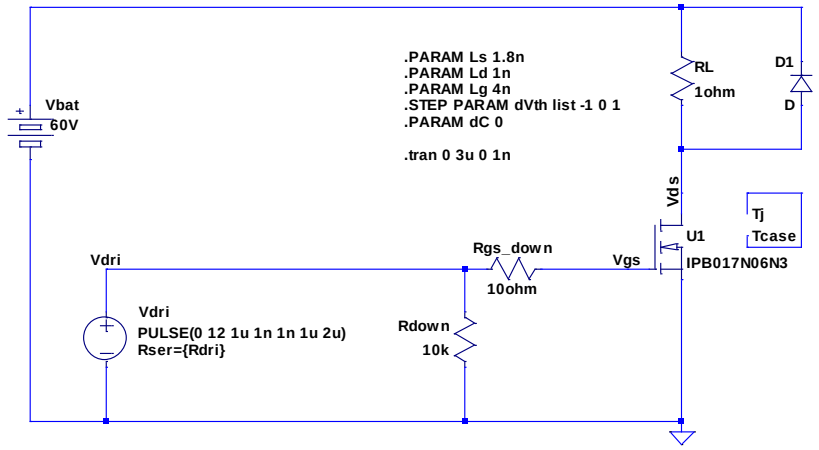

Fig. 1 SPICE simulation circuit

The switching performance is strongly dependent on the selected power MOSFET device, especially the device structure and process deviations – on which the designer has no influence. Since the designer of the application has no influence on the selected power

MOSFET device properties, or the device process deviations, the following presented simulation shows only the deviation of a single parameter – which is in this case the gate threshold voltage *VTH*.

The simulation results presented in Fig. 2 indicates the signal behavior where a single parameter such as a device threshold voltage *VTH* is varied.

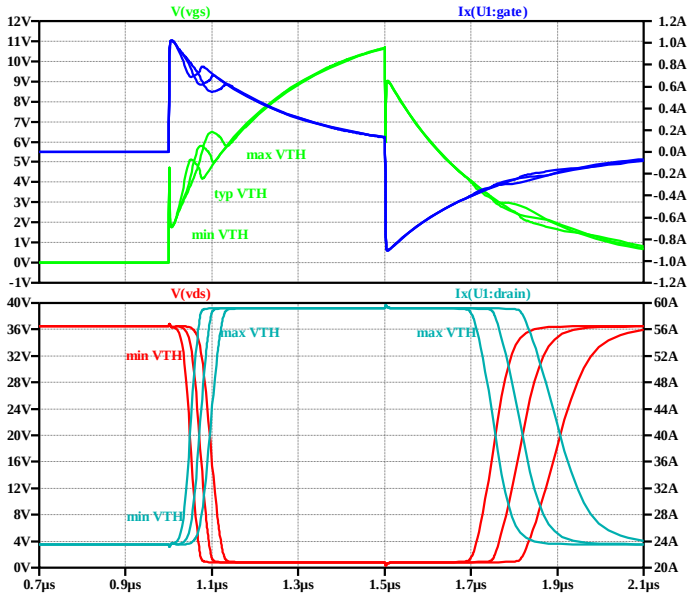

Fig. 2 Switching waveforms simulated with single IPB017N06N3 device in package

Fig. 2 presents SPICE simulation results of the Trench MOSFET device (IPB017N06N3) where voltage *V*(*vgs*) and current *Ix*(*U1:gate*) waveforms of the MOSFET control pin (gate) are shown in the upper graph. The second graph indicates signals of *V(vds)* in *Ix(U1:drain)* of the connected MOSFET device. The results of both graphs shown in Fig. 2 present the dependence of the signals if only the gate threshold voltage *VTH* is varied from the device's specified minimum ("*min VTH*"), typical, and maximum ("*max VTH*") values. (see Fig. 2).

The presented simulation results present only a single device process parameter variation. For further analysis of the power MOSFET switching behaviour also other process variations and interactions of other parameters should be analysed.

2.2. Driver properties

The driver of the power MOSFET device is used for providing a conditioned control signal to the gate of the power MOSFET device in order to control the connected device operation. Voltage/current and power capacities of the driver, whether realized as an ASIC of an electrical circuit with multiple components, have to be tailored to the power MOSFET device or to a network of such devices (usually connected in parallel in order to obtain higher power density capabilities).

The properties and functionality of the selected driver circuit have, in addition to MOSFET device properties and application layout design, an important impact on the power MOSFET switching, performance (losses and efficiency), EMI behaviour, bill-of-material (BOM), size, and price.

The designer has to consider the influences of the aforementioned construction parts in order to accomplish the specified end application requirements, such as EMI compatibility, power density per unit of volume, and many others. In Fig. 3 the simulation results of power MOSFET device operation are shown for different driver output current capabilities. The simulation circuit and description of the presented graphs in Fig. 3 are identical to the previously presented simulation results in Fig. 1. The output current driver capability is controlled with an adjustment of internal driver resistance *Rdri* (0Ω, 12Ω and 24Ω). The resistance *Rdri* influences the power MOSFET device switching du/dt and di/dt performance as seen in the lower graph of Fig. 3. The impact of the driver's current capability is even more noticeable when the power MOSFET device is being switched 'off.' Not only the du/dt and di/dt behaviour is considerably altered, but also additional time delays occur. Those time delays result not only in an increase of switching power losses, but also in a limited available minimal time pause ('dead-time'). The 'Dead-time' needs to be controlled and adjusted in the case where operation of two or more power switches (e.g. H-bridge circuit topology) can lead to uncontrolled coincident operation. This can establish a short circuit path between the connected power source terminals. When a short circuit path through the series connected power switches occurs, it can lead to a sudden increase in the power source current, increased power losses, and elevated temperatures. This occurrence can in some cases also lead to power switch destruction and even possible application failure.

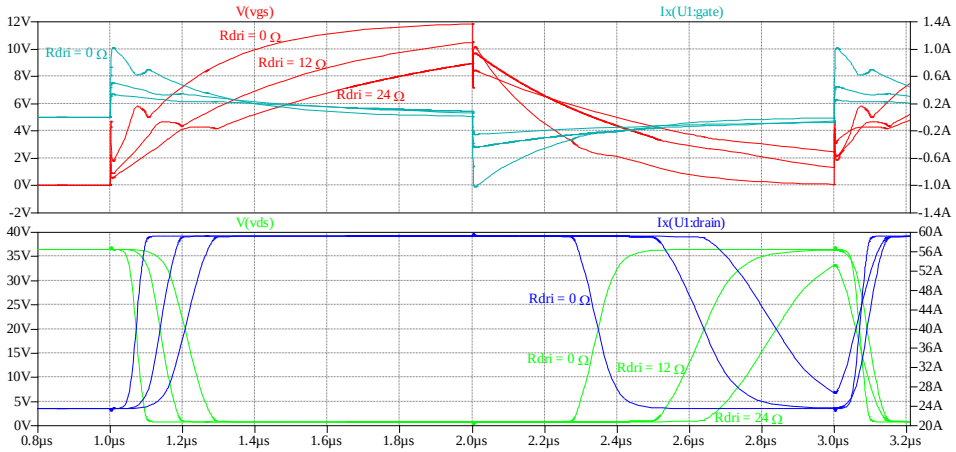

Fig. 3 Switching waveforms of the power MOSFET with different driver current capabilities (simulated with R_{dri} (0Ω, 12Ω and 24Ω)/ driver internal resistance)

As previously mentioned power MOSFET device and driver selection, the board layout also plays an important role in the power system design. The electrical and the thermal properties of the board used for final power system components assembly should

be considered with respect to the expected operation of the power MOSFET device, and the end application environment conditions (e.g. ambient temperature, storage, mechanical loads, EMI, etc.).

The detailed analysis of the board layout is not the main scope of this paper, so at this point the analysis of direct and indirect effect factors of the board layout to the power MOSFET device and driver operation is not discussed in detail. Some further approaches of different analysis of the power module layout are highlighted in [15], [16], [17].

3. ASIC DRIVER CONCEPT

In the following section some of the design ideas and techniques of an intelligent power MOSFET ASIC driver are introduced. This concept emphasizes only some highlighted approaches about power MOSFET driving, implementation of protection, and safety functionality. An idea of the ASIC implementation is also introduced.

3.1. Power MOSFET driving

The driving of the power MOSFET device has a direct influence on the power MOSFET device's performance, operation reliability lifetime, and also effects correlated to the EMI susceptibility must not be neglected. In the past many of the power MOSFET device driving techniques and approaches were introduced. In the previously reported work [18], [19] alternative MOSFET drivers with voltage controlled output are summarized and more detailed described.

The proposed driving technique, instead of 'conventional' voltage control of the V_{GS} (voltage applied between gate and source) of the connected power MOSFET, proposes the use of an integrated current controlled source connected to the ASIC driver output.

The idea of using current controlled ASIC power MOSFET driver output is to obtain control over the source/sink current provided to the gate terminal of the power MOSFET device during each of the switching segments.

An introduced intelligent current driving technique optimizes switching efficiency and enables higher level of control of the *du/dt* and *di/dt* during switching of the power MOSFET device. Additional features of the ASIC driver should also implement various algorithms which can automatically adjust the ASIC driver internal current driving algorithm parameters regarding the sensing values of the power MOSFET device such as die power, MOSFET die temperature, voltage drop V_{DSon}, etc.

In Fig. 4 a block diagram of the integrated intelligent power MOSFET driver ASIC is presented. The block diagram introduces an implementation of the intelligent algorithm with safety functions and configuration of the input/output pins which are more in detailed analyzed in previously published work [18]. The introduced block diagram of the intelligent driver has, beside power supply pins, also additional input/output pins which are required for its operation.

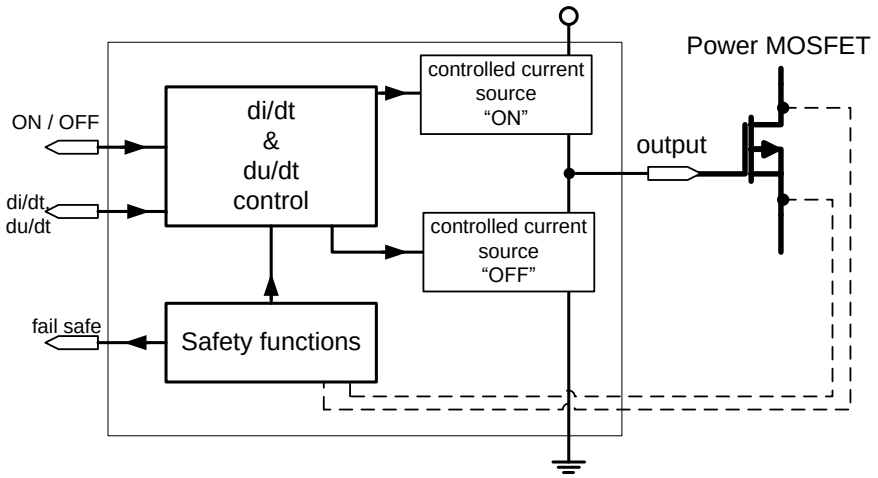

Fig. 4 Block diagram of the intelligent driver and safety function of the MOSFET driver ASIC

Control signal connected to the "ON/OFF" pin usually provided from an external microcontroller unit is used for controlling an operation of the connected power MOSFET. The signal "ON/OFF" pin is connected to the internal functional block "di/dt & du/dt control" and controls operation of the connected "controlled current source "ON" " and "controlled current source "OFF". The controlled current source additionally marked with "ON" is used for the signal conditioning of the gate control signal during switching the power MOSFET transistor on. The second current source, marked with "OFF", is active when the power MOSFET is being switched off – when there is no conduction between drain and source terminal of the power MOSFET.

An external signal connected to the pin "di/dt, du/dt" is used for programming the current values of both controlled current sources separately. The pin named "output" is connected to the gate terminal of the connected power MOSFET device.

An implementation of the safety functions are presented with functional block "Safety functions". This block is used for monitoring voltage drop between source and sink of the connected power MOSFET device and the temperature of the driver ASIC. When any of the observed values of the voltage drop or temperature is exceeded the operation of the driver is disabled. The internal signal of the "Safety functions" block overrides the command provided from the external control signal connected to the "ON/OFF" pin and set the highest available sinking current of the "controlled current source OFF". When any of the predefined monitored values is exceeded the "Safety functions" block immediately turns off the connected power MOSFET device in order to avoid any further uncontrolled events and possible also any further damage of the application. Furthermore, the "fail safe" signal, a part of the "Safety functions" block, is connected to the external control unit and is used as an interrupt for external control unit when any of the monitored operation parameter (e.g. overcurrent, temperature, battery voltage) of the power MOSFET is out of the predefined limits.

3.2. ASIC protection and safety functions

In addition to the ASIC driver's efficient and reliable driving of the connected power MOSFET device, implementation of safety functionality should be considered. Standard functionality can be already found in existing solutions, such as those mentioned in [20] and [21].

The proposed implementatin of the power MOSFET driver consists of implementation of the following safety functions: the temperature detection of the power MOSFET driver die, the monitoring of the battery voltage and the overcurrent protection of the controlled power MOSFET device.

3.3. ASIC driver implementation

Power MOSFET device drivers are usually assembled in different IC packages (e.g. SOIC). The influence of connections of the drivers and controlled power MOSFET devices also differ between applications, and the parasitic influences of such connections cannot be universally determined. In order to optimize connections influences to the performance an combined integration of the power MOSFET device's structure and the ASIC's driver circuit on a single die is proposed. Fig. 5 shows an ASIC integrated power MOSFET driver protoype with implemented introduced intelligent driving algorithm and safety functions.

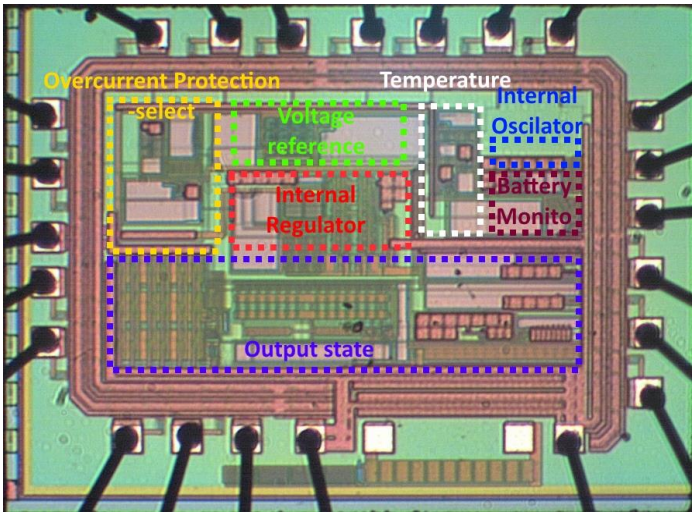

Fig. 5 Intelligent power MOSFET driver prototype photo; die size: (1612 x 1192) µm

The ASIC has been prototyped in 0.25µm CMOS technology with maximal breakdown voltage of 40V.

In Fig. 5 marked area on the prototyped power MOSFET driver die gives an illustrative indication of individual function blocks as introduced in a block diagram shown in Fig. 4. Additionally also some peripheral function block are added required for integrated circuit operation. The detailed description of the peripheral function blocks presented in Fig. 5 is not the topic of this paper.

Such an approach reported in [20] was previously mentioned, but the solution only addresses high voltage power devices where switching current densities do not represent any notable influence on the integrated ASIC's driver operation. The combination of the power and CMOS structure on a single substrate introduces new challenges for future work.

3.4. Measurement results of the prototyped ASIC

In this section some preliminary measurement results of the prototyped ASIC are presented. Figure 6 and 7 show oscilloscope waveform captures of the "input" and "output" signal of the ASIC at three different set values of the control current source "ON" and "OFF", respectively. The ASIC was supplied with a 12VDC supply and load capacitor of 10nF on the ASIC "output" pin was connected. The "input" pin was controlled with an external signal generator.

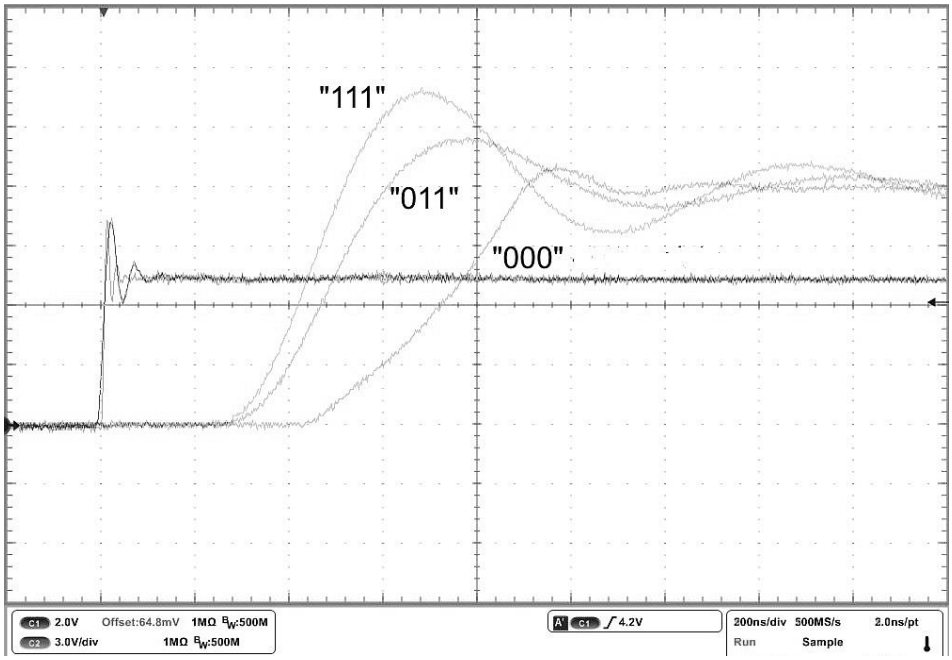

Fig. 6 Switching waveform of the intelligent power MOSFET driver prototype during load capacitor charging

In Fig 6 an "output" pin voltage signal behaviour connected to the load capacitor of 10nF at maximum ("111"), middle ("011") and minimum ("000") pre-set current source capability of the controlled current source "ON" is shown. The measurement results show influence of different controlled current source values which directly affects the du/dt slope of the connected capacitor load during charging. Current capability of the controlled current source "ON" ranges from 550mA to 100mA for maximum and minimum pre-set values, respectively.

Fig 7 present waveforms when the connected capacitor load for different pre-set controlled current source “OFF” values during discharging. The voltage signal “output” marked as “111” on the Fig 7 present signal behaviour when maximal available discharge current in the ASIC is pre-set. The “output” signal marked with “000” indicated signal behaviour when minimal available discharge current of the controlled current source “OFF” was selected. The range of pre-set current values of the controlled current source “OFF” could be set in eight programmable steps from 330mA to 270mA.

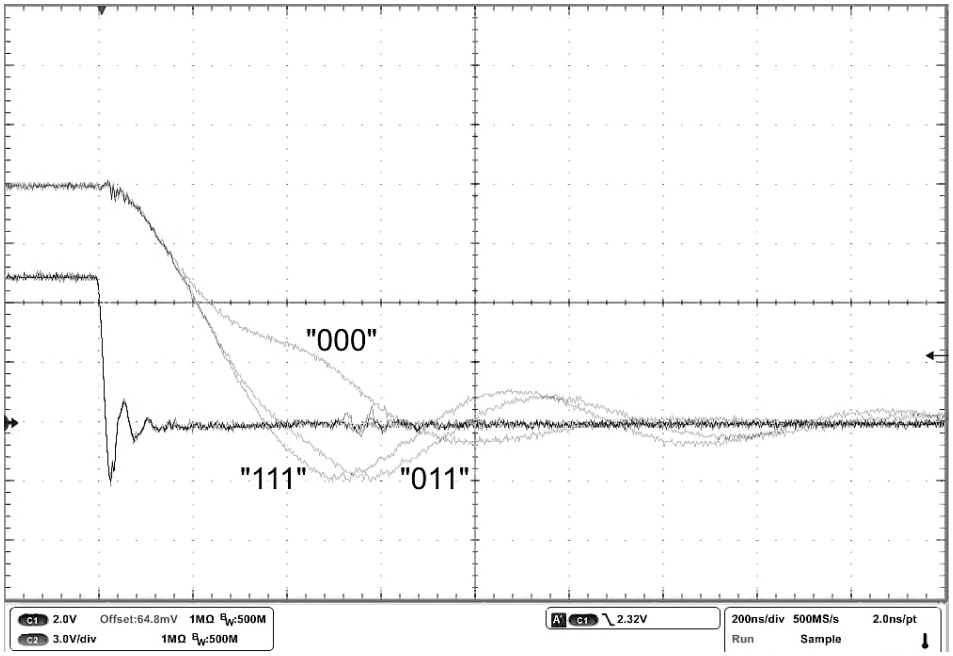

Fig. 7 Switching waveform of the intelligent power MOSFET driver prototype during load capacitor discharging

Presented measurement results show implementation of the controlled current source “ON” and “OFF” in first ASIC prototype. The ASIC prototype proved that independent control of charging and discharging of the connected loads capacitor is achieved and measured without implementation of any external electrical components.

4. CONCLUSION

An important part of power MOSFET device operation requires a novel approach on the efficient and reliable control of such devices. The paper introduces some simulation results of various influences of the power MOSFET device parameters and analyses their effect on switching performance. The paper concludes with an introduction of some design aspect and ideas of the intelligent ASIC drivers and driving algorithm, the integration of protection and safety functions, and proposes a combined implementation of the ASIC

driver and power MOSFET device on a single die. The article also introduces the photo of the first prototyped power MOSFET driver ASIC with intelligent driving algorithm and some safety functions integration.

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