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NONLINEARITY COMPENSATION AND ACCURACY IMPROVEMENT METHOD FOR AN OPTICAL ROTARY ENCODER

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Abstract. *This paper presents a method for the nonlinearity compensation of an optical rotary encoder. The proposed method is based on the application of 1) a special 4-bit mixed analog-digital circuit used for the generation of a quasi-linear signal, and 2) a two-stage nonlinear ADC which performs linearization and digital conversion of the quasi-linear signal at the same time. The quasi-linear signal is obtained by combining fragments of phase-shifted sinusoidal signals, where each fragment is presented with a 4-bit digital code. In the continuation, the quasi-linear signal is linearized with the two-stage nonlinear ADC of a compact design based on the application of a single flash ADC in both conversion stages. Additionally, the design of the flash ADC is modified so that the number of employed comparators is equal to the resolution of the flash ADC. For instance, by linearizing an optical rotary encoder using the 4-bit mixed analog-digital circuit and the 20-bit two-stage nonlinear ADC containing 10 comparators, the maximal value of the absolute measurement error can be reduced to* $3.23 \cdot 10^{-5}$°.

Key words: *Accuracy, compact design, flash ADC, linearization, mixed analog-digital circuit, optical rotary encoder*

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1. INTRODUCTION

An optical rotary encoder (ORE) is a sinusoidal transducer that can be used to measure angular displacement, position, and velocity. The OREs are convenient for applications in control systems and robots, heavy civil or military equipment and vehicles, sophisticated medical equipment, computer peripherals, antenna and radar systems, etc. However, OREs exhibit a high nonlinearity of the transfer characteristic, i.e. their output voltage signals (sine and cosine) nonlinearly vary with the change of the angular position that is being measured [1]. As a consequence, even a significant change in the angular position can lead to a small or undetectable output voltage change. For this reason, unsatisfying measurement accuracy can be expected in some sections of the measurement range.

As a solution to the previous problem, this paper proposes a nonlinearity compensation and accuracy improvement method developed for OREs, which can be adapted for linearization of other types of sinusoidal encoders, such as magnetic encoders and resolvers [1]. The proposed linearization method needs no processing power like digital linearization techniques [2] and is more flexible when compared to analog linearization techniques [3], i.e. it can be used for all sinusoidal sensors. In [4], a phase-locked loop resolver converter that is utilizing full-wave rectifiers to obtain the absolute values of the modulated resolver signals was reported. At the output of the converter, a triangular voltage signal and two digital signals were obtained, representing together a measure of the input angle. However, the employment of rectifiers for the resolver linearization introduces additional nonlinearity which contributes to the overall measurement error equal to ±0.3° over the full 360° range. In [3], an all-analog phase-locked loop converter based on a triangular-to-sine converter was used for angular position measurement with an error of ±0.05° in the 360° range. However, the use of phase-locked loop converters provides a loop filter which prolongs the response time and disturbs the converter stability. A high accuracy resolver-to-linear converter composed of a demodulator and a linear shaper was proposed in [5]. The proposed converter is using one phase of the resolver signal to obtain a linear signal and reduce a maximal absolute error to ±0.014° in the 360° range. In [6], a digital converter was used with sinusoidal transducers to determine an unknown angle without a look-up table. This method is based on dividing the measurement range into N equally wide sections. A coarse value of the measured angle is first determined by identifying the belonging section. The fine value of the measured angle is determined using a phase-shifted tangent signal and a linear approximation. As a result, the maximal measurement error decreases with the increase of the number of sections N, and for N=16 it is 0.0365° (for N=64 the error is $6 \cdot 10^{-4}$°).

A linearization method proposed in this paper is based on the application of two circuits. One is a 4-bit mixed analog-digital circuit used for the generation of a quasi-linear signal composed of the most linear fragments of phase-shifted sinusoidal signals [7]. Also, at the output of this circuit, a 4-bit digital code is obtained representing a section of the input range to which the current angle belongs. The second circuit is a novel and compact two-stage nonlinear ADC that linearizes and digitizes the quasi-linear signal providing very accurate information about the current angular position. The proposed linearization method allows simultaneous linearization of the OERs response signals and digitization of measurement results, which is not typical for previously mentioned techniques. It will be confirmed by the numerical results that the proposed method is comparable with, or even superior to cited techniques in terms of measurement accuracy.

2. DESIGN OF THE PROPOSED LINEARIZATION CIRCUIT

2.1. A 4-bit mixed analog-digital circuit

The sine and cosine voltage signals obtained at the output of the ORE are generated in response to the angular position changes in the range between 0° and 360°. As it is known, sine and cosine signals are very nonlinear, especially near the extremes where they exhibit almost undetectable voltage changes even at significant angular position changes. In other words, there are sections of the measurement range where the encoder sensitivity is extremely low and the measurement error is high. Using a 4-bit mixed analog-digital circuit [7], shown in Fig. 1, eleven analog signals can be obtained out of the encoder output signals. These analog signals are S_1, S_2,…, S_8, S_6+S_1, S_4+S_1 and S_6+S_4. The part of the mixed analog-digital circuit devoted to analog signals generation is composed of operational amplifiers and resistors, where resistors marked with R have the resistance of 1 kΩ, and resistors marked with R_1 have the resistance equal to $\sqrt{2}/2$ =0.707 kΩ. The last value can be obtained using a serial connection of two standard resistors of 680 Ω and 27 Ω, with 1% tolerance [7]. Analog signals S_1 to S_8 represent phase-shifted sine and cosine signals, as shown in Table 1. Also, signals S_1 to S_8 are brought to the inputs of a 16 to 1 analog multiplexer (MUX 16 to 1) which combines their fragments to create output quasi-linear signal $V_{QL}(x)$. The resulting quasi-linear signal is shown in Fig. 2 (bolded black line), and the fragments of signals S_1 to S_8 are also marked.

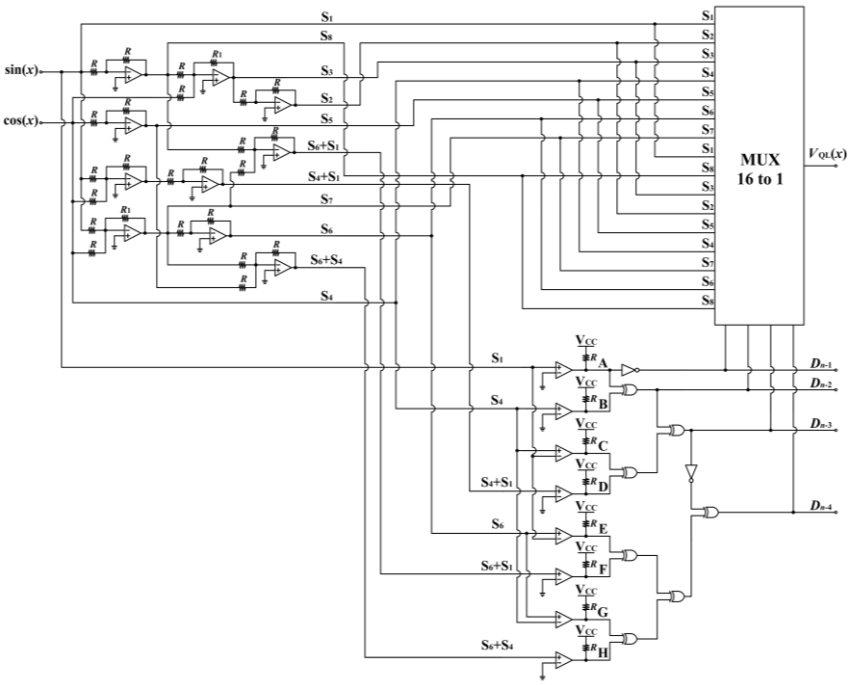

Fig. 1 A 4-bit mixed analog-digital circuit

As it can be noticed, the amplitude of the quasi-linear signal is equal to 0.383 V, when the amplitude of sinusoidal signals is 1 V. In general if the amplitude of sinusoidal voltages is equal to A, then the amplitude of the quasi-linear signal is equal to $\sin(45°)\cdot A=(0.383\cdot A)$ V.

Table 1 Analog and digital signals generated within the 4-bit mixed analog-digital circuit

Analog signals	Digital signals	Comparison
$S_1=\sin(x)$	A	$S_1>0$
$S_2=\cos(x+45°)=\frac{\sqrt{2}}{2}(\cos(x)-\sin(x))$	B	$S_4>0$
$S_3=-\cos(x+45°)=-\frac{\sqrt{2}}{2}(\cos(x)-\sin(x))$	C	$S_4>S_1$
$S_4=\cos(x)$	D	$S_4+S_1>0$
$S_5=-\cos(x)$	E	$S_6>S_1$
$S_6=\sin(x+45°)=\frac{\sqrt{2}}{2}(\cos(x)+\sin(x))$	F	$S_6+S_1>0$
$S_7=-\sin(x+45°)=-\frac{\sqrt{2}}{2}(\cos(x)+\sin(x))$	G	$S_6>S_4$
$S_8=-\sin(x)$	H	$S_6+S_4>0$

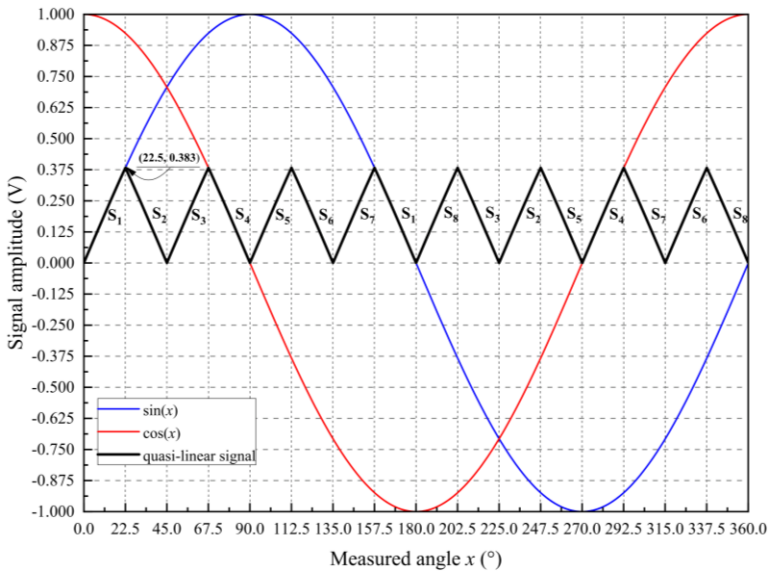

Fig. 2 The shape of the quasi-linear signal

To obtain a 4-bit digital code $D_{n-1}D_{n-2}D_{n-3}D_{n-4}$ (where n=4+2N is the overall resolution of the 4-bit mixed analog-digital circuit and the two-stage nonlinear ADC) representing a

section of the input range to which the measured angle belongs, eight digital signals are needed (A to H). Digital signals are obtained by performing the comparisons listed in the last column of Table 1.

The 4-bit digital code is obtained by conducting logical operations over digital signals A to H, as can be seen in the lower section of Fig. 1. In addition, the 4-bit digital code $D_{n-1}D_{n-2}D_{n-3}D_{n-4}$ is used for controlling the MUX 16 to 1. In precise, the multiplexer controlled by these bits selects one of 16 analog signals according to Table 2. As a result, the quasi-linear signal is obtained and brought to the input of the two-stage nonlinear ADC for additional linearization.

Table 2 Digital 4-bit representations for each of 16 sections of the input range

Sections	Signals	$D_{n-1}D_{n-2}D_{n-3}D_{n-4}$
0-22.5°	S_1	0000
22.5°-45°	S_2	0001
45°-67.5°	S_3	0010
67.5°-90°	S_4	0011
90°-112.5°	S_5	0100
112.5°-135°	S_6	0101
135°-157.5°	S_7	0110
157.5°-180°	S_1	0111
180°-202.5°	S_8	1000
202.5°-225°	S_3	1001
225°-247.5°	S_2	1010
247.5°-270°	S_5	1011
270°-292.5°	S_4	1100
292.5°-315°	S_7	1101
315°-337.5°	S_6	1110
337.5°-360°	S_8	1111

2.2. A two-stage nonlinear ADC of a novel compact design

For the linearization of a quasi-linear voltage signal, a two-stage nonlinear ADC of a compact design is proposed. In precise, it is a two-stage piecewise-linear ADC which is realized using one flash ADC in both conversion stages [8-11]. At the same time, the architecture of the flash ADC is modified so that the number of employed comparators is reduced and equal to the flash ADC resolution. The linearization is performed by the first-stage ADC with a transfer characteristic that is a piecewise-linear approximation of a function inverse to the voltage $V_{QL}(x)$. From Fig. 2 it can be observed that the voltage $V_{QL}(x)$ is sine shaped in each of 16 sections (each 22.5° wide) of the input range. Therefore, the first-stage ADC performs linearization of the function $\sin(x)$ by having the transfer characteristic that is the piecewise-linear approximation of a function $\arcsin(x)$. The linearization of the quasi-linear signal is performed within one section of the input range, while the information about the current section is provided with the 4-bit digital code obtained using the 4-bit mixed analog-digital circuit. On the other hand, the second-stage ADC does not perform linearization, but it improves measurement accuracy by increasing the overall resolution.

By employing a special sequential design of the flash ADC, a 2*N*-bit resolution of the two-stage nonlinear ADC is achieved using only *N* comparators [12, 13]. In the conventional flash ADC design, 2^N-1 comparators are employed [14], and in the two-stage nonlinear ADC with two flash ADCs of the same *N*-bit resolution, $2\cdot(2^N\text{-}1)$ comparators are used. There are cases when the first and the second conversion stage are of different resolutions, i.e. $N_1 \neq N_2$, when the comparator count equals $2^{N1}\text{-}1+2^{N2}\text{-}1$. However, in the proposed design of the two-stage nonlinear ADC, both conversion stages are performed using one flash ADC with two different resistive ladder networks (see Fig. 3). For the specific case, the resolution of the flash ADC is $N=4$ and only 4 comparators are used. The resistive ladder network used in the first stage is composed of mutually different resistors R_1-R_{16} that are setting the break-point voltages V_1-V_{15} as reference voltages for the comparators in the first conversion stage [7-11, 13, 15, 16]. These voltages are nonuniformly distributed within the input range of the first-stage ADC, which spans from 0 V to $V_{REF}=V_{max}=(0.383\cdot A)$ V. The break-point voltages V_i can be calculated as $\sin(i\cdot 2^{-N}\cdot 45°)$, where $i=1,\ldots, 2^N\text{-}1$. At the output of the first conversion stage, a 4-bit digital code is obtained ($D'_3D'_2D'_1D'_0$) representing a non-uniform segment (between two consecutive break-point voltages) to which the input sample V_{in} belongs. Also, the lower and higher boundary V_{jL} and V_{jH} ($j=1, 2,\ldots, 2^N$) of the current non-uniform segment, respectively, are determined with the help of two analog multiplexers 16 to 1 controlled by the bits ($D'_3D'_2D'_1D'_0$). The voltages V_{jL} and V_{jH} also represent the boundaries of the input range for the second conversion stage.

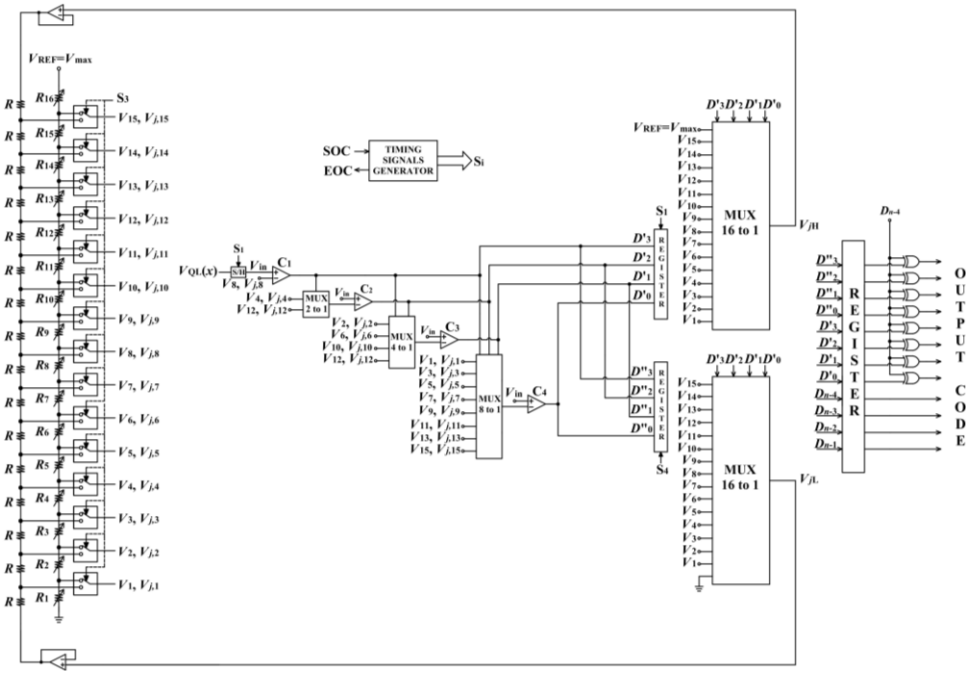

Fig. 3 An 8-bit two-stage nonlinear ADC of a compact design

The second resistive ladder network, consisting of resistors of mutually equal resistances R, is used during the second 4-bit conversion stage to set uniform reference voltages for the comparators. The reference voltages, uniformly distributed within the segment boundaries $V_{j\mathrm{L}}$ and $V_{j\mathrm{H}}$, can be expressed as follows:

$$V_{j,k} = V_{j\mathrm{L}} + k \cdot \frac{V_{j\mathrm{H}} - V_{j\mathrm{L}}}{2^N},\ j=1,...,2^N,\ k=1,...,2^N-1, \tag{1}$$

where j represents the non-uniform segment ordinal number, and k represents the ordinal number of a uniform reference voltage within the j^{th} segment. These voltages are brought to comparators which then determine the position of the current input sample within the second stage input range and represents it with a 4-bit digital code ($D''_3D''_2D''_1D''_0$). The second conversion stage is uniform (linear), it reduces the quantization noise generated during the first stage of conversion and increases the measurement resolution and accuracy.

As already mentioned, the quasi-linear signal has the shape of sin(x) function in each section of the input range, (see Fig.2.) but its slope varies, i.e. it is negative in even segments. To obtain a linear and monotonically rising transfer characteristic of the whole measurement system the inversion of bits ($D'_3D'_2D'_1D'_0D''_3D''_2D''_1D''_0$) is needed for even segments [10, 15]. The inversion is performed using XOR circuits and the bit $D_{n\text{-}4}$, as shown in Fig.3.

3. Simulations, Numerical Results and Discussions

This section of the paper is devoted to the evaluation of the proposed linearization concept by conducting two simulations, one using National Instruments (NI) Multisim software, and the second using NI LabVIEW software. The Multisim simulation proves that the developed 4-bit mixed analog-digital circuit generates a quasi-linear signal, while the LabVIEW simulation confirms the proper functioning of the 4-bit mixed analog-digital circuit and the two-stage nonlinear ADC. In precise, the program created in LabVIEW, i.e. virtual instrument (VI), gives information about the transfer characteristic of the whole measurement system. Additionally, it provides the assessment of the effectiveness of the encoder nonlinearity compensation based on the calculated absolute measurement error and relative nonlinearity error. Mentioned simulations are important in evaluating whether the proposed linearization circuit works as expected, i.e. whether it performs the nonlinearity compensation as effectively as planned. In other words, the simulation is significant in preventing possible production costs and time loss if there is an error in the circuit design. In Fig. 4 the Multisim simulation of the 4-bit mixed analog-digital circuit is shown and, as it can be noticed, all components employed are real and commercially available. In other words, the Multisim results can be considered experimental since the simulation is carried out by employing components with real characteristics. In Fig. 5 is given a digital Tektronix oscilloscope screen appearance with the quasi-linear signal (purple coloured) of the amplitude of (0.383·A) V, where A=5 V represents the amplitude of sine (yellow coloured) and cosine (blue coloured) signal. The obtained waveforms are in excellent agreement with theoretical assumptions, meaning that the real circuit will work as expected.

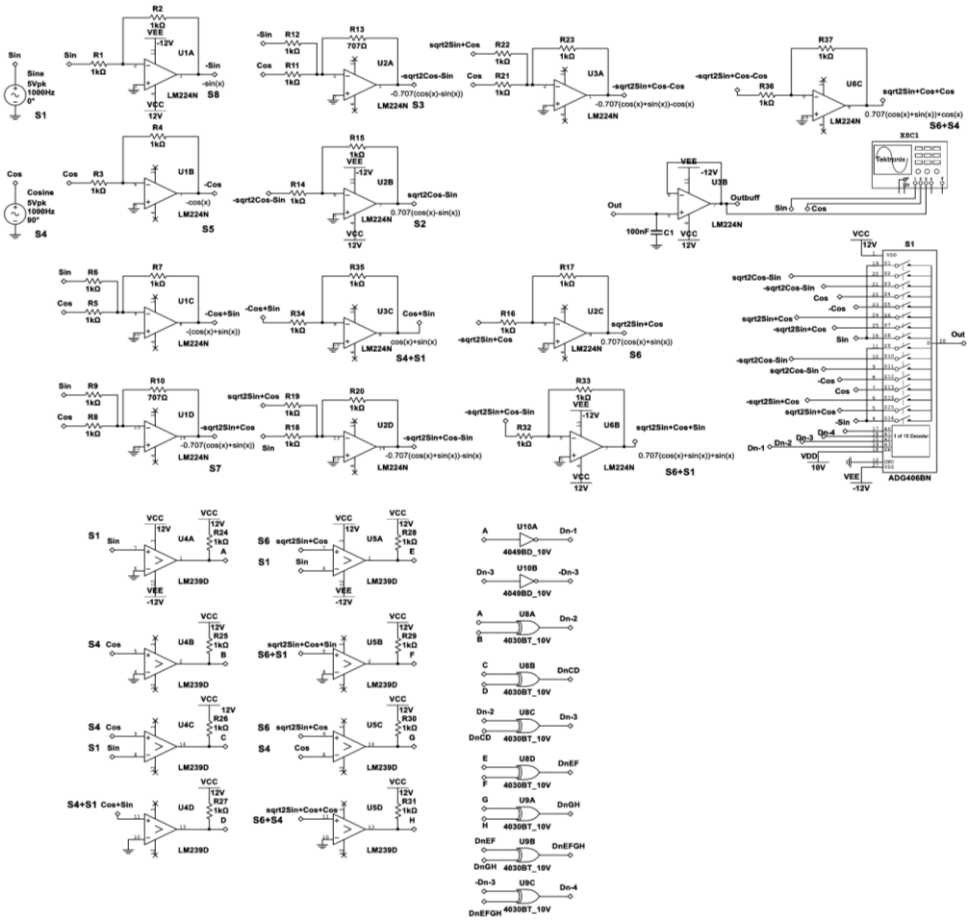

Fig. 4 A Multisim simulation of the 4-bit mixed analog-digital circuit

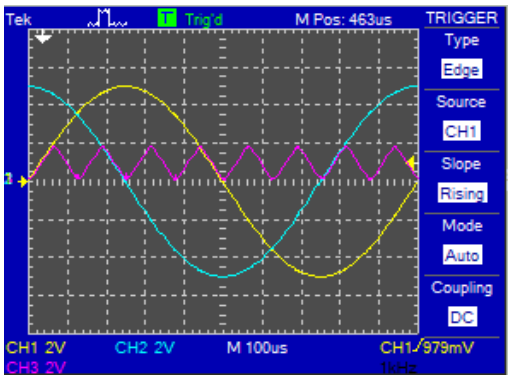

Fig. 5 Sine (CH1), cosine (CH2) and quasi-linear signal (CH3) displayed using Tektronix oscilloscope

The performances of the proposed linearization circuit can be evaluated through comparison with its previous version [10] consisted of a 3-bit mixed analog-digital circuit and a two-stage nonlinear ADC of a special design. The two-stage nonlinear ADC from [10] also employs one flash ADC in both conversion stages, but the number of comparators used in the flash ADC design is equal to 2^N-1, i.e. the employed flash ADC is of a conventional design. In other words, the resolution of $2N$ bits is achieved using 2^N-1 comparators. However, in the newly proposed design of the $2N$-bit two-stage nonlinear ADC, only N comparators are used. In the continuation are given expressions for the numbers of employed comparators n_c, n_s and n_p:

$$n_c = (2^N - 1) + (2^N - 1) = 2 \cdot (2^N - 1), \tag{2}$$

$$n_s = 2^N - 1, \tag{3}$$

$$n_p = N, \tag{4}$$

where n_c represents the number of employed comparators in the classic two-stage nonlinear ADC composed of two N-bit flash ADCs of the conventional design [16], n_s is the number of employed comparators in the two-stage nonlinear ADC containing one N-bit flash ADC of the conventional design [10], and n_p is the number of comparators employed in the newly proposed design of the two-stage nonlinear ADC. The values of the discussed comparator counts are given in Table 3 for different values of resolution $2N$ of the two-stage nonlinear ADC. By observing the obtained comparator counts one can conclude that the newly proposed design of the two-stage nonlinear ADC is the most compact and in this manner the most cost-effective in terms of power consumption, dimensions and production costs in comparison to other discussed designs.

Table 3 Comparator counts for three discussed designs of the two-stage nonlinear ADC

Resolution	Comparator count		
$2N$ [bit]	n_c	n_s	n_p
6	14	7	3
8	30	15	4
10	62	31	5
12	126	63	6
14	254	127	7
16	510	255	8
18	1022	511	9
20	2046	1023	10

In addition to the number of comparators employed, the newly proposed linearization circuit with the 4-bit mixed analog-digital circuit and a $2N$-bit two-stage nonlinear ADC is compared by the values of maximal absolute error Δx_{max} [rad] and relative nonlinearity error NE [%] with the linearization circuit proposed in [10]. These parameters are expressed in the following manner:

$$\Delta x_{max} = \left| x_{out} - x_{in} \right|_{max}, \tag{5}$$

$$NE = \frac{\Delta x_{\max}}{2\pi} \cdot 100\%, \tag{6}$$

where x_{in} [rad] is the input angle, x_{out} [rad] is the measured angle, while 2π [rad] represents the full measurement range. The error values are calculated using LabVIEW VI whose front panel is presented in Fig. 6. The designed VI determines the first four bits $D_{n-1}D_{n-2}D_{n-3}D_{n-4}$ using a special subVI. Also, the first and the second stage of conversion are performed (N_1=N_2=N=3 bits in Fig. 6) and the complete digital code is obtained. Values of the nonuniform break-point voltages are determined during the first stage of conversion. The VI can determine the measured angle value for a specific input angle (switch in the position One calculation) or can display the transfer characteristic and give the absolute error diagram for the whole measurement range (switch in the position Graphics). The obtained numerical results, i.e. parameters $\Delta x_{\max}$ and NE are listed in Table 4 together with parameters obtained using the linearization circuit proposed in [10]. For the same 2N-bit resolution, the newly proposed linearization method achieves two times lower maximal absolute error and relative nonlinearity error in comparison to the method proposed in [10]. This advantage follows from the higher resolution of the mixed analog-digital circuit. On the other hand, the newly proposed method utilizes a significantly lower number of comparators, which makes it more convenient for applications with constrained power consumption.

The proposed method is additionally compared with other methods previously proposed in the literature [3-6] regarding the measurement accuracy, i.e. the residual absolute measurement error after linearization. The error values are given in Table 5, and as it can be noticed, the maximal absolute measurement error after the application of the proposed method is lower than in all other cases, meaning that the proposed linearization method provides the highest accuracy.

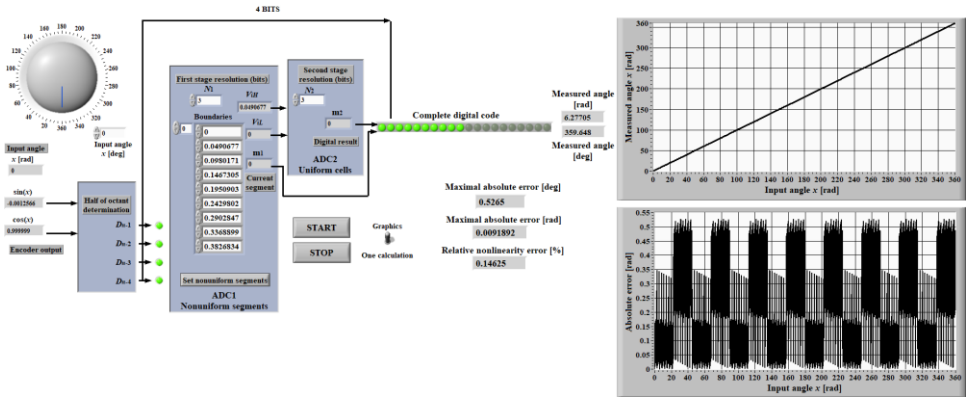

Fig. 6 The front panel of a VI programmed to simulate the whole measurement system

Table 4 Numerical results obtained using the linearization method proposed in [10] and the newly proposed method

Resolution $2N$ [bit]	Design				
	The method proposed in [10]		The newly proposed method		
	Maximal absolute error [rad]	Relative nonlinearity error [%]	Maximal absolute error [rad]	Maximal absolute error [°]	Relative nonlinearity error [%]
6	0.0194386	0.309375	0.0091892	0.5265	0.14625
8	0.0048351	0.0769531	0.0023096	0.132328	0.0367578
10	0.0011953	0.0190234	0.0005805	0.0332578	0.0092383
12	0.0002985	0.004751	0.0001437	0.0082354	0.0022876
14	$7.55\cdot10^{-5}$	0.0012012	$3.63\cdot10^{-5}$	0.0020786	0.0005774
16	$1.84\cdot10^{-5}$	0.000293	$9.1\cdot10^{-6}$	0.0005186	0.000144
18	$4.6\cdot10^{-6}$	$7.37\cdot10^{-5}$	$2.3\cdot10^{-6}$	0.0001296	$3.6\cdot10^{-5}$
20	$1.2\cdot10^{-6}$	$1.88\cdot10^{-5}$	$6\cdot10^{-7}$	$3.23\cdot10^{-5}$	$9\cdot10^{-6}$

Table 5 A comparison between different linearization methods regarding the maximal absolute error

Linearization method	from [4]	from [3]	from [5]	from [6]	newly proposed
Maximal absolute error [°]	0.3°	0.05°	0.014°	$6\cdot10^{-4}$°	$3.23\cdot10^{-5}$

4. CONCLUSIONS

A linearization method used for optical rotary encoders and other sinusoidal encoders which generate sine and cosine signals in response to angular position changes has been proposed. The proposed method is based on the application of a 4-bit mixed analog-digital circuit and a novel and compact two-stage nonlinear ADC. The mixed analog-digital circuit generates a quasi-linear signal that is further linearized in the two-stage nonlinear ADC, which performs both conversion stages using one flash ADC. The employed N-bit flash ADC uses only N comparators, meaning that for the realization of the $2N$-bit two-stage nonlinear ADC only N comparators are needed. For example, a 20-bit two-stage nonlinear ADC composed of two flash ADCs of the conventional design employs 2046 comparators, while in the proposed design of the 20-bit two-stage nonlinear ADC only 10 comparators are used. In this manner, a compact and cost-effective architecture of the two-stage nonlinear ADC has been obtained. What is even more significant is that the proposed linearization method provides a substantial nonlinearity reduction witnessed by a very high measurement accuracy of $6\cdot10^{-7}$ [rad], i.e. $3.23\cdot10^{-5}$° in the 360° range.

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