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A COMPACT AND COST-EFFECTIVE LINEARIZATION CIRCUIT USED FOR ANGULAR POSITION SENSORS

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Abstract. *In this paper a compact and cost-effective design of a linearization circuit used for angular position sensors is proposed. The proposed circuit is composed of two sections, wherein the first section performs pseudo-linearization of the sensor output signal, while in the second section reduction of the residual signal nonlinearity and the signal digitalization are performed. In particular, the second section of the proposed circuit represents a two-stage piecewise linear analog-to-digital converter. Compact design of the two-stage piecewise linear analog-to-digital converter provides cost-effectiveness of the linearization circuit in terms of power consumption. In particular, these benefits are achieved by excluding power consuming components such as comparators since just one flash analog-to-digital converter performs both conversion stages. The obtained numerical results prove the efficiency of the linearization circuit we are proposing since the maximal absolute error is $1.84078 \cdot 10^{-5}$ [rad] (0.001^{o}) when the 16-bit two-stage piecewise linear analog-to-digital converter is employed.*

Key words: *angular position, comparator count, linearization, pseudo-linearization, sine/cosine signals processing*

1. INTRODUCTION

The application range of angular position sensors is wide and includes determination of angular velocity and angular position in a variety of systems such as industrial robots, radars, antennas, automobiles, aircrafts, machine tools, computer mice, etc. This group of sensors includes different types of magnetic sensors, optical rotary encoders and resolvers [1, 2], which convert angular position into an electrical signal. In particular, the aforementioned sensors generate sine and/or cosine voltage signals in response to the angular position changes, which means that the output voltage is in nonlinear relation to the input angle. Due to nonlinear

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shape of the sine signal, equal changes of the measured angle at the sensor input lead to unequal voltage changes at the sensor output. Variations of the sensor output voltage can be sometimes so small that their detection becomes very difficult, which on the other hand causes low measurement accuracy. In order to increase the measurement accuracy, linear dependence between sensor output voltage and the angular position needs to be provided, i.e. sensor linearization has to be performed.

Sensor linearization is an important process that has to be performed to provide a satisfying accuracy of the measurement system used solely or as a part of, for example, an automatic control system. Nonlinear dependence of a sensor output on its input, i.e. nonlinear transfer function of the sensor, is unwanted due to many reasons, but for the automatic control systems the presence of a nonlinear sensor in the control loop may cause certain anomalies, like excessive oscillations [3]. Also, when the sensor is a part of a larger control system, its nonlinear transfer function makes the design and analysis of the whole system more difficult.

Led by the goal to perform the linearization of the angular position sensors and to overcome disadvantages and combine advantages of the conventional analog and digital linearization methods, in this paper a compact and cost-effective design of a special linearization circuit is proposed. The proposed linearization circuit first performs pre-processing of the sensor output signals (sine and/or cosine signals) towards obtaining pseudo-linear signal [4, 5] that is further linearized and simultaneously digitized by the two-stage piecewise linear analog-to-digital converter (two-stage PWL ADC) [5-8]. The pseudo-linear signal is obtained by combining the most linear parts of sine and cosine signals, i.e. by avoiding the most nonlinear parts of the signals (parts that are close to the signals' extremes). In papers [4, 9-11] several angular position determination methods, based on the resolver application, were proposed. The authors of the papers [4, 9-11] developed special analog circuits in order to provide linear dependence of the resolver output on its input. Their solutions do not include analog-to-digital converter and in this manner signal digitalization. In addition, the information about the quadrant position ($\pi/2$ [rad] in width) of the input angle is needed to obtain the complete information about the angle value. In this paper pseudo-linear signal is obtained by using the method similar to the one proposed in [4], wherein in this paper the authors suggest determination of the input angle octant position (half of the quadrant). As a result, measurement resolution is increased and in this manner measurement accuracy is increased as well.

The linearization circuit proposed in this paper represents an improvement of the linearization circuit proposed in [5] in terms of higher dimensional compactness and lower energy consumption. Also, the circuit proposed in this paper provides higher measurement accuracy (lower measurement error) in comparison to the corresponding result obtained by the circuit proposed in [5]. The first section of the linearization circuit proposed in this paper is equivalent to the corresponding section of the circuit proposed in [5], i.e. the generation of the pseudo-linear signal is performed in the same manner in both solutions. However, the difference between these two solutions is reflected in the realization of the two-stage PWL ADC. Specifically, both conversion stages of the two-stage PWL ADC proposed in this paper, in contrast to the circuit presented in the paper [5], are performed using one flash ADC that employs two different resistor ladder networks. Hence, the compactness and the cost-effectiveness of the solution proposed in this paper are achieved by excluding the comparators that are needed when two flash ADCs are used.

The design of the two-stage PWL ADC used in this paper is based on the design presented in paper [8]. The main principles of the linearization process performed by the two-stage PWL ADC used in this paper are the same as those applied in papers [5-8], i.e. the linearization of the pseudo-linear signal (or as in papers [6-8] sensor output signal directly) is performed in the first stage of analog-to-digital conversion, while the second stage removes the quantization error introduced in the first conversion stage. The linearization is performed by the first stage piecewise linear flash ADC with the transfer function that is the piecewise linear approximation of a function inverse to the functional dependence of the pseudo-linear voltage signal on the measured angle. More details about the design of the employed two-stage PWL ADC are given in the following section of the paper.

To recapitulate, in this paper the angular position determination method based on pre-processing of the sensor output signals towards obtaining the pseudo-linear signal and its additional linearization and digitalization conducted by the two-stage PWL ADC is proposed. More precisely, two different linearization circuits are employed. The first, so called circuit of a special purpose (can be used only with the sensors with sine/cosine output signals) is used for the input angle octant position detection and pseudo-linear signal generation. The second linearization circuit is of a general purpose (can be used with all sensor types), i.e. it is the two-stage PWL ADC. Combining the benefits of these two linearization circuits measurement errors are significantly reduced, while the measurement resolution and accuracy are increased in comparison to cases where each of these linearization circuits are used separately.

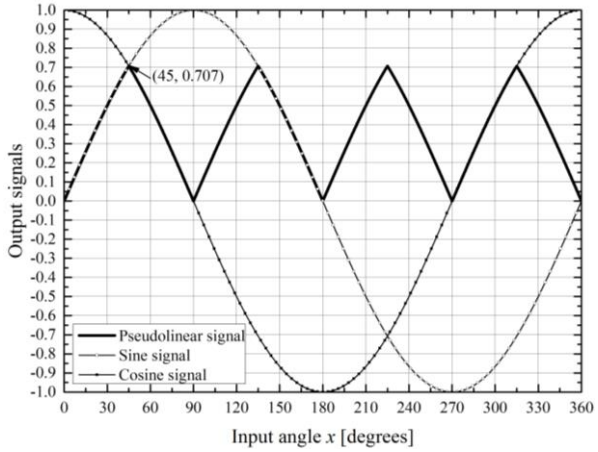
The rest of the paper is organized as follows. The circuit used for the pseudo-linear signal generation is described in the first subsection of the Section 2. In continuation of the Section 2 a detailed description of the employed two-stage PWL ADC is given. The simulation of the considered measurement system is performed by using the LabVIEW software and the numerical results are in the same manner obtained. The third section of the paper is devoted to the presentation of the numerical results, while the conclusions drawn after the analysis of the numerical results are given in the final section of the paper.

2. THE PROPOSED DESIGN OF THE LINEARIZATION CIRCUIT

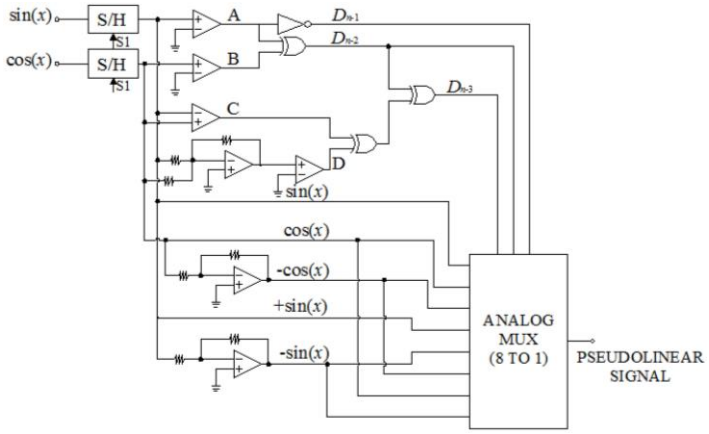
In this paper an angular positon sensor linearization circuit, consisted of two sections, is proposed. The first linearization section represents the circuit used for generation of the pseudo-linear signal by combining sine and cosine signals from the sensor output, and the second linearization section represents the two-stage PWL ADC realized as one flash ADC with two different resistor ladder networks. The two-stage PWL ADC is used for simultaneous linearization of the pseudo-linear signal and digitalization of measurement results. Below are given detailed descriptions of both linearization sections.

2.1. Circuit used for the pseudo-linear signal generation

The first, so called pre-processing step is performed by using the circuit designed for detection of the octant position of the input angle (one octant is $\pi/4$ [rad] wide) and generation of the pseudo-linear signal. This signal is obtained by combining the segments of sine and cosine signals that are characterized with a satisfying linearity (see Fig. 1 a)). More precisely, the bolded line from Fig. 1 a) represents the pseudo-linear signal composed of eight segments (more linear parts of sine and cosine signals) and with the amplitude of 0.707 [V], if the amplitude of the sine and cosine signals is 1 [V].



a)



b)

Fig. 1 a) Pseudo-linear signal composed of sine and cosine signals' segments, b) Circuit used for the pseudo-linear signal generation

In general, the amplitude of the pseudo-linear signal is $0.707 \cdot A$ [V], where A represents the amplitude of the sine and cosine signals. By observing the Fig. 1 a) one can conclude that the amplitude of the pseudo-linear signal follows from the fact that the sine and cosine signal have the same value for the angles of $(2k+1) \cdot \pi/4$ [rad], k=0, 1, 2,…. Since the pseudo-linear signal is composed of eight segments (octants) three bits are needed for coding of the octant to which the input angle belongs. These bits are generated using the circuit presented in the Fig. 1 b), and marked with D_{n-1}, D_{n-2} and D_{n-3} (n represents the overall resolution of the proposed linearization circuit). These bits are used to control the output of a multiplexer 8 to 1, and at the same time represent the most significant bits of the final digital code.

The pseudo-linear signal represents a combination of the segments of the following signals: sin(x), cos(x), -sin(x) and -cos(x), and which of them is selected by the multiplexer depends on the octant where the input angle belongs.

The sine and cosine output signals are brought to the inputs of the comparators for comparison with the zero reference voltage and for their mutual comparison. In Table 1 are given logic values from the comparators' outputs A, B, C and D, the bits D_{n-1}, D_{n-2} and D_{n-3} and the signal that is brought to the input of the two-stage PWL ADC for the corresponding input angle octant position (the last column). For each of these eight octants there is just one signal (sin(x), cos(x), -sin(x) or -cos(x)) that has positive value and shows good linearity, and it is selected by the multiplexer that is controlled by the bits D_{n-1}, D_{n-2} and D_{n-3}. This means that the second linearization step is always performed within one octant.

Table 1 Signals at different points of the circuit used for the pseudo-linear signal generation

Input angle x[rad]	A sin(x)>0	B cos(x)>0	C cos(x)>sin(x)	D sin(x)+cos(x)>0	D_{n-1}	D_{n-2}	D_{n-3}	Signal
0-π/4	1	1	1	1	0	0	0	+sin(x)
π/4-π/2	1	1	0	1	0	0	1	+cos(x)
π/2-3π/4	1	0	0	1	0	1	0	-cos(x)
3π/4-π	1	0	0	0	0	1	1	+sin(x)
π-5π/4	0	0	0	0	1	0	0	-sin(x)
5π/4-6π/4	0	0	1	0	1	0	1	-cos(x)
6π/4-7π/4	0	1	1	0	1	1	0	+cos(x)
7π/4-2π	0	1	1	1	1	1	1	-sin(x)

2.2. Compact and cost-effective design of the two-stage PWL ADC

With the linearization of the pseudo-linear signal by using the two-stage PWL ADC simultaneous digitalization of the measurement results is performed. Although the analog-to-digital conversion is performed in two stages, linearization is performed only in the first stage. The working principle of two-stage PWL ADC is based on the fact that the transfer function of the first stage flash ADC is the piecewise linear approximation of a function that is inverse to the functional dependence of the pseudo-linear signal on the input angle. This means that the transfer function of the first stage ADC is composed of linear segments of unequal width. In addition, these linear segments are bounded by the points called the break voltages [5-8], which at the same time represent the reference voltages of the comparators that are composing the first stage piecewise linear flash ADC. These voltages are derived from the reference voltage V_{ref} that is applied to the resistor ladder network composed of resistors that have different resistance values. The values of resistors need to be different since the break voltages are non-uniformly distributed between 0 and V_{ref}. The voltage V_{ref} is 0.707 [V].

However, in the second conversion stage the linearization is not performed and the flash ADC utilizes the resistor ladder network composed of resistors with mutually equal resistances. Differences between the first and the second conversion stage are: the first stage flash ADC input range is spanning from 0 to V_{ref}, while the input range of the second stage define the break voltages determined in the first conversion stage; and, in the first stage reference voltages are non-uniformly distributed between 0 to V_{ref}, while in the second

conversion stage the reference voltages of the comparators are uniformly distributed between two break voltages. Although the linearization is not performed in the second conversion stage, the second stage of conversion eliminates the quantization error introduced in the first conversion stage, which improves the accuracy of the final measurement result.

The two-stage PWL ADC design proposed in [8] is in this paper adapted for the linearization of the optical rotary encoder. The employed two-stage PWL ADC is shown in the Fig. 2 and has two stages of analog-to-digital conversion both of the same resolution, since both conversion stages are performed with one flash ADC. The overall resolution of the linearization circuit is n=3+2N, where 3 represents the bits $D_{n\text{-}1}$, $D_{n\text{-}2}$ and $D_{n\text{-}3}$ and N represents the resolution of the flash ADC.

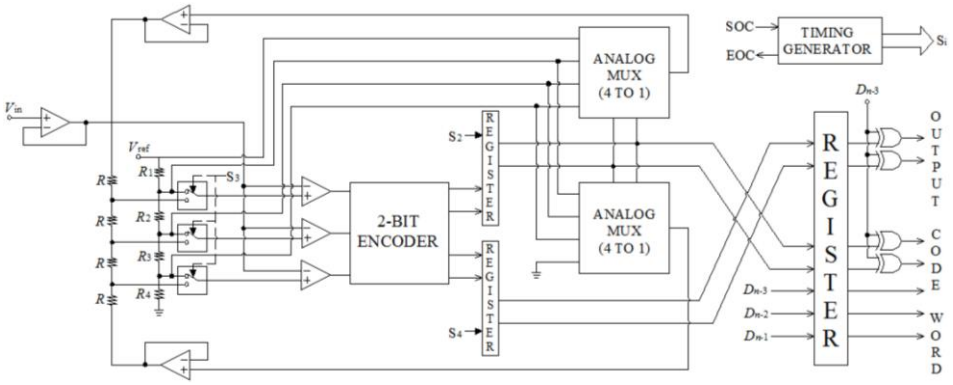


Fig. 2 The 4-bit two-stage PWL ADC used for pseudo-linear signal linearization

In the circuit shown in Fig. 2 in both conversion stages 2-bit flash ADC (N=2) is used and in accordance with the design of the conventional flash ADC three comparators are employed [1, 2]. A sample of the pseudo-linear signal V_{in} and the reference voltages are brought to the inputs of the comparators for their mutual comparison. As already mentioned, the reference voltages are provided by the resistor network composed of resistors with different resistances (R_1, R_2, R_3 and R_4), since the reference voltages are non-uniformly distributed between 0 and V_{ref}. The values of the resistors are selected to adjust the comparators' reference voltages to correspond to the break voltages that split the flash ADC input range into the segments of unequal width. In general, the values of the resistors need to be selected in advance to provide the linearization of a specific nonlinear signal by using the flash ADC.

For the particular case, the signal that is linearized is sin(x) for the range from 0 to π/4, which means that the transfer function of the first stage piecewise linear flash ADC should be the piecewise linear approximation of the function arcsin(x), where x is the input angle. Since the signal slope varies while its shape remains the same through octants (Fig. 1 a)), it is enough to perform the linearization of the signal sin(x) while having the information about the octant position of the input angle (defined by the bits $D_{n\text{-}1}$, $D_{n\text{-}2}$ and $D_{n\text{-}3}$). However, in the second, fourth, sixth and eighth octant the slope of the pseudo-linear signal is negative, i.e. its amplitude decreases while the value of the input angle increases. Therefore, in order to obtain monotonically rising transfer function of the whole system, the inversion of the least significant bits D_0-$D_{n\text{-}4}$ needs to be performed. The inversion is performed by bringing the bits D_0-$D_{n\text{-}4}$ together with $D_{n\text{-}3}$ to XOR circuits (see Fig. 2).

The break voltages are calculated for angles that are obtained by dividing the sensor input range from 0 to $\pi/4$ on 2^2 equal segments (from 0 to $\pi/16$, from $\pi/16$ to $2\pi/16$, from $2\pi/16$ to $3\pi/16$ and from $3\pi/16$ to $\pi/4$). However, the break voltages are calculated as the sine function only for the angles of $\pi/16$, $2\pi/16$ and $3\pi/16$. The angles of 0 and $\pi/4$ are the boundaries of the sensor input range and for them the break voltages are not calculated.

The result of the first conversion stage are two bits, which are stored in the register using the strobe signal S2, and used to control two multiplexers 4 to 1. These multiplexers have the task to select the lower and upper bound of the segment to which the sample of the pseudo-linear signal belongs. At the same time, the multiplexers' output voltages are brought to the input of the 2-bit flash ADC as the boundaries of its input range. This is the beginning of the second conversion stage. Also, the switches that are controlled by the strobe signal S3 are closed and replace the first resistor network with another ladder network composed of four equal resistors marked with *R*. These resistors generate the comparators' reference voltages that are uniformly distributed throughout the range defined by the break voltages determined in the first conversion stage. The reference voltages in the second stage split the input range on four uniform cells, because the second conversion stage also has 2-bit resolution. The result of the second conversion stage represents two the least significant bits that are stored in the register by using the strobe signal S4. Together with bits D_{n-1}, D_{n-2} and D_{n-3} and the bits determined in the first stage of conversion, these last two bits represent the final digital output code that is in linear relation with the input angle.

3. Simulation Results and Discussions

For deriving the numerical results that will prove the efficiency of the linearization circuit we propose we have used the LabVIEW software. In the Fig. 3 the front panel of the virtual instrument that simulates the circuit for pseudo-linear signal generation and determination of the input angle octant position and the 4-bit two-stage PWL ADC circuit is presented. The simulation includes determination of the sine and cosine values of the input angle, determination of the most significant bits D_{n-1}, D_{n-2} and D_{n-3}, detection of the segment in the first stage of analog-to-digital conversion, determination of the segment boundaries (break voltages) and at the end determination of the uniform cell, within the segment boundaries to which the pseudo-linear voltage belongs. In the Fig. 3 the simulation of the measurement system for the input angle of 60° or $\pi/3$ [rad] is shown. This angle belongs to the second octant (see Table 1), and because the virtual instrument starts counting the octants from 0 this octant is marked with 1 and coded with 001. Since in this octant the pseudo-linear signal is represented with $\cos(x)$ (see Table 1), the voltage value is 0.5 [V]. In the second octant the inversion of bits D_0-D_{n-4} is needed. The voltage of 0.5 [V] belongs to the third segment (in the Fig. 3 the segment value is 2 because the counting starts from 0) bounded by the voltages of 0.382683 and 0.55557 [V]. This segment is coded with 10 (the segment 0 is coded with 00), but after inversion these bits become 01.

Since the two-stage PWL ADC has 2 bits of resolution in each conversion stage, the number of uniform cells in one segment is 4, and for the angle of $\pi/3$ [rad] $\cos(\pi/3)$ belongs to the cell marked with 3 and coded with 11 (the cell 0 is coded with 00) and after inversion these bits become 00. The final digital output is 0010100 which can be seen on the right side of the Fig. 3. After conversion to the analog domain the value of the

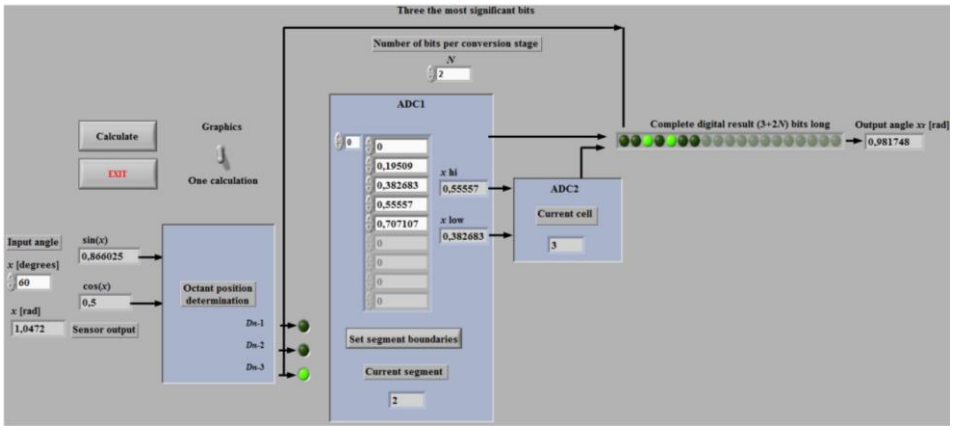


Fig. 3 Front panel of the virtual instrument that simulates the circuit used for angular position sensor linearization

angle, i.e. the measured value is 0.981748 [rad]. The difference between the accurate value of 1.0472 [rad] and the measured value is great due to low resolution of the two-stage PWL ADC, which is only for 4 bits. This resolution is not used in practice, but it was useful as an example of how the simulation works.

Table 2 The number of employed comparators in relation to the resolution and design of the two-stage PWL ADC

$2N$ [bit]	8			12				16				
Design	2x4	4+4	2+6	2x6	6+6	4+8	2+10	2x8	8+8	6+10	4+12	2+14
Comparator count	15	30	66	63	126	270	1026	255	510	1086	4110	16386

Let us now discuss the influence of the two-stage PWL ADC resolution on the circuit compactness and energy consumption. The circuit compactness is higher and the energy consumption is lower if lower number of comparators is employed. In Table 2 an overview of the comparator count in relation to the design of the two-stage PWL ADC and its resolution is given. The cases with the resolutions of 8, 12, and 16 bits are examined. Each of these resolutions can be obtained using one of two different two-stage PWL ADC designs. The columns that are in Table 2 labeled as the product of number 2 and the resolution of 4, 6 and 8 bits refer to the two-stage PWL ADC design where one flash ADC performs both conversion stages. The other columns refer to the realization with two flash ADCs of the same or different resolutions, i.e. like in [5, 7]. By observing the results that are given in Table 2 one can easily conclude that the proposed two-stage PWL ADC design (2x4, 2x6 and 2x8) employs lower number of comparators in comparison to the two-stage PWL ADC of the same total resolution employing two flash ADCs. The lack of the design with two flash ADCs is that the resolution increase of one flash ADC significantly increases the number of employed comparators although the total resolution remained unchanged (by decreasing the resolution of another flash ADC, see columns 8+8, 6+10, 4+12, 2+14). In this manner we have shown that the design used in this paper is more compact, i.e. it takes less space on the integrated circuit board and provides higher cost-effectiveness in terms of energy consumption.

However, the primer advantage of the linearization circuit we propose in this paper is reflected in the measurement accuracy increase. To assess the effect of the linearization on the accuracy of the angular position measurement we have determined the values of the absolute and the relative measurement error by using the following expressions:

$$\textit{absolute error}\ [\text{rad}] = \left| x_{\text{r}} - x \right|, \tag{1}$$

$$\textit{relative error}\ [\%] = \frac{\left| x_{\text{r}} - x \right|}{2\pi} \cdot 100\%, \tag{2}$$

wherein x represents the accurate value of the input angle, x_{r} represents the measured value of the input angle and 2π represents the full scale range of the measured angle. The maximal values of these errors in relation to the resolution of the two-stage PWL ADC are given in Table 3. The examined resolutions represent the integer multiples of number 2 because both conversion stages are performed by one flash ADC. It is clearly evident that the resolution increase leads to the significant reduction of the absolute and relative errors.

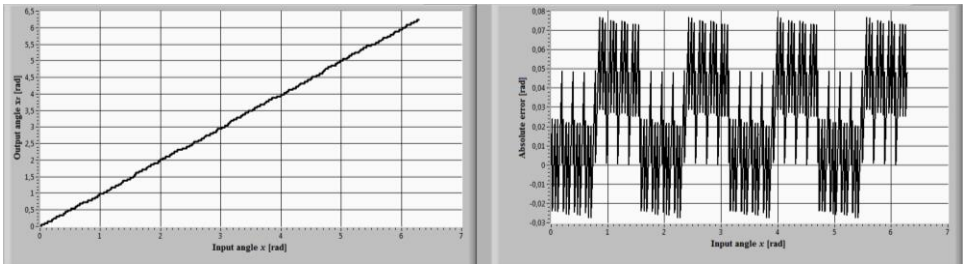
Table 3 Maximal absolute error [rad] and maximal relative error [%] in relation to the two-stage PWL ADC resolution

Resolution 2*N* [bit]	Maximal absolute error [rad]	Maximal relative error [%]
4	0.0766549	1.22
6	0.0194386	0.309375
8	0.00483511	0.0769531
10	0.00119528	0.0190234
12	0.000298513	0.00475098
14	$7.54719 \cdot 10^{-5}$	0.00120117
16	$1.84078 \cdot 10^{-5}$	0.000292969

By comparing the maximal absolute error obtained by using the linearization circuit with the 16-bit (2x8 bits) two-stage PWL ADC used in this paper with the corresponding value obtained by using the linearization circuit with the 16-bit (4+12 bits) two-stage PWL ADC proposed in paper [5], a significant difference is noticed. In particular, in our case, the maximal absolute error is $1.84078 \cdot 10^{-5}$ [rad] while the corresponding value from paper [5] is $3 \cdot 10^{-4}$ [rad], i.e. 16 times higher. This result is caused by the fact that the resolution of the first stage flash ADC used in this paper (8 bits) is greater than the resolution of the first stage flash ADC from [5] (4 bits), although the overall resolution is the same in both cases (16 bits). Since the first stage flash ADC performs the linearization, its greater resolution gives better results, i.e. lower maximal absolute error. Also, we have noticed that the same maximal absolute error achieved by the circuit that employs 16-bit two-stage PWL ADC used in [5] can be achieved with the circuit that employs 12-bit two-stage PWL ADC used in this paper.

In the Fig. 4 the transfer function of the whole system, i.e. the relation between output (measured) angle and input (accurate) angle and the graphical representations of the absolute error dependence on the measured angle are given for the cases when 4, 8, 12 and 16-bit two-stage PWL ADC is employed. From Fig. 4 it is easy to observe that the increase of the two-stage PWL ADC resolution produces smoother and more linear transfer functions and smaller absolute error values. Therefore, depending on the requirements

in terms of measurement accuracy and the maximal resolution, which is usually limited by the available space and permitted power consumption, a compromise solution can be found.



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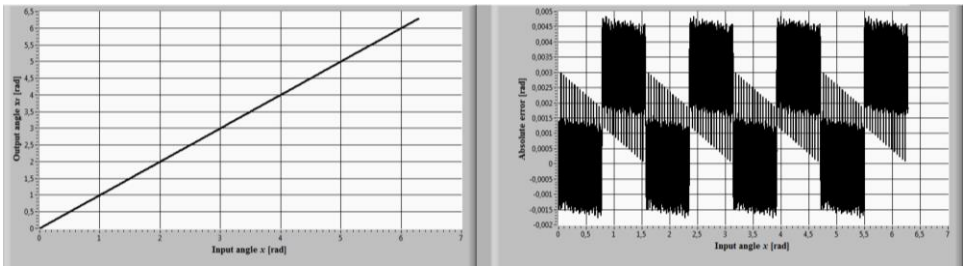

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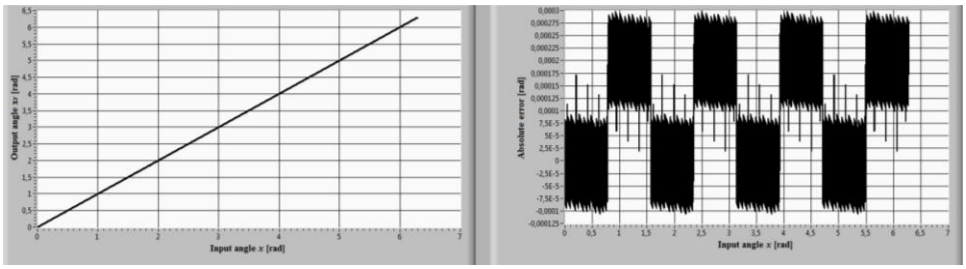

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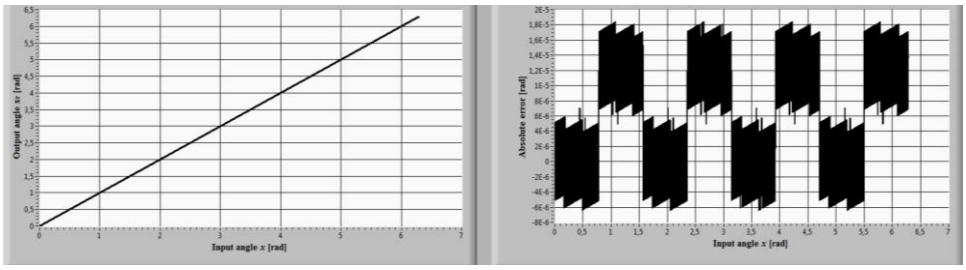

d)

Fig. 4 Transfer function of the whole system and the absolute error [rad] for the case when: a) $2N$=4 bits, b) $2N$=8 bits, c) $2N$=12 bits, d) $2N$=16 bits.

4. CONCLUSIONS

The linearization of angular position sensors that generate sine and cosine signal due to angular position changes has been the subject of the paper. More precisely, the compact design of the linearization circuit has been proposed in order to provide cost-effective linearization process. The proposed circuit is composed of two sections: the first section where the pseudo-linear signal is generated and the second section where the pseudo-linear signal further linearization and digitalization are performed. The second section is the two-stage PWL ADC with the compact design. The compactness of the two-stage PWL ADC design has been achieved by using one flash ADC that performs both conversion stages. This is possible since the flash ADC uses two different resistor ladder networks: one with mutually different resistors and one with mutually equal resistors. After completion of the first conversion stage the first resistor network is replaced with the second one. By using the proposed circuit design, lower number of power consuming comparators is employed, i.e. power consumption is significantly reduced. On the other hand, the results concerning the performance of the linearization circuit in terms of measurement accuracy also prove the circuit efficiency, i.e. the maximal absolute measurement error is reduced to the level of $1.84078 \cdot 10^{-5}$ [rad] when the 16-bit two-stage PWL ADC is employed. This result has proved that the goal to improve the angular position sensor accuracy, by eliminating sensor nonlinearity, has been achieved.

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