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ADAPTIVE COMPLEX FILTERS BASED TRANSMITTER IQ IMBALANCE REJECTION

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Abstract. *This paper presents an efficient method for compensation of frequency-dependent (FD) transmitter In-phase Quadrature (IQ) imbalance. Proposed method compensates imbalance by exploiting indirect learning architecture (ILA) and complex filters whose coefficients are determined in an iterative process. Compensation performance is assessed after the method has been implemented in a Software Defined Radio (SDR) platform, capable of transmitting modulations at different central frequencies. Measured results demonstrate that the imbalance related images are reduced down to the noise floor. After applying the proposed IQ imbalance correction method, the transmitter image rejection ratio (IRR) is increased by 15dB in the case of an SDR transmitter operating at central frequency of 1.7 GHz. The ADC/DAC sampling rate is 61.44MS/s, while the signal bandwidth, for which the compensation is performed, is 30.72MHz. The advantage of the proposed method is low complexity in terms of a reduced number of coefficients. The method is generic and can be utilized for IQ imbalance compensation when wideband signals are transmitted.*

Key words: *In-phase, quadrature imbalance, complex filters, indirect learning architecture, digital predistortion.*

1. INTRODUCTION

Identification of nonlinear systems with memory effects is one of the challenging topics in wireless communications. The Orthogonal Frequency Division Multiplexing

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(OFDM) systems have been widely used in many communication standards achieving high data rates and spectral efficiency [1]. However, performance of OFDM systems is significantly degraded in a presence of power amplifier (PA) nonlinearities and its memory effects. The degradation is caused by signal multi-carrier nature which introduces high peak-to-average power (PAPR) ratios and inter-modulation product terms. The resulting in-band interference severely degrades the signal quality. In addition, PA nonlinearity introduces out-of-band interference producing spectral regrowth [2].

Digital pre-distortion (DPD) is an efficient method that improves performance and energy efficiency of wireless infrastructure, compensating various transmitter imperfections [2]. DPD is basically used for compensation of PA distortions which arise due to the nonlinear PA transfer characteristics. DPD is implemented in the base-band (BB), before the digital-to-analogue (DA) conversions and BB to radio-frequency (RF) frequency up-conversions are performed. Other imperfections which can be compensated by DPD include transmitter in-phase and quadrature (IQ) imbalance and the crosstalk which exist between different channels in multi-input multi-output (MIMO) systems [3].

The IQ imbalance (IQI) occurs when the phase or amplitude of I and Q signal components are not perfectly matched. The impact of IQI on signal quality can be harmful, leading to the spectral regrowth, increased error rates and reduced system performance. This paper presents an efficient frequency-dependent (FD) IQI compensation method dedicated for usage in software-defined radio (SDR) transceivers. The compensation method is implemented in the BB using complex finite impulse response (FIR) filters whose coefficients are determined in an iterative process. The advantage of proposed method is that the IQI compensation is performed during the transmitter operation. Another advantage is low complexity in terms of reduced number of complex valued coefficients. Steps for efficient imbalance mitigation are thoroughly described, starting from a mathematical model to complete realization in SDR.

This paper is organized as follows. Related work is given in the following section. In the Section 3 the IQI mitigation method is described. In Section 4, the simulation setup is presented, followed by simulation results. The measured results are presented in Section 5. Section 6 is dedicated to discussion. The conclusion is drawn in the last section.

2. RELATED WORK

The IQI of RF transceivers is caused by various sources, such as the mismatches in the components of the transmitter chain, imperfections in the analog circuits including the analogue low-pass filters (LPF), phase and gain mismatches in mixers or limitations in the analogue-to-digital (ADC) and digital-to-analogue converters (DAC) [4].

Various techniques are employed for compensation of the IQ imbalance in wideband transmitters which can be generally divided in calibration and adaptive techniques.

Calibration methods are based on the measurement of actual imbalances in the hardware and applying digital correction schemes to compensate for these imbalances [5], [6]. Calibration techniques rely on utilization on test signals and their operations are performed at transceiver start-up [5]. Adaptive compensation techniques neutralize imbalance during transceiver operation [6].

The Refs [5]-[7] investigate the mismatches between LPFs of transmitter I and Q signal paths as a source of the FD IQI. In order to equalize the LPF frequency responses, a feedback path, consisting of additional ADC, is used to bring back the transmitter

output signal to the BB for imbalance detection [5], [6]. The imbalance is compensated using digital filters [5], [7]. In Ref. [5] the single-tone signals are used as the test signals. The least squares (LS) optimization method is employed to minimize the error that exists between the desired filter response and the measured one. In Refs. [8], [9] the transmitter impairments are reduced using complex-valued FIR filters. The coefficients are calculated in an iterative process which is based on the LS method.

DPD is often employed for the FD IQI mitigation [10]. Many publications combine the IQI compensation with PA linearization. Such publications extend the parallel Hammerstein structure [11], Volterra series model [12] and asymmetrical complexity-reduced Volterra series model [13]. Impairments are cancelled using the complex-valued filters. The filter coefficients are determined in an adaptive process that utilizes monitoring path in form of additional receiver [11]-[13]. Although efficient, methods suffer from an increase in computational complexity compared to an independent IQI compensation [14].

Most of the techniques which are found in the literature are implemented using laboratory equipment, in which modulation waveforms are created by software and vector signal generators (VSG).

In previous work [15] memory polynomial (MP) DPD is created that jointly compensates transmitter FD IQI, PA nonlinearity and PA memory effects. The disadvantage of MP DPD is limited signal bandwidth, because DAC/ADC sampling frequency should be at least five times greater than signal bandwidth. For ADC/DAC sample rate of 61.44MS/s, the maximum signal bandwidth of 20MHz is achieved [15]. In the Ref. [16] both transmitter and receiver IQI are calibrated in the same process. The method is developed for IQI compensation and wideband fifth generation new radio (5G NR) signals transmission. The maximum signal bandwidth of 100MHz is achieved at ADC/DAC sampling rate of 245.75MS/s [16]. The FD IQI is compensated by complex filters [17]. The IQI calibration method [16] does not use monitoring path and coefficient calculation process is not adaptive. The calibration procedure is executed only at transceiver power-up. The method [16] utilizes single tone test signals for IQI identification and calibration. During calibration process the digital modulator is stopped and numerically controlled oscillator (NCO) is employed for test signal generation [16].

Unlike the method described in [16], the proposed method is adaptive and utilizes a monitoring path for IQI identification. This implies that compensation is performed during the transceiver normal operation. The transmitter impairments are reduced using adaptive complex-valued FIR filters. The coefficients are calculated in an iterative process that is based on the recursive least squares (RLS) method. The method can be employed in the applications when wideband signals are transmitted.

3. IQ Imbalance Correction Method

The signal $x(n)$, consisting of quadrature components $x_I(n)$ and $x_Q(n)$, is modified by the IQ imbalance source into the signal $y(n)$, consisting of components $y_I(n)$ and $y_Q(n)$.

$$\begin{aligned} y_I(n) &= x_I(n) \cdot G_I(\omega) \cos(\omega n + \varphi_I(\omega)) \\ y_Q(n) &= x_Q(n) \cdot G_Q(\omega) \sin(\omega n + \varphi_Q(\omega)) \end{aligned} \tag{1}$$

Amplitude response functions of I and Q channels are denoted by $G_I(\omega)$ and $G_Q(\omega)$, while corresponding channel phases are $\varphi_I(\omega)$ and $\varphi_Q(\omega)$. The IQ imbalance is defined by gain and phase imbalance functions, $\varepsilon_{err}(\omega)$ *and* $\varphi_{err}(\omega)$, which are defined by (2) and (3) [10]:

$$\varepsilon_{err}(\omega) = \frac{G_I(\omega)}{G_Q(\omega)} \tag{2}$$

$$\varphi_{err}(\omega) = \varphi_I(\omega) - \varphi_Q(\omega) \tag{3}$$

Transmitter IQI leads to the incomplete image signal rejection which is quantified by image rejection ratio (IRR) [10]:

$$IRR(\omega) = 10\log\frac{1+\varepsilon_{err}(\omega)^2 + 2\varepsilon_{err}(\omega)\cos(\varphi_{err}(\omega))}{1+\varepsilon_{err}(\omega)^2 - 2\varepsilon_{err}(\omega)\cos(\varphi_{err}(\omega))} \tag{4}$$

The functions $\varepsilon_{err}(\omega)$ and $\varphi_{err}(\omega)$ are frequency dependent. The transmitter, which is composed of real valued circuits, has positive symmetrical $\varepsilon_{err}(\omega)$ around the DC and negative symmetrical $\varphi_{err}(\omega)$ [18]. In this case, the imbalance can be compensated using two real-valued FIR filters positioned in the BB, in separate I and Q signal paths. However, in RF, the transmitter symmetry may be degraded. It was proven that transmitters produce asymmetric $\varepsilon_{err}(\omega)$ and $\varphi_{err}(\omega)$ [9]. The utilization of valued digital filters is required for IQI compensation [9].

The generalized diagram of the circuit dedicated for wideband IQ imbalance correction is depicted in Fig. 1a). The correction scheme is based on utilization of a complex FIR filters, adopted from [9]. The IQ imbalance correction method utilizes an indirect learning architecture (ILA) which is comprised of two complex filters, denoted with predistorter and postdistorter, as depicted in Fig. 1a). The predistorter takes at input the complex-valued signal $xp(n)$, produced by a digital modulator. The real and imaginary parts of $xp(n)$ are denoted with $xp_I(n)$ and $xp_Q(n)$, respectively.

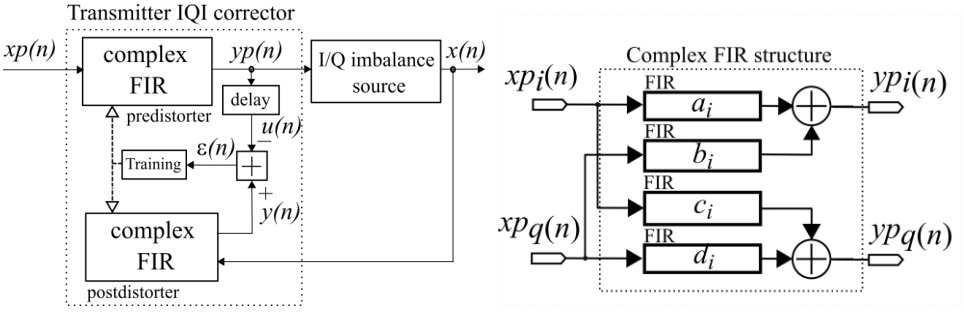


Fig. 1 a) Indirect learning architecture dedicated for IQI rejection b) complex FIR structure

The predistorter produces at output the signal $yp(n)$ consisting of $yp_I(n)$ and $yp_Q(n)$ components:

$$yp(n) = yp_I(n) + \mathbf{j}\cdot yp_Q(n) = \sum_{i=0}^{N}(a_i \cdot xp_I(n-i) + b_i \cdot xp_Q(n-i)) + \mathbf{j}\sum_{i=0}^{N}(c_i \cdot xp_I(n-i) + d_i \cdot xp_Q(n-i)) \quad (5)$$

The parameter N represents the filter order, while a_i, b_i, c_i, d_i are FIR coefficients. Postdistorter is a simple copy of predistorter, both sharing the same set of coefficients.

$$y(n) = y_I(n) + \mathbf{j}\cdot y_Q(n) = \sum_{i=0}^{N}(a_i \cdot x_I(n-i) + b_i \cdot x_Q(n-i)) + \mathbf{j}\sum_{i=0}^{N}(c_i \cdot x_I(n-i) + d_i \cdot x_Q(n-i)). \quad (6)$$

The block diagram of the complex FIR dedicated for IQ correction is depicted in Fig. 1b). The circuit is composed of four real valued FIR filters. Two real-valued FIRs are positioned in I and Q signal paths. The other two are located in the cross paths. The FIR filters have length N. The coefficients are calculated in an adaptive process using RLS algorithm. The RLS aims to minimize the sum of the squares of the difference between the predistorter and postdistorter outputs. The RLS cost function $K(n)$ is defined as:

$$K(n) = \sum_{m=0}^{n}\lambda^{n-m}((u_I(m) - y_I(m))^2 + (u_Q(m) - y_Q(m))^2), \quad (7)$$

where $u_I(n)$ and $u_Q(n)$ are real and imaginary parts of the $yp(n)$, delayed by loop delay from predistorter output to the postdistorter output. The λ is the RLS "*forgetting factor*" [10]. In order to minimize $K(n)$, system of linear equations is formed by setting to zeros the partial derivatives of $K(n)$ in respect to a_i, b_i, c_i, d_i. To express system of equations in a matrix form, the coefficients a_i, b_i, c_i, d_i are stored in the vector $\mathbf{S}(n)$.

$$\begin{aligned}\mathbf{S}(n) &= [s_i \quad s_{i+N+1} \quad s_{i+2(N+1)} \quad s_{i+3(N+1)}]^T_{4(N+1)} \\ &= [a_i \quad b_i \quad c_i \quad d_i]^T_{4(N+1)}, \quad i = 0,...,N.\end{aligned}, \quad (8)$$

The signals $u_I(n)$ and $u_Q(n)$ are stored in the vector $\mathbf{u}(n)$:

$$\mathbf{u}(n) = [u_i]_{4(N+1)} = [u_I(n) \quad u_Q(n) \quad 0 \quad ... \quad 0]_{4(N+1)}. \quad (9)$$

The signals $x_I(n)$ and $x_Q(n)$ and its previous samples are stored the matrix $\mathbf{X}(n)$, which has dimension $4(N+1)$x$4(N+1)$:

$$\mathbf{X}(n) = \begin{bmatrix} x_I(n-i)_{i,0} & x_Q(n-i)_{i,1} & 0 & ... & 0 \\ -x_Q(n-i)_{i+N+1,0} & x_I(n-i)_{i+N+1,1} & 0 & ... & 0 \\ x_I(n-i)_{i+2(N+1),0} & -x_Q(n-i)_{i+2(N+1),1} & 0 & ... & 0 \\ x_Q(n-i)_{i+3(N+1),0} & x_I(n-i)_{i+3(N+1),1} & 0 & ... & 0 \end{bmatrix}_{4(N+1)\times 4(N+1)} \quad (10)$$

Following the RLS algorithm, after every training step, the elements of matrix $\mathbf{A}(n)$ and vector $\mathbf{B}(n)$ are calculated according to (11) and (12). The matrices $\mathbf{A}(n)$ and $\mathbf{B}(n)$ have dimensions $4(N+1)$ x $4(N+1)$ and $4(N+1)$ x 1, respectively.

$$\mathbf{A}(n) = \mathbf{X}(n)\times\mathbf{X}(n)^T + \lambda\cdot\mathbf{A}(n-1) \quad (11)$$

$$\mathbf{B}(n) = \mathbf{X}(n) \times \mathbf{u}(n)^T + \lambda \cdot \mathbf{B}(n-1) \tag{12}$$

The system of equations in matrix form is expressed by (13). The a_i, b_i, c_i and d_i are found by solving the (13).

$$\mathbf{A}(n) \times \mathbf{S}(n) = \mathbf{B}(n)\,, \tag{13}$$

4. SIMULATION OF IQ CORRECTION METHOD

The IQI corrector model has been implemented in SystemC [19], the set of C++ classes which can be used to system-level modeling [19]. The advantage of SystemC utilization is possibility to simulate the real-time environments, using datatypes offered by standard C++ and additional ones, defined in the SystemC libraries. The simulation setup is depicted in the Fig. 2. The figure presents the transmitter and receiver paths consisting of the digital modulator, predistorter, postdistorter, the IQ imbalance source, inverse SINC filter, ADC and DAC, modeled in SystemC.

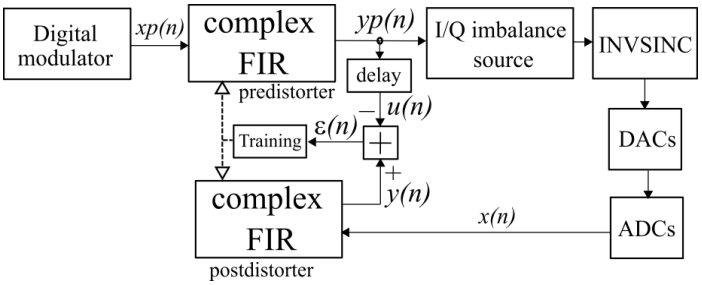
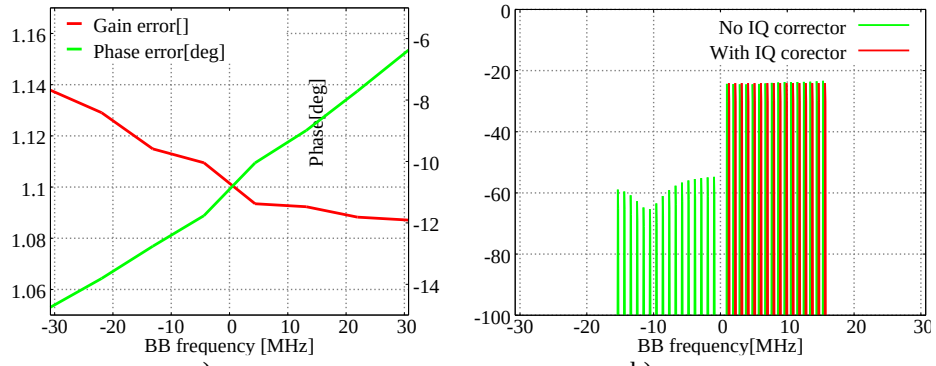


Fig. 2 Simulation setup for IQ imbalance rejection

As a test waveform the low intermediate frequency (low-IF) waveform is used. It consists of the sixteen single frequency tones. The waveform is generated at the rate of 61.44MS/s. The frequencies of successive tones are spaced by 0.96MHz, covering the frequency range from DC to the 15.36MHz.

The SystemC model of IQ corrector is designed based on (5). The order of complex filter is represented by parameter *N*. In every training step, new elements of matrices **A**(*n*) and **B**(*n*) are calculated according to (11) and (12). The coefficients are obtained after the system of equations (13) is solved. For this task the LU decomposition method is used. After the signal is processed by predistorter, the imbalance is inserted into signals (Fig. 2).

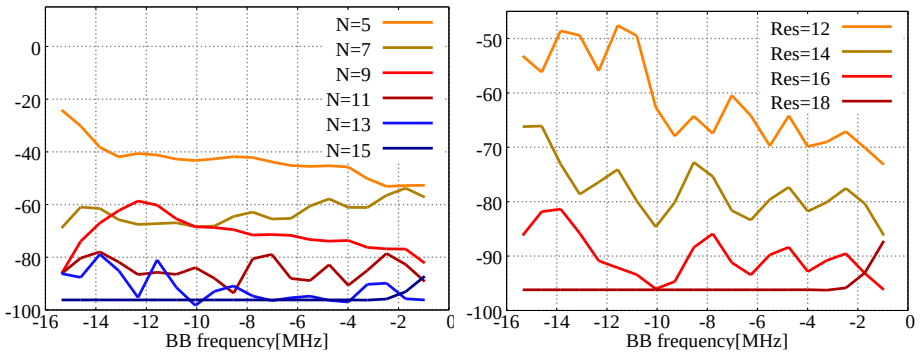
The IQI source is created based on measured data. For this purpose, the RF transceiver IC LMS7002M [20] is tuned to central frequency of 3.55GHz. Transmitter IQ gain and phase error values are determined for the BB frequencies in the range between -30.72MHz and 30.72MHz, with a step of 5MHz. The imbalance values are calculated and used as inputs of IQI source model. Derived gain and phase imbalance functions manifest FD behavior and they are depicted in Fig. 3a).



a) b)

Fig. 3 a) Measured gain and phase errors of transmitter at 3.55GHz, b) Simulation results of transmitter output a) when correction is bypassed and b) when correction is applied.

The DAC roll-off is compensated by an inverse SINC filter. In simulations the arithmetical precision of 18 bits is adopted and the number of points for FFT is set to 2^{16}. The simulation results shows efficiency of the proposed method in image rejection. Fig. 3b) depicts the power spectral densities of transmitter output signal when corrector is bypassed and in the case when IQI correction method is applied. As it can be seen from Fig. 3b), imbalance produced tone signals are completely removed. The presented results correspond to the 18-bit ADC/DAC resolution and utilized filter order is N=16.



a) b)

Fig. 4 a) IRR results as a function of filter order N and BB frequency. b) The impact of ADC/DAC resolution *Res* on IRR results at different BB frequencies.

Simulations gave valuable information about required complex filter order N and ADC/DAC sampling rate. In simulations, the influence of filter order N on IQI mitigation performance is investigated. The N is gradually increased from N=5 to N=15. The IRR results, as a function of N, are presented in Fig. 4a). The results correspond to the 18-bit ADC/DAC resolution and the sample rate of 61.44MS/s. The results in Fig. 4a) show dependence between the selected filter order and obtained IRR values. The imbalance is more efficiently compensated with the increase of N. On the other side, lower N occupies

less hardware resources. If we take the result as satisfactory when IRR is improved over 60dB, it can be concluded that filter order should be greater or equal than N=7.

Finally, the impact of ADC/DAC resolution on IQI mitigation performance is analyzed. The resolution, denoted with parameter *Res*, is changed from *Res*=12 to *Res*=18, with a step of ΔR=2. In the simulations the filter order is set to 16 and the sample rate is 61.44MS/s. The amplitudes of tones at negative frequencies are determined and IRR values calculated. The IRR results are presented in Fig. 4b). The imbalance related images are efficiently suppressed if *Res* is greater or equal than 14.

5. Implementation and Measured Results

Measurement results are obtained after the method has been implemented in the LimeSDR board [21]. The SDR incorporates a transceiver IC LMS7002M [20] for the frequency conversion between BB and RF. The chip is capable of transmitting modulations at different central frequencies from several MHz to 3.8GHz. The transmitter exhibits FD IQI whose amount is increased with the increase of central frequency [16].

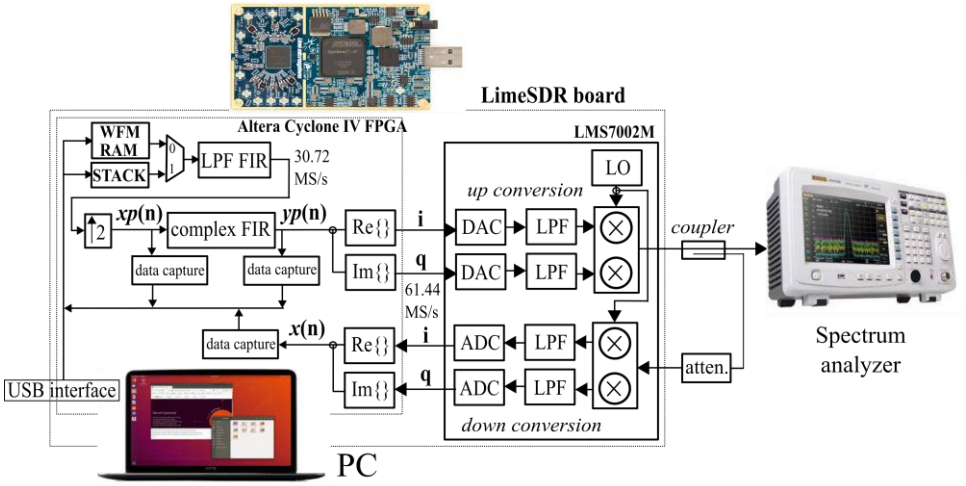


Fig. 5 IQI corrector implementation in the SDR board.

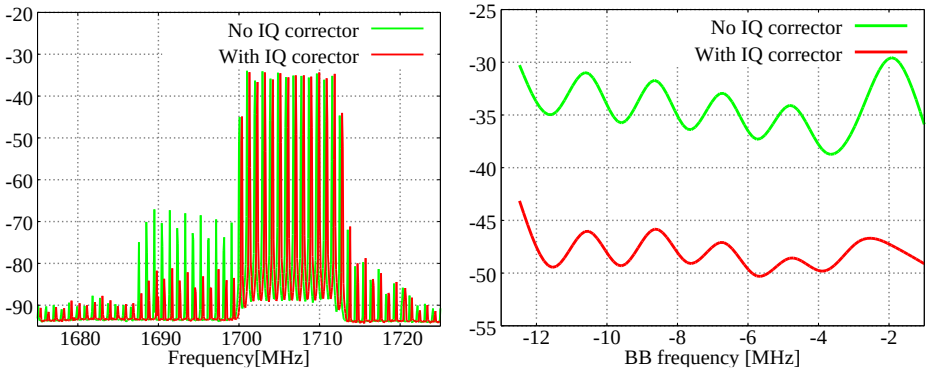
The general block diagram of the SDR board is depicted in Fig. 5. For clarity, only hardware blocks, which are required for method description, are shown in Fig. 5. The Altera Cyclone IV FPGA chip is utilized for the implementation of IQI compensation circuits [20]. The board uses 12-bit DAC/ADCs and it is connected to the CPU core through the USB interface [21]. For the development or demo, the test waveform can be uploaded and played from FPGA internal RAM blocks. In real applications, the CPU core performs digital modem functions transmitting the waveforms over USB interface at a rate of 30.72MS/s [21].

The SDR board implements both transmit (TX) and receive (RX) channels [21]. The IQ corrector is located in the TX path (Fig.5.). For IQ imbalance identification additional

RX channel is used, whose output is represented by the signal $x(n)$ in the Fig. 5. The monitoring path is utilized by the complex filter training process.

The interpolation circuit is used to double the data rate from 30.72MS/s to 61.44MS/s. It is followed by the IQ corrector (the predistorter), implemented as 8th order complex FIR filter. The number of real-valued coefficients is $4(N+1) = 36$. The circuit operates at 61.44MS/s sample rate. Its implementation in FPGA is optimized by multiplexing input data and executing the operations at the clock frequency of 122.88MHz, which is determined by longest propagation delay of FPGA blocks. The 18-bit arithmetic precision is adopted based on the simulation results.

The predistorter occupies following FPGA resources: 2130 combinatorial adaptive look-up tables (ALUT), 3402 dedicated logic registers and 18 DSP blocks. The FPGA have the provision of capturing following signals: the corrector input $xp(n)$, output $yp(n)$ and monitoring path input $x(n)$. The $xp(n)$, $yp(n)$ and $x(n)$ data streams are made available to the CPU core over the USB interface. The coefficients are calculated by software performing the role of the postdistorter. In each RLS iteration step, after the coefficients are calculated, they are sent back to LimeSDR board via USB interface. Beside LimeSDR board and CPU core, the hardware equipment includes the Rigol DSA1030 spectrum analyzer (SA). The SA input is connected to TX output and SA is used for IRR measurements.



a) b)

Fig. 6 a) Spectra of signals obtained at transmitter output when 13-tone waveforms is applied, obtained at central frequency of 1.7GHz b) Measured IRR results obtained at the same central frequency.

The software consists of Lime Suite GUI application [21] dedicated to configuration of SDR board and specially created command-line application. At the beginning of measurement process, the configuration file is loaded into LMS7002M using Lime Suite GUI. Also, the LMS7002 DAC and ADC sample rate is configured to 61.44MHz. Upon loading the configuration files, the LMS7002M transmitter is set in un-calibrated state.

The command-line application is created specifically for IQ calibration process control. It implements the postdistorter, performing the operations defined by (11) – (13). In order to automate the measurement process, the application provides control of SA via virtual instrument software architecture (VISA) interface. The IRR measurements are conducted before the calibration, and after the calibration is done.

In order to assess the IQI mitigation performance, asymmetrical positive-band thirteen-tone waveform is used as a test signal. The waveform is generated at the rate of 30.72MS/s. The frequencies of successive tones are spaced by 0.96MHz, covering the frequency range from DC to the 12.48MHz. Besides, the LMS7002M local oscillator (LO) is tuned to the frequency of 1700MHz.

Fig. 6a) illustrates the results by showing power spectral densities of the transmitter output with and without using IQI corrector. The IRR values, measured at negative BB frequencies, are given in Table 1. It can be seen from Fig. 6b) that IRR is increased from 35dB, measured for un-calibrated transmitter, to approximately 50dB.

Table 1 IRR at negative frequencies for 13-tone waveform

f [MHz]		-6.72	-5.76	-4.8	-3.84	-2.88	-1.92	-0.96
IRR[dB]	Corr. off	32.92	37.3	34.08	38.46	35.4	29.56	36.31
	Corr. on	47.08	50.27	48.57	49.81	47.04	47.38	49.19
f [MHz]			-12.48	-11.52	-10.56	-9.6	-8.64	-7.68
IRR[dB]	Corr. off		30.27	34.92	30.99	35.76	31.71	36.4
	Corr. on		43.15	49.46	46.01	49.32	45.82	49.07

6. DISCUSSION

The simulation and measurement results demonstrate an efficient IQI mitigation without sacrificing the transmitter output power. The advantage of the proposed method is that the transmitter's static IQ calibration procedure is not required.

The IQI correction is implemented using a complex FIR filter whose coefficients are found iteratively by an RLS algorithm. The postdistorter is implemented in the software. In each iteration step, new coefficients are calculated and sent back to the predistorter. The FIR registers are programmed periodically, once after every several seconds during the transmitter operation. In simulations the impact of complex filter order N on IRR results is analyzed. It is shown that N should be greater than 8 in order to have IRR values greater than 60dB. Furthermore, in simulations the impact of ADC/DAC resolution on the IQI compensation performance is analyzed. The resolution Res=14 gives satisfactory IRR results.

The IQ compensation performance of the method is evaluated after it is implemented in low-cost SDR board. The resolution of ADC/DACs, located in the transceiver IC LMS7002M, is limited to 12 bits [21]. The data rate of digital interface between FPGA and LMS7002M is limited to 61.44MS/s [21]. The ADC/DAC sampling rate is 61.44MS/s, while the signal bandwidth, for which the compensation is performed, is 30.72MHz.

The method provides low complexity in terms of a reduced number of coefficients. The number of coefficients is $4(N+1)$. For parameter N=8, the number of coefficients is 36. A reduced number of coefficients enables savings of FPGA resources. It is worth mentioning that beside the IQ corrector, the TX chain includes the other digital blocks, such as the crest factor reduction (CFR) and post-CFR FIR filters, for which implementation significant amount of FPGA resources is required [22].

In a simulation and in real measurements asymmetrical multi-tone signal is used as test waveform. However, in a simulation and in real measurements the system parameters are not identical. In simulations, the waveform sample rate is 61.44MS/s. The highest tone is positioned at 15.36MHz, which is half of the Nyquist frequency. In the measurements, the

sample rate of the input waveform is 30.72MHz, and therefore, it was impossible to generate a tone at 15.36MHz. Instead, in measurements, thirteen-tone waveform is used. After the interpolation block is utilized, the sample rate is increased to 61.44 MS/s and the Nyquist frequency became 30.72MHz. The highest tone in the waveform is made close to the half of the Nyquist frequency. The measurement results, which are presented in Table 1, confirm the accuracy of the simulation results. Before compensation is performed, the average IRR is 34.16 dB. After the compensation is performed, the average IRR becomes 47.85dB. Although the IQI effects are observed and analyzed for negative image frequencies, the method gives similar results if IQI is present at positive frequencies.

The advantage of the proposed IQ corrector, compared to MP DPD [15], is reduced ADC/DAC sampling rate. For example, in order to transmit 100MHz wideband signals, the MP DPD ADC/DAC sampling frequency must be at least 500MHz [15]. If the proposed method is used for transmission of 100MHz signals, very high-speed ADC and DAC are not required. Sufficient ADC/DAC sample rate is 245.76MS/s. Transmitted signal bandwidth maximum is equal to the half of a sampling frequency. Moreover, being adaptive, the proposed method has significant advantage over the method presented in [16]. The proposed IQ calibration method is generic and can be applied in wideband transmitters.

Table 2 Comparison of proposed method with the methods found in literature

reference	BB bandwidth [MHz]	Sample rate [MS/s]	Central frequency [GHz]	Before comp. IRR[dB]	After comp. IRR[dB]
[23]	400	800	11	20	45
[13]	150	10000	1	40-45	50-55
[16]	100	245.76	1.5-3.5	20-30	45-55
proposed	30.72	61.44	1.7	35	50

Another advantage of the proposed IQ corrector is reduced complexity. The MP DPD parameters are chosen to accommodate a specific PA architecture and transmitter IQI characteristics. The number of MP DPD coefficients is significantly larger than in the proposed method. In order to achieve similar IQI compensation performance, the MP DPD memory length should be equal to complex filter order. For the selected nonlinearity order M=2 and memory length N=8, the total number of MP DPD real-valued coefficients is 72 [15]. For N=8, the number of coefficients in proposed IQ corrector is 36. The number of utilized DSP blocks is directly related to the number of coefficients and it is limited by FPGA resources. Moreover, measured results showed that the IQ gain and phase errors get increased with the increase of SDR central frequency, demanding greater N value [16]. When comparing measured results with the results from literature test-bed conditions cannot be neglected, such as the number of bits of the waveforms, the data rate and DAC/ADC resolution. The measured results found in literature are produced using laboratory equipment that relies on high-performance signal generators. Moreover, calibration procedures are realized in MATLAB. The Ref. [23] uses a wideband transmitter with a 400MHz bandwidth, operating at 11GHz.

The circuit parameter estimation is carried out by high-performance BB/DAC boards and the CPU board, where a DAC with 16-bit resolution and 800MS/s sampling rates were used. The CPU board performs signal processing. Automatic parameter estimation

software is achieved using MATLAB. By compensating for IQI, the image components were reduced less than the IRR threshold of 45dB, the method yields increase in IRR by 10-15dB. In Ref. [13] 10dB IRR enhancement is achieved. The method produces more that 50dB IRR on both sidebands, which indicates that the FD IQI is mitigated well. In the Ref. [16] 20-25dB increase in IRR is achieved for the signal bandwidth of 100MHz.

7. CONCLUSION

In this paper we consider the effects of the IQ imbalance in wireless transmitters and propose low complexity IQ correction method, based on the indirect learning architecture. The method yields linearization results comparable with conventional DPD solutions while minimizing the number of coefficients. The method performance has been evaluated after it is implemented on the SDR board. The measurement results show excellent performance in terms of IRR. The IQI images are suppressed down to the noise floor. In case of multi tone waveform the IRR improvement of 15dB is achieved. Measured results are derived with ADC/DAC sample rate of 61.44MS/s. Transmitted signal bandwidth is 30.72MHz. The proposed method is generic and can be utilized in other SDR platforms transmitting wideband signals.

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REFERENCES

[1] V. Stanković and Z. Perić, "OFDM Low Complexity Channel Estimation using Time-Frequency Adjustable Window Functions", *Facta Universitatis, Series: Automatic Control and Robotics*, 2022, vol. 21, no. 2, pp. 107–116, DOI:10.22190/FUACR210824009S

[2] J. K. Cavers, "The effect of quadrature modulator and demodulator errors on adaptive digital predistorters for amplifier linearization", *IEEE Transactions on Vehicular Technology*, 1997, vol. 46, no. 2, pp. 456–466, DOI:10.1109/25.580784

[3] Z. A. Khan, E. Zenteno, P. Händel, M. Isaksson, "Digital Predistortion for Joint Mitigation of I/Q Imbalance and MIMO Power Amplifier Distortion", *IEEE Transactions on Microwave Theory and Techniques*, 2016, vol. 65, no. 1, p. 322–333. DOI: 10.1109/TMTT.2016.2614933

[4] M. Valkama, "Advanced I/Q signal processing for wideband receivers: Models and Algorithms", Ph.D. dissertation, Tampere (Finland): Tampere University of Technology, 2001. ISBN:9521507152

[5] J. Tuthill and A. Cantoni, "Efficient compensation for frequency-dependent errors in analog reconstruction filters used in IQ modulators", *IEEE Transactions on Communications*, 2005, vol. 53, no. 3, pp. 489–496, DOI:10.1109/TCOMM.2005.843455

[6] A. G. K. C. Lim, V. Sreeram and G.Q. Wang, "Digital compensation in IQ modulators using adaptive FIR filters", *IEEE Transactions on Vehicular Technology*, November 2004, vol. 53, no. 6, pp. 1809–1817, DOI:10.1109/TVT.2004.836934

[7] P. Kiss and V. Prodanov, "One-tap wideband I/Q compensation for zero-IF filters", *IEEE Transactions on Circuits and Systems I: Regular Papers*, June 2004, vol. 51, no. 6, pp. 1062–1074, DOI:10.1109/TCSI.2004.829233

[8] L. Ding, Z. Ma, D. R. Morgan, M. Zierdt and G. T. Zhou, "Compensation of frequency-dependent gain/phase imbalance in predistortion linearization systems", *IEEE Transactions on Circuits and Systems I: Regular Papers*, 2008, vol. 55, no. 1, pp. 390–397, DOI:10.1109/TCSI.2007.910545

[9] L. Anttila, M. Valkama and M. Renfors, "Frequency-Selective IQ Mismatch Calibration of Wideband Direct-Conversion Transmitters", *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 55, no. 4, pp. 359-363, April 2008, DOI:10.1109/TCSII.2008.919500.

[10] J. K. Cavers and M. W. Liao "Adaptive compensation for imbalance and offset losses in direct conversion transceivers", *IEEE Transactions on Vehicular Technology*, November 1993, vol. 42, no. 4, p. 581–588, DOI:10.1109/25.260752

[11] L. Anttila, P. Handel, and M. Valkama, "Joint mitigation of power amplifier and I/Q modulator impairments in broadband direct-conversion transmitters", *IEEE Transactions on Microwave Theory and Techniques*, April 2010, vol. 58, no. 4, pp. 730–739. DOI:10.1109/TMTT.2010.2041579

[12] H. Cao, A S. Tehrani, C. Fager, T. Eriksson and H. Zirath, "I/Q imbalance compensation using a nonlinear modeling approach", *IEEE Transactions on Microwave Theory and Techniques*, 2009, vol. 57, no. 3, pp. 513–518. DOI: 10.1109/TMTT.2008.2012305

[13] W. Li, Y. Zhang, L.K. Huang, J. Cosmas, C. Maple and J. Xiong, "Self-IQ-Demodulation Based Compensation Scheme of Frequency-Dependent IQ Imbalance for Wideband Direct-Conversion Transmitters. *IEEE Transactions on Broadcasting*. 2015, vol. 61. no. 4, pp. 666-673, DOI: 10.1109/TBC.2015.2465138.

[14] F. Mkadem, M. C. Farres, S. Boumaiza, and J. Wood, "Complexity reduced Volterra series model for power amplifier digital predistortion", *Analog Integrated Circuits and Signal Processing*, 2014, vol. 79, pp. 331–343, DOI:10.1007/s10470-014-0266-4

[15] B. Jovanović and S. Milenković, "Transmitter IQ Imbalance Mitigation and PA Linearization in Software Defined Radios", *Radioengineering Journal*, Vol. 31, No. 1, April, 2022, pp. 144-154 , ISSN 1210-2512, DOI:10.13164/re.2022.0144

[16] B. Jovanović and S. Milenković: "IQ Imbalance Correction in Wideband Software Defined Radio Transceivers", *Radioengineering Journal*, December, 2023, pp. 479-491, ISSN 1210-2512, DOI:10.13164/re.2023.0479

[17] S. Nikolić, G. Stančić and S. Cvetković, "Realization of Digital Filters with Complex Coefficients", *Facta Universitatis, Series: Automatic Control and Robotics*, 2018, vol. 17, no. 1, pp. 25–38, DOI:10.22190/FUACR1801025N

[18] B. Razavi, "Design Considerations for Direct-Conversion Receivers", *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, 1997, vol. 44, no. 6, pp. 428–435. DOI:10.1109/82.592569

[19] SystemC (2023), http://accellera.org/downloads/standards/systemc

[20] Limemicrosystems, LMS7002M (accessed 2023), https://limemicro.com/technology/lms7002m/

[21] Limemicrosystems, LimeSDR (accessed 2023), https://limemicro.com/products/boards/limesdr/

[22] B. Jovanović and S. Milenković, "PA Linearization by Digital Predistortion and Peak To Average Power Ratio Reduction in Software Defined Radios", *Journal of Circuits Systems and Computers*, 2020, vol. 29, no. 9, pp. 1–19. DOI: 10.1142/S0218126620501479

[23] M. Kim, Y. Maruichi and J. I. Takada, "Parametric Method of Frequency Dependent I/Q imbalance Compensation for Wideband Quadrature Modulator", *IEEE Transactions on Microwave Theory and Techniques*, 2013, vol. 61, no. 1, pp. 270–280, DOI: 10.1109/TMTT.2012.2228215