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REPETITIVE RIPPLE ESTIMATOR FILTER BASED PHASE-LOCKED LOOP

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Abstract. *In this paper, a novel phase-locked loop is presented based on a repetitive ripple estimator filter. The primary application of the presented phase-locked loop is in the monitoring of three-phase grid voltages and synchronization of grid connected power converters for renewable energy sources with the grid. The filter is inserted inside the loop filter of the phase-locked loop to reject oscillations that can be expected from common grid voltage disturbances. Details of the filter and phase-locked loop are presented, along with the influence of all freely adjustable parameters on overall system behaviour. In the end, the behaviour of the novel phase-locked loop is tested, validated and compared to the base phase-locked loop.*

Key words: *Renewable energy sources, phase-locked loop, synchronization.*

1. INTRODUCTION

As renewable energy sources increase their share in total electricity production, so does their role in the stability of electrical power systems [1]. It is up to the interface elements between renewable energy sources and power systems to positively contribute to the overall stability of power systems. In the case of hydropower plants, the conversion of the kinetic energy of water into electrical energy is done through power turbines and synchronous

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machines. This process is well-researched and guidelines are established for safe and reliable operation [2]. In the case of modern renewable energy sources, like photovoltaic and wind power plants, electrical energy obtained after prime conversion is not suitable for exchange without additional modification. This modification is done using a grid connected inverter – power electronic-based device that serves as an interface element between renewable energy sources and an electrical power system [3].

Traditional synchronous machines require harmonization of generated voltages with the power system at the point of coupling with the power system before connection. This process is referred to as machine synchronization and includes matching of the machine's output voltage amplitude, frequency, phase angle and direction of rotation with the power system in the point of coupling. Synchronization is done before connection with the power system, and after a successful connection, the physical phenomena of generator-grid interaction maintains once achieved synchronization. On the opposite side, synchronization of grid-tie inverters has to be constantly performing during operation [4].

Over time, a broad spectrum of synchronization algorithms for grid-tie inverters was developed and adopted from similar applications. Along with the basic grouping of synchronization algorithms according to the number of phases (single phase and three phase), the largest classification is done according to the control method (open loop and closed loop). Open loop methods directly estimate grid voltage parameters necessary for synchronization. Closed loop methods incorporate feedback mechanisms for voltage parameter estimation. The majority of research papers today related to grid-tie inverters incorporates closed-loop methods due to their accuracy and performance, while the most popular methods in this group incorporate Phase-Locked Loop (PLL) [5].

Synchronous Reference Frame PLL (SRF-PLL) is ubiquitously exploited for the synchronization of grid-tie inverters, an algorithm that was thoroughly examined in scientific literature and easily implemented. But SRF-PLL can provide adequate performances when voltage unbalance is low, and there is no presence of voltage harmonics. If this is the case, undamped oscillations in the estimated grid voltage angle are present and the performance of all other algorithms that incorporate grid voltage angle deteriorates [6]. Coping with the voltage unbalance is usually done using Second Order Generalized Integrator (SOGI) [7] or Decoupled Double Synchronous Reference Frame (DDSRF) [8] modifications of basic SRF-PLL. These algorithms can be expanded to deal with oscillations resulting from voltage harmonics, but the practicality of that implementation is in question, due to a high number of elements and feedback loops. A more elegant method for dealing with disturbances due to voltage unbalance and/or harmonics incorporates a Moving Average Filter (MAF). It enables complete suppression of oscillations that are multiples of selected basic frequency, but with a cost on the dynamic performance of phase-locked loop [9].

In this paper, a novel method is proposed, based on repetitive control that provides the benefits of MAF without impacting the dynamic performance of the phase-locked loop. In subsequent chapters, theoretical analysis of oscillations in phase-locked loops, along with details of the proposed phase-locked loop is presented. The second chapter is dedicated to a detailed analysis of three-phase grid voltages, and the transfer of common grid disturbances in synchronous reference frame. In the third chapter basics of SRF-PLL are provided with a method for the calculation of freely selectable parameters. Forth chapter is dedicated to the proposed modification of SRF-PLL based on a repetitive filter. A detailed description of the filter is provided, its implementation, and the influence of all parameters on the overall system behavior. In the next section, validation of performance is done using MATLAB/Simulink on

a set of tests that include voltage sags and voltage harmonics. In the end, a conclusion is made according to the presented results.

2. THREE-PHASE GRID VOLTAGES

Time dependent form of phase values of three-phase grid voltages is presented using the following set of equations:

$$\begin{aligned} v_a(t) &= \sum_{h=0}^{\infty} V_{am,h} \cos(h\omega t + \varphi_{a,h}) \\ v_b(t) &= \sum_{h=0}^{\infty} V_{bm,h} \cos(h\omega t + \varphi_{b,h} - h\tfrac{2\pi}{3}) \\ v_c(t) &= \sum_{h=0}^{\infty} V_{cm,h} \cos(h\omega t + \varphi_{c,h} + h\tfrac{2\pi}{3}) \end{aligned} \tag{1}$$

where, $v_a(t)$, $v_b(t)$ and $v_c(t)$ presents a time dependant resulting voltage in phases *a*, *b* and *c*, *h* is a harmonic number ($h = 1$ is a fundamental voltage harmonic), $V_{am,h}$, $V_{bm,h}$ and $V_{cm,h}$ represents the amplitude of *h*-th voltage harmonic, ω is the angular frequency of fundamental harmonic, $\varphi_{a,h}$, $\varphi_{b,h}$ and $\varphi_{c,h}$ are the phase angle of *h*-th voltage harmonic in phase *a*, *b* and *c*.

Using the method of symmetrical components [10], and under the assumption that only fundamental voltage harmonic can have unbalance, voltages (1) can be grouped according to the sequence they belong to like:

$$\begin{aligned} v_a(t) &= \sum_{h=1,7,13\ldots} V_{m,h+} \cos(h\omega t + \varphi_{h+}) + \sum_{h=-1,-5,-11\ldots} V_{m,h-} \cos(h\omega t + \varphi_{h-}) \\ v_b(t) &= \sum_{h=1,7,13\ldots} V_{m,h+} \cos(h\omega t + \varphi_{h+} - h\tfrac{2\pi}{3}) + \sum_{h=-1,-5,-11\ldots} V_{m,h-} \cos(h\omega t + \varphi_{h-} - h\tfrac{2\pi}{3}) \\ v_c(t) &= \underbrace{\sum_{h=1,7,13\ldots} V_{m,h+} \cos(h\omega t + \varphi_{h+} + h\tfrac{2\pi}{3})}_{\textit{Positive sequence}} + \underbrace{\sum_{h=-1,-5,-11\ldots} V_{m,h-} \cos(h\omega t + \varphi_{h-} + h\tfrac{2\pi}{3})}_{\textit{Negative sequence}} \end{aligned} \tag{2}$$

In the previous equation, $V_{m,h+}$ ($V_{m,h-}$) are amplitudes of *h*-th positive (negative) sequence voltage harmonics. In (2) zero order sequence components are omitted from consideration. Voltages (2) can be transferred in the synchronous reference frame (*dq*) using Park transformation. After transformation three-phase system of voltages can be written in the form:

$$\begin{aligned} v_d(t) &= \sum_{h=1,7,13\ldots} V_{m,h+} \cos(h\omega t + \varphi_{h+} - \omega t) + \sum_{h=-1,-5,-11\ldots} V_{m,h-} \cos(h\omega t + \varphi_{h-} - \omega t) \\ v_q(t) &= \sum_{h=1,7,13\ldots} V_{m,h+} \sin(h\omega t + \varphi_{h+} - \omega t) + \sum_{h=-1,-5,-11\ldots} V_{m,h-} \sin(h\omega t + \varphi_{h-} - \omega t) \end{aligned} \tag{3}$$

Where $v_d(t)$ and $v_q(t)$ are direct and quadrature voltage components after Park transformation, and $\hat{\theta} = \hat{\omega}t$ presents an angle of Park transformation ($\hat{\omega}$ presents the angular frequency of Park transformation). If the fundamental positive voltage is separated from the sum in (3), and under the assumption of $\varphi_{1+} = 0$, the following expression can be obtained:

$$\begin{aligned} v_d(t) &= V_{m,1+}\cos(\omega t - \omega t) + \sum_{h=7,13...} V_{m,h+}\cos(h\omega t + \varphi_{h+} - \omega t) + \\ &\sum_{h=-1,-5,-11...} V_{m,h-}\cos(h\omega t + \varphi_{h-} - \omega t) \\ v_q(t) &= V_{m,1+}\sin(\omega t - \omega t) + \sum_{h=7,13...} V_{m,h+}\sin(h\omega t + \varphi_{h+} - \omega t) + \\ &\sum_{h=-1,-5,-11...} V_{m,h-}\sin(h\omega t + \varphi_{h-} - \omega t) \end{aligned} \tag{4}$$

From (4) can be concluded that when the angular frequency of the fundamental harmonic matches the angular frequency of Park transformation ($\omega = \hat{\omega}$), the fundamental frequency in the synchronous reference frame is observed as a DC component. Other components can be grouped, and the following expression can be obtained

$$\begin{aligned} v_d(t) &= V_{m,1+}\cos(\omega t - \omega t) + f(2h, 6h, 12h...) \\ v_q(t) &= V_{m,1+}\sin(\omega t - \omega t) + f(2h, 6h, 12h...) \end{aligned} \tag{5}$$

where $f(2h, 6h, 12h...)$ is a function that consists of the oscillation on 2*h*, 6*h*, 12*h* and a result of fundamental voltage unbalance, fifth and seventh harmonic, eleventh and thirteenth harmonic, respectively.

3. SYNCHRONOUS REFERENCE FRAME PHASE-LOCKED LOOP

Substituting $\hat{\theta} = \hat{\omega}t$ and $\theta_{1+} = \omega t$ in (5), and under previous assumption $\omega = \hat{\omega}$, the following equation can be obtained:

$$\begin{aligned} v_d(t) &= V_{m,1+}\cos(\theta_{1+} - \theta) + f(2h, 6h, 12h...) \\ v_q(t) &= V_{m,1+}\sin(\theta_{1+} - \theta) + f(2h, 6h, 12h...) \end{aligned} \tag{6}$$

If the oscillatory term is neglected, when $\theta_{1+} \approx \hat{\theta}$, direct and quadrature components can be written in the form:

$$\begin{aligned} v_d(t) &= V_{m,1+}\cos(\theta_{1+} - \theta) \approx V_{m,1+} \\ v_q(t) &= V_{m,1+}\sin(\theta_{1+} - \theta) \approx V_{m,1+}(\theta_{1+} - \theta) \end{aligned} \tag{7}$$

According to (7), when the fundamental grid voltage vector angle matches the Park transformation angle, the quadrature component in the synchronous reference frame is equal to zero. This is the basic mechanism behind the fundamental phase-locked loop – SRF-PLL.

The block structure of SRF-PLL is presented in Fig. 1. It consists of a Phase Detector (PD), Loop Filter (LF) and Voltage Controlled Oscillator (VCO). The role of PD is to provide an output proportional to the difference between the grid voltage angle and the estimated angle. LF determines the output dynamics and VCO generates a phase angle proportional to input frequency. PD in its basic variant consists of Park transformation, and the voltage v_q is used as a measure of phase difference (as shown in (7)). LF consists of a PI controller, and VCO consists of an integrator and feedforward angular frequency ω_{ff} (fixed to nominal grid frequency) to speed up the process of initial synchronization [11]. Laplace complex variable is denoted as p.

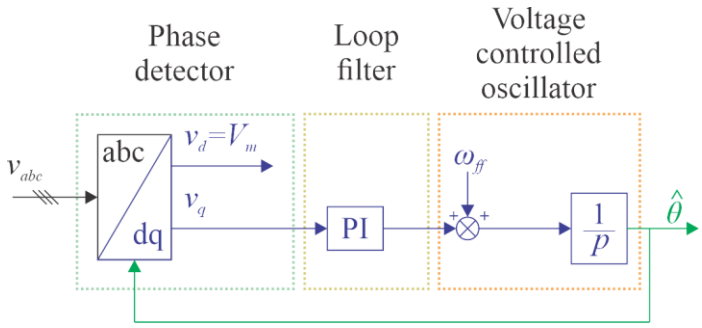


Fig. 1 Block structure of Synchronous Reference Frame Phase-Locked Loop (SRF-PLL)

A small signal model of SRF-PLL is shown in Fig. 2 [12], with $D(p)$ Laplace representation of oscillations shown in (6) is denoted $D(p) = L(f(2h, 6h, 12h...))$. As can be observed, oscillations have the same control path as the difference between the fundamental positive grid voltage angle and the estimated angle at the output of SRF-PLL θ. k_p and T_i are proportional gain and integral time constant of the PI controller.

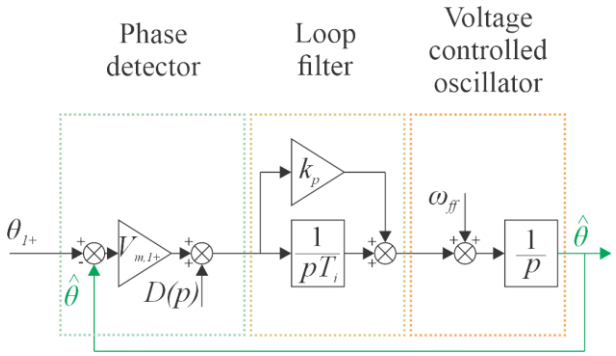


Fig. 2 Small signal model of SRF-PLL

The open loop transfer function of SRF-PLL can be presented in the form:

$$G_{ol}(p)=\frac{\theta(p)}{\theta_{1+}(p)}=V_{m,1+}\frac{pk_pT_i+1}{p^2T_i} \tag{8}$$

And closed-loop transfer function of SRF-PLL can be presented in the form:

$$G_{cl}(p)=\frac{G_{ol}(p)}{1+G_{ol}(p)}=V_{m,1+}\frac{pk_pV_{m,1+}+\frac{V_{m,1+}}{T_i}}{p^2+pk_pV_{m,1+}+\frac{V_{m,1+}}{T_i}} \tag{9}$$

Parameters of PI controller of SRF-PLL can be chosen by a comparison of closed loop transfer function of SRF-PLL and canonical form of the second order transfer function:

$$\frac{pk_pV_{m,1+}+\frac{V_{m,1+}}{T_i}}{p^2+pk_pV_{m,1+}+\frac{V_{m,1+}}{T_i}}=\frac{p2\zeta\omega_n+\omega_n^2}{p^2+p2\zeta\omega_n+\omega_n^2} \tag{10}$$

where ω_n is the natural frequency of the system, and ζ is the damping coefficient of the system. Based on the comparison between the left and right side of (10), PI controller parameters can be calculated using the following equation:

$$k_p=\frac{2\zeta\omega_n}{V_{m,1+}} \quad \wedge \quad T_i=\frac{V_{m,1+}}{\omega_n^2} \tag{11}$$

It is usual in scientific literature to tune SRF-PLL using the following parameters: $\zeta=\sqrt{2}/2$ and $\omega_n=2\pi 20$ [13].

4. REPETITIVE RIPPLE ESTIMATOR FILTER BASED PHASE-LOCKED LOOP

The initial repetitive ripple estimator in a phase-locked loop was introduced in [14]. Although the presented estimator was able to suppress oscillations in the control loop due to voltage imbalance or harmonics, the dynamic of the phase-locked loop was related to the parameters of the filter. In this paper the modification of the filter was done to have a minimal effect on the dynamics of PLL. The proposed repetitive ripple estimator filter is shown in Fig. 3. It consists of two gain blocks with gain k_r, one delay block and one Moving Average Filter (MAF). The transfer function of the proposed filter is:

$$\frac{\bar{v}_q}{v_q}=(1+k_r)\frac{1-e^{-pT_\omega}+\frac{1-e^{-pT_\omega}}{pT_\omega}}{1-e^{-pT_\omega}+\frac{1-e^{-pT_\omega}}{pT_\omega}+k_r} \tag{12}$$

where T_ω is the time delay in delay block and also the window of MAF, and k_r is the coefficient of repetitive ripple estimator.

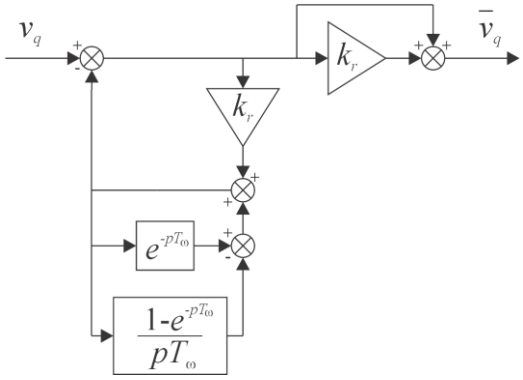


Fig. 3 Model of repetitive ripple estimator filter

The Repetitive Ripple Estimator Filter Phase-Locked Loop (RREF-PLL) proposed in this paper is presented in Fig 4. It requires minimum modification of SRF-PLL, because the repetitive ripple estimator filter is inserted at the output of the phase detector, before the PI controller and it requires no further modification of the phase-locked loop structure.

Using the Taylor series expansion and the first order Pade approximation [9], the linearized transfer function of (12) can be obtained in the form:

$$\left.\frac{\bar{v}_{g,q}(p)}{v_{g,q}(p)}\right|_{e^{-pT_\omega}\approx\frac{1-pT_\omega/2}{1+pT_\omega/2}} = (1+k_r)\frac{1+pT_\omega}{(1+k_r)+pT_\omega(1+k_r/2)} \tag{13}$$

It can be concluded that for small values of k_r, the linearized transfer function of the proposed filter is close to unity. The gain of the proposed filter for the DC component can be calculated as:

$$\left|\frac{\bar{v}_{g,q}(j\omega)}{v_{g,q}(j\omega)}\right|_{\omega=0} = 1 \tag{14}$$

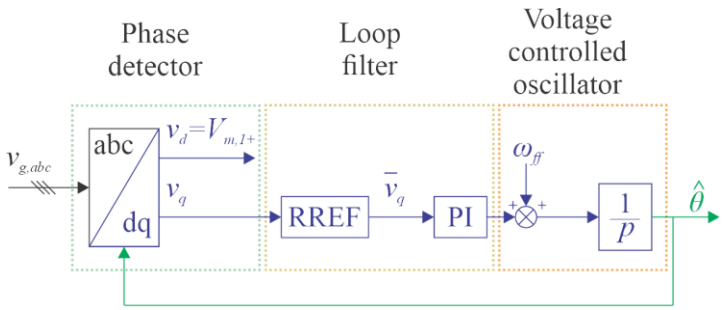


Fig. 4 Proposed Repetitive Ripple Estimator Filter PLL (RREF-PLL)

In Fig. 5 three models are presented for examination of the control structure:

- Large signal model that incorporates all nonlinearities in the control structure;
- Small signal model that incorporates a linearized version of all elements;
- Small signal model that omits dynamic of the proposed filter (for small values of k_r). This small signal model is identical to the small signal model of SRF-PLL.

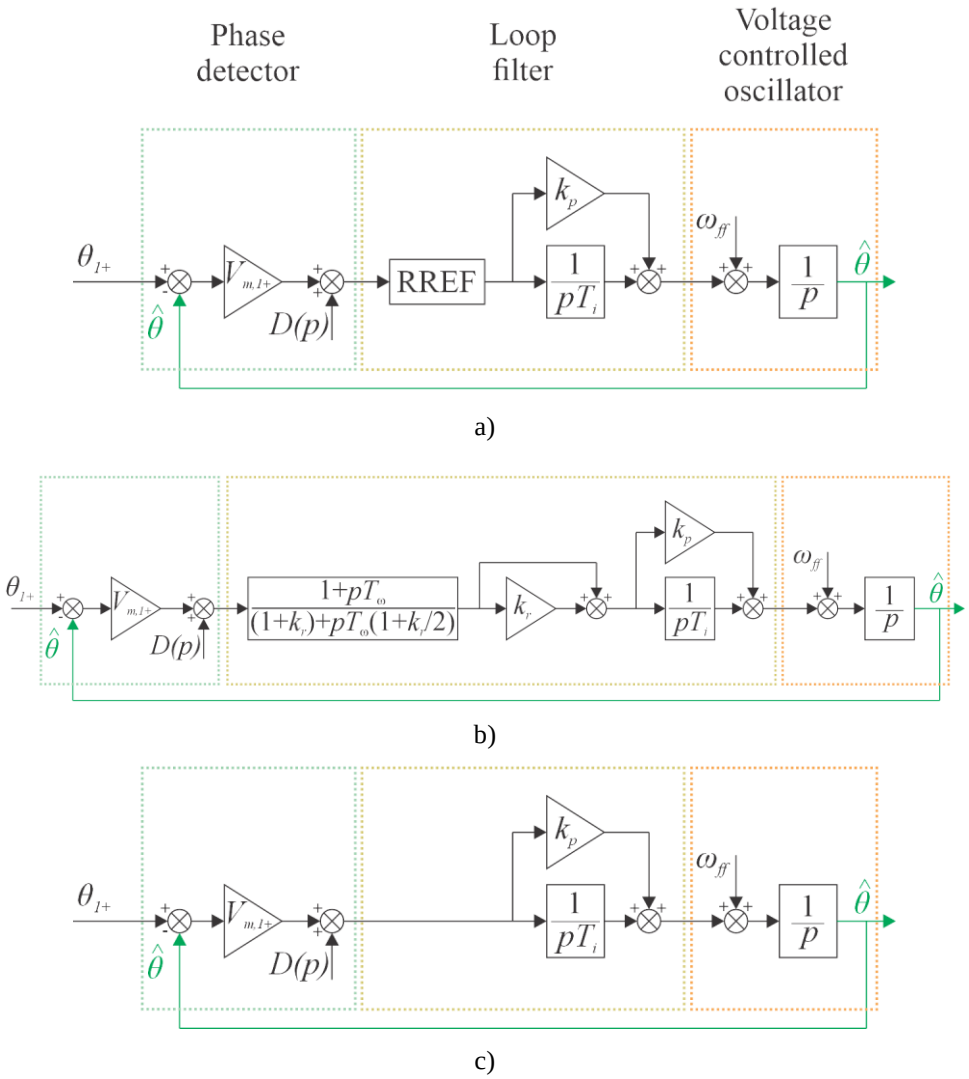


Fig. 5 Proposed RREF-PLL: a) large signal model; b) small signal model; c) small signal model for small k_r

Time delay in delay block and window of MAF T_ω is used for the suppression of the undesired oscillation in the control loop. It is well documented that MAF can suppress all

frequencies that are multiples of the window frequency ($f_\omega = 1/T_\omega$) [9]. With an appropriate T_ω a fundamental frequency for suppression can be selected, and all its multiples will also be suppressed.

The effect of k_r on filtering characteristics of the phase-locked loop can be observed in Fig 6. In the time period between 0.1 s and 0.2 s an unbalanced voltage sag without phase jump occurs that generates an oscillation in the PLL control structure. The proposed filter manages to suppress the induced oscillation. Lower values of k_r enable a more gradual suppression of disturbances in a signal. On the opposite side, higher values of k_r provide a more aggressive suppression of disturbances, but that can also result in abrupt jumps of the filtered signal. When $k_r = 0$ the filter has no effect (system behaves as SRF-PLL). The other characteristic of a filter is that it can inject disturbances once they are no longer available in the signal – the time it takes the filter to suppress oscillations is the time it needs to recover once oscillations are no longer present.

From Fig. 7 can be observed the dynamic response of the proposed RREF-PLL, along with its proposed large signal model and small signal model for different values of k_r. For the comparison test of the dynamic response, the following simulation experiment is conducted:

- In 0.1 s from the start, phase jump of 30 degrees occurs;
- In 0.2 s from the start, phase jump of 30 degrees in opposite direction occurs;
- In 0.3 s from the start, fundamental frequency jumps from 50 Hz to 55 Hz;
- In 0.4 s from the start, fundamental frequency jumps from 55 Hz to 50 Hz.

Based on the response from Fig. 7 it can be concluded that the large signal model is a good representation of RREF-PLL. Also, the response of the small signal model resembles SRF-PLL more for smaller values of k_r.

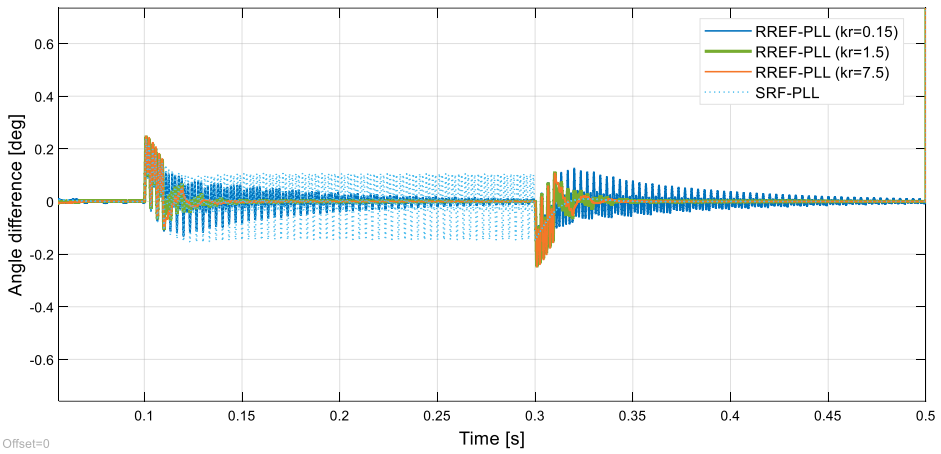
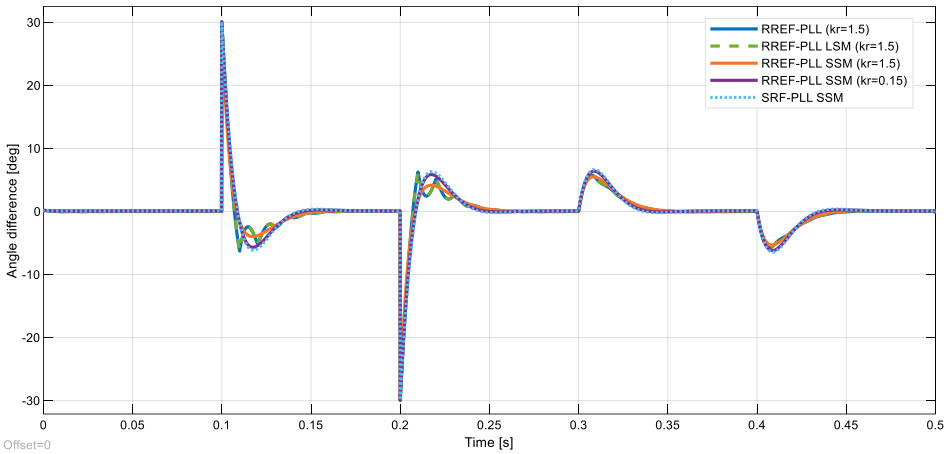
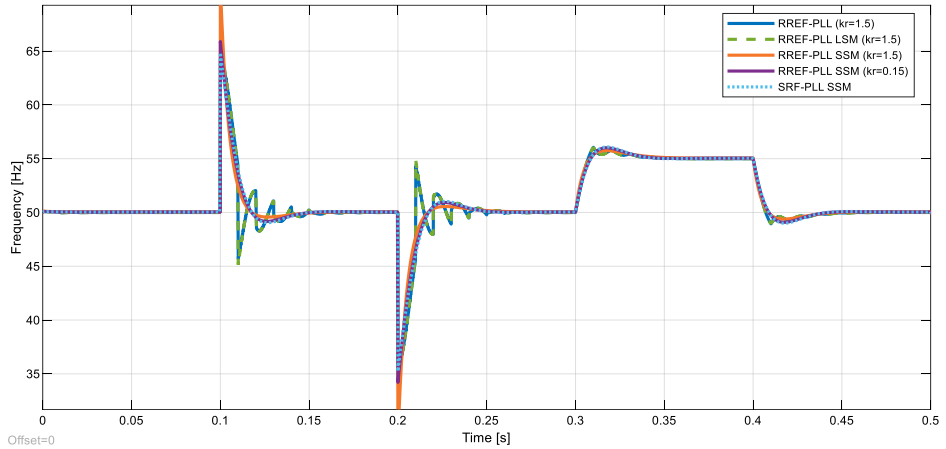


Fig. 6 Influence of parameter k_r on filtering characteristics of phase-locked loop



a)



b)

Fig. 7 Comparison of dynamic response of RREF-PLL, its proposed large signal model and small signal model with various values of k_r a) estimation of phase angle; b) estimation of frequency

The tuning procedure of all freely adjustable parameters of RREF-PLL can be deduced to the following steps:

- The parameters of PI controller can be calculated according to (11);
- The parameter T_ω is selected to suppress expected oscillations in the control loop;
- The parameter k_r is selected by trial and error according to the desired speed of oscillation suppression.

6. PERFORMANCE VALIDATION

Performance validation of the proposed RREF-PLL is done in simulation using MATLAB/Simulink R2024a. Proposed RREF-PLL is compared to SRF-PLL in the following set of tests:

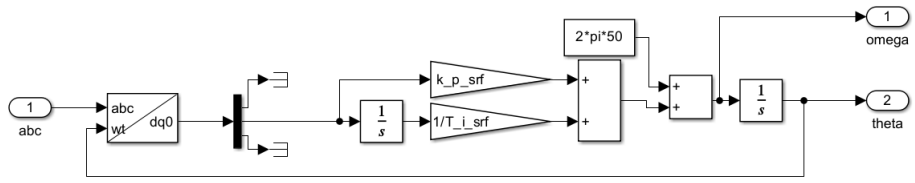
- Unsymmetrical voltage sag – in the specific case Voltage sag type B [15], with a sag dip of 30%;
- Voltage harmonics – upper limits of 5-th, 7-th and 11-th harmonic continuously permissible by EN 50160:2023.

The grid voltage amplitude and all freely adjustable parameters of PLLs are listed in Table 1.

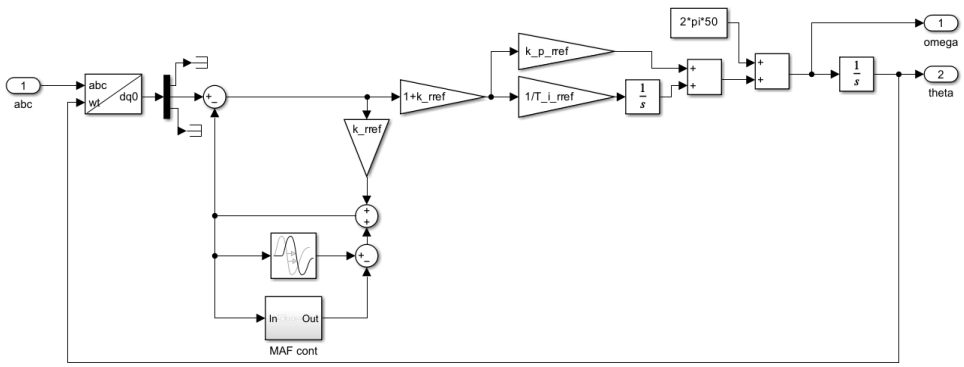
Table 1 Parameters of phase-locked loops

Algorithm\Parameter	$V_{m,1+}$	ζ	ω_n	k_p	T_i	T_ω	k_r
RREF-PLL	$230\sqrt{2}$	$\sqrt{2}/2$	$2\pi 20$	0.546	0.021	0.01	1.5
SRF-PLL	$230\sqrt{2}$	$\sqrt{2}/2$	$2\pi 20$	0.546	0.021	/	/

Details of PLL implementation in MATLAB/Simulink R2024a are shown in Fig. 8.



a)



b)

Fig. 8 Details of PLL implementation in MATLAB/Simulink R2024a: a) SRF-PLL; b) RREF-PLL

The voltage sag test is shown in Fig. 9. The sag transition was rectangular, and 30 degrees phase jump accompanied the sag. SRF-PLL exhibited undamped oscillations during sag on twice the fundamental frequency, while RREF-PLL successfully suppressed the oscillations and was able to provide the exact fundamental positive sequence voltage phase angle estimation.

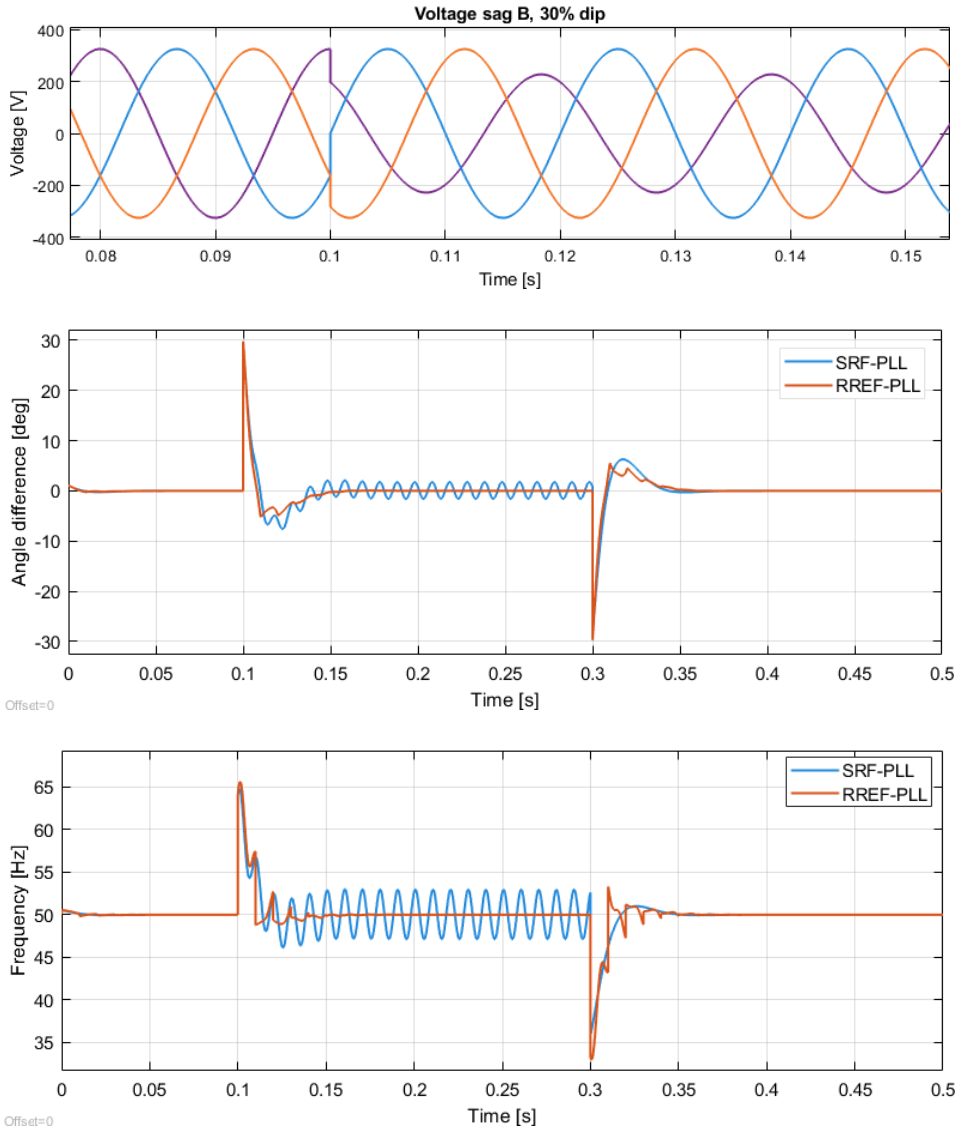


Fig. 9 Dynamic response of proposed RREF-PLL compared to SRF-PLL in the event of voltage sag

The voltage harmonics test is shown in Fig 10. As in the voltage sag test, SRF-PLL exhibits undamped oscillations during the period with harmonics. RREF-PLL iteratively suppressed harmonics within the time of about 50 milliseconds. About 50 milliseconds after the harmonics were terminated, RREF-PLL generated oscillations until it was able to provide an accurate prediction of the phase angle.

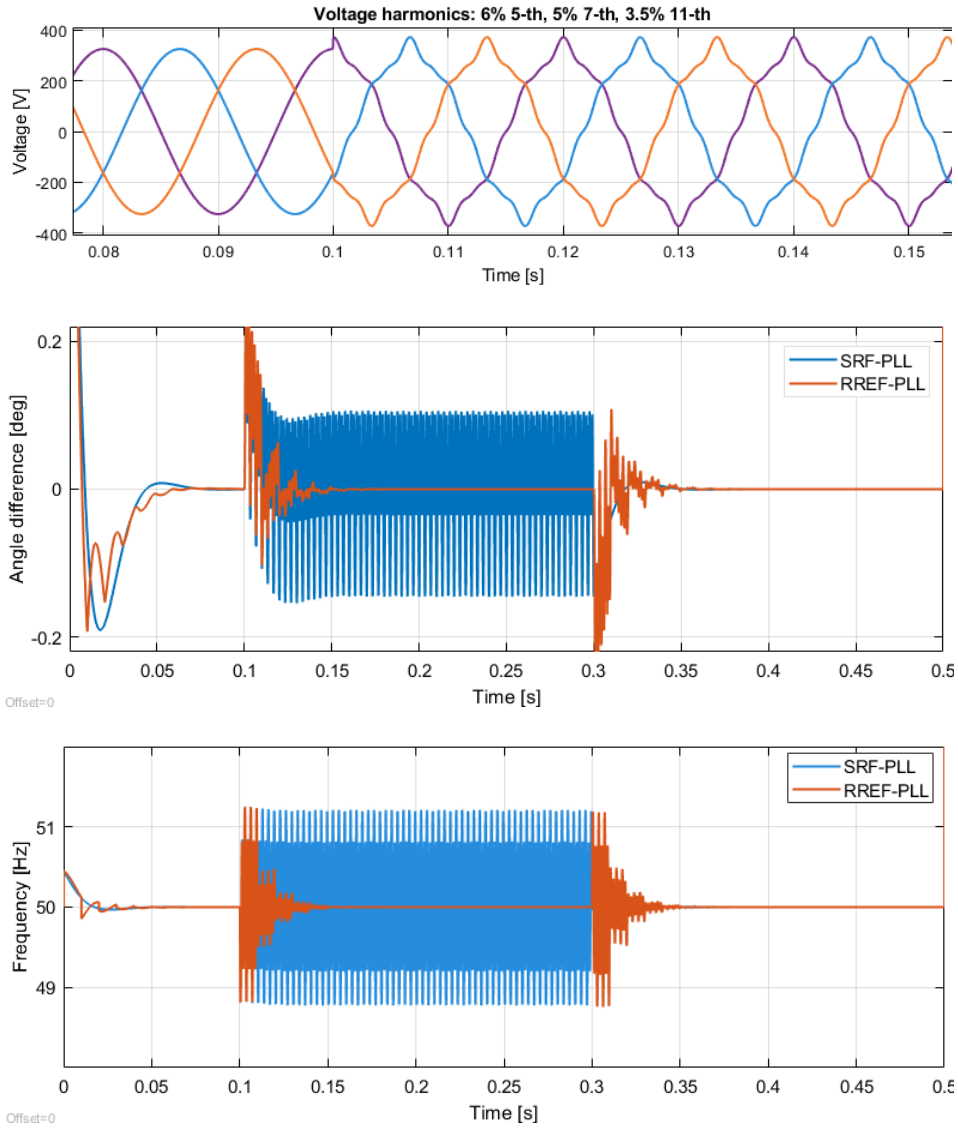


Fig. 10 Dynamic response of proposed RREF-PLL compared to SRF-PLL in the event of voltage harmonics

Abrupt variations of the phase angle estimation for large values of k_r does not make RREF-PLL suitable for coordinate transformations of vector-controlled grid-tie inverters, but rather for acquisition and monitoring algorithms. Smaller values of k_r make RREF-PLL suitable for coordinate transformations of vector-controlled grid-tie inverters, at the cost of disturbances in the estimated phase angle for a longer period than in the case of larger k_r. Also, smaller values of k_r can induce oscillations after their cause is eliminated in the measured voltages, that can lead to an unexpected behaviour of the device where the proposed RREF-PLL is implemented.

7. CONCLUSION

In this paper a novel phase-locked loop is presented based on the SRF-PLL and repetitive ripple estimator filter. A detailed design procedure was provided, accompanied by a proposed large signal model and a small signal model. The proposed repetitive ripple estimator filter provides unity gain for the DC component. For small values of k_r, parameters of the proposed RREF-PLL can be calculated as for the SRF-PLL. The parameter T_ω is selected to suppress expected oscillations in the control loop as for MAF-PLL. The effectiveness of the repetitive ripple estimator was shown in suppressing undesired oscillations originating from the voltage unbalance or voltage harmonics in the simulation.

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REFERENCES

[1] B. Qin, M. Wang, G. Zhang, and Z. Zhang, "Impact of renewable energy penetration rate on power system frequency stability," Energy Reports, vol. 8, pp. 997–1003, Nov. 2022. doi:10.1016/j.egyr.2022.05.261.

[2] B. Xu et al., "Stability Analysis of a hydro-turbine governing system considering inner energy losses," Renewable Energy, vol. 134, pp. 258–266, Apr. 2019. doi:10.1016/j.renene.2018.11.026.

[3] V. Boscaino et al., "Grid-connected photovoltaic inverters: GRID codes, topologies and control techniques," Renewable and Sustainable Energy Reviews, vol. 189, p. 113903, Jan. 2024. doi:10.1016/j.rser.2023.113903.

[4] W. Jarzyna, "A survey of the synchronization process of synchronous generators and Power Electronic Converters," Bulletin of the Polish Academy of Sciences Technical Sciences, pp. 1069–1083, Dec. 2019. doi:10.24425/bpasts.2019.131565.

[5] P. Gawhade and A. Ojha, "Recent advances in synchronization techniques for grid-tied PV system: A Review," Energy Reports, vol. 7, pp. 6581–6599, Nov. 2021. doi:10.1016/j.egyr.2021.09.006.

[6] N. Jaalam, N. A. Rahim, A. H. A. Bakar, C. Tan, and A. M. A. Haidar, "A comprehensive review of synchronization methods for grid-connected converters of renewable energy source," Renewable and Sustainable Energy Reviews, vol. 59, pp. 1471–1481, Jun. 2016. doi:10.1016/j.rser.2016.01.066.

[7] M. Ciobotaru, R. Teodorescu, and F. Blaabjerg, "A new single-phase PLL structure based on second order Generalized Integrator," 2006 37th IEEE Power Electronics Specialists Conference, Jun. 2006. doi:10.1109/pesc.2006.1711988

[8] P. Rodriguez et al., "Double synchronous reference frame PLL for power converters control," 2005 IEEE 36th Power Electronics Specialists Conference, vol. 4, pp. 1415–1421, 2005. doi:10.1109/pesc.2005.1581815

[9] S. Golestan, M. Ramezani, J. M. Guerrero, F. D. Freijedo, and M. Monfared, "Moving average filter based phase-locked loops: Performance Analysis and Design Guidelines," IEEE Transactions on Power Electronics, vol. 29, no. 6, pp. 2750–2763, Jun. 2014. doi:10.1109/tpel.2013.2273461

[10] C. L. Fortescue, “Method of symmetrical co-ordinates applied to the solution of Polyphase Networks,” Transactions of the American Institute of Electrical Engineers, vol. XXXVII, no. 2, pp. 1027–1140, Jul. 1918. doi:10.1109/t-aiee.1918.4765570

[11] “Synchronous reference frame PLL,” Enhanced Phase-Locked Loop Structures for Power and Energy Applications, pp. 133–145, Mar. 2014. doi:10.1002/9781118795187.ch6

[12] Z. Dai et al., “Global Stability Analysis for synchronous reference frame phase-locked loops,” IEEE Transactions on Industrial Electronics, vol. 69, no. 10, pp. 10182–10191, Oct. 2022. doi:10.1109/tie.2021.3125655

[13] Y. F. Wang and Y. Wei Li, “Analysis and digital implementation of cascaded delayed-signal-cancellation PLL,” IEEE Transactions on Power Electronics, vol. 26, no. 4, pp. 1067–1080, Apr. 2011. doi:10.1109/tpel.2010.2091150

[14] F. Filipovic, M. Petronijevic, N. Mitrovic, B. Bankovic, and V. Kostic, “Application of repetitive ripple estimator in synchronization of three phase grid tie inverters,” 2019 20th International Symposium on Power Electronics (Ee), pp. 1–6, Oct. 2019. doi:10.1109/pee.2019.8923405

[15] M. H. Bollen, Understanding Power Quality Problems, 1999. doi:10.1109/9780470546840