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POGO PIN PARASITIC IMPEDANCE CHARACTERISATION AND INFLUENCE ON PMIC SEMICONDUCTOR EVALUATION PROCES

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Dejan Milošević, Miodrag Arsić, Dragan Denić, Dragan Živanović

University of Niš, Faculty of Electronic Engineering, Niš, Republic of Serbia

Abstract. *During the semiconductor evaluation of modern Power Management Integrated Circuit (PMIC) devices, high quality Zero-Insertion-Force (ZIF) sockets must be used in order to measure many semiconductor parts with a single dedicated hardware. The most critical part of socket is contact between the device terminal and PCB. There are couples of technology processes that can provide solid contact between the device and the rest of the circuit, but the most common technology uses so called Pogo-pin, also called spring pin. Pogo pin must have as small as possible parasitic impedance, since the signal frequency and the signal power transfer between the PMIC terminal and the rest of the circuit must be without distortions, in order to obtain correct measurement results of tested devices. In some cases, influence of Pogo-pin parasitic impedance can lead to the partial damage of the device internal structure. This article should point to the potential problems using simulation results and should describe the simple procedure of Pogo-pin impedance characterization using network analyzer with appropriate aperture. Couples of measurements results from different Pogo-pin suppliers are also shown in this example with some practical results.*

Key words: *PMIC semiconductor, Pogo-pin, Parasitic Impedance, Simulation, Network analyzer, ZIF socket*

1. INTRODUCTION

Connecting modern Ball Greed Array (BGA) devices with more than 200 terminals with the application circuit using ZIF socket is not an easy task, since introducing additional parasitic impedance could lead to the device damage. Socket manufacturers usually have measurement reports [1, 2], mostly done by using S parameters for AC analyze, like Ironwood. Unfortunately these reports do not cover all the Pogo-pin types,

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Corresponding author: Dejan Milošević
University of Niš, Faculty of Electronic Engineering, Niš, Republic of Serbia
E-mail: dgenije@yahoo.com

so for the new development customer needs to relay on the simulation data which is not always correct. Pogo pin spice model was introduced by Emulation technology in 2009 [3], consists of standard π cell with inductor in serial and 2 capacitors to the reference node, as on Fig. 1.

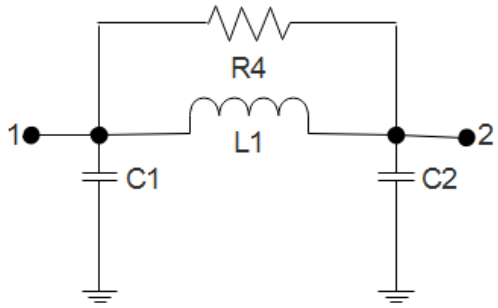

Fig. 1 Pogo-pin spice model by Emulation technology is represented by the standard P cell with addition of bypass resistor

Resistance R4 approximates the thermal losses. Slightly modified model was given by Ironwood [1] as on Fig. 2.

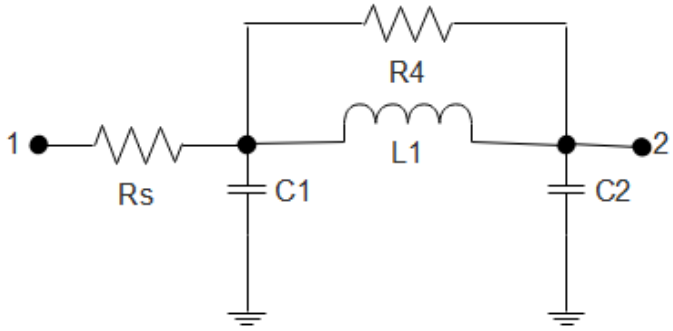

Fig. 2 Pogo-pin spice model by Ironwood, introduces serial small value resistor to the standard P cell

Small value of Rs present serial parasitic resistance and in most of the cases is not taking into account during characterization. The only exception would be the high current, low voltage flow, where corresponding to the basic Ohm law, small value of Rs can have significant effect.

Many of the articles focused on durability test, like the Pogo-pin characteristics after many mating cycles [4] as on Fig. 3. Since such a test requires large amount of time and different setup, this will not be in focus of this article.

In this paper we present very simple way of Pogo-pin parasitic inductance measurement, since this is very important for a proper evaluation of PMIC semiconductor devices.

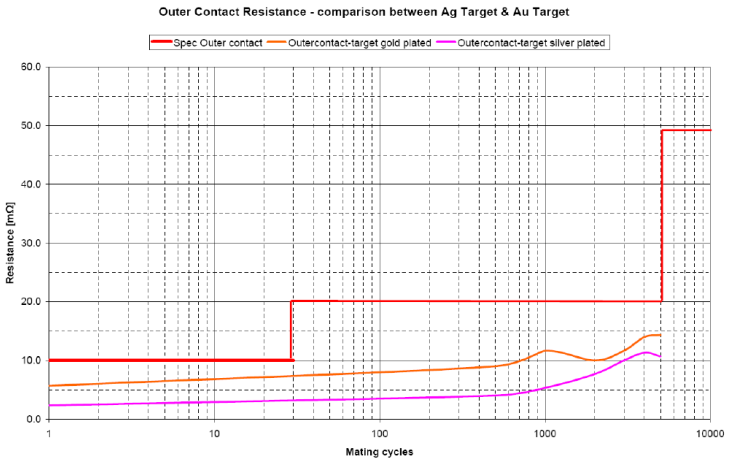

Fig. 3 Contact resistance durability test represents the changes in the Pogo pin resistance due to the mating cycles

2. Equivalent Schematic of DC-DC Convertor Circuit with Pogo-pin and Simulation of Pogo-pin Influence on the Output Stage

Considering equivalent spice representation of Pogo pin shown on Fig. 1, and taking into account that the value of R4 is too high for circuit interaction, the structure of DC-DC convertor in the ZIF socket with Pogo-pins can be presented as on Fig. 4. Note that the parasitic capacitors are also not taken into account since their values are too small for our frequency of interest, which is up to 100MHz.

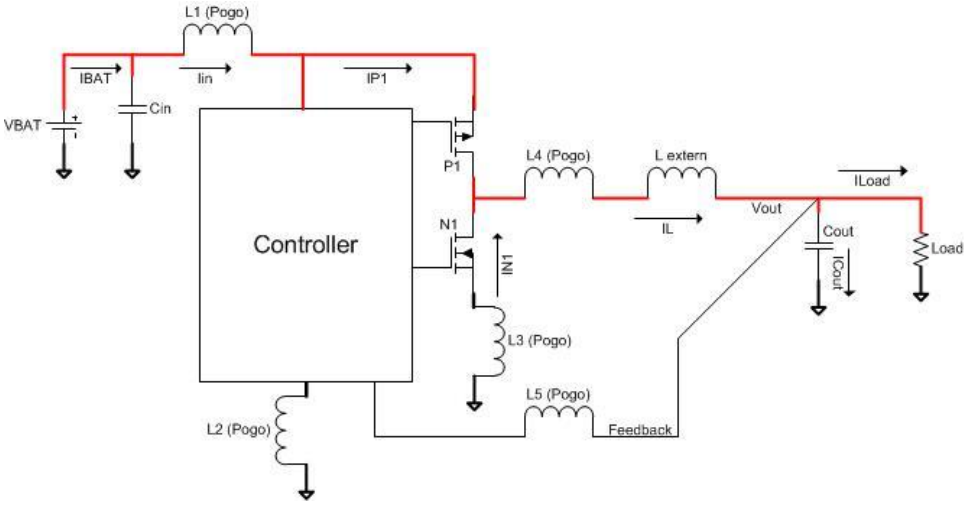

Fig. 4 Influence of Pogo pin inductance on standard buck configuration, presented by L1, L2, L3, L4 and L5

L1 and L3 inductors influence circuit to behave as a partial boost convertor. Output stage, consists of N-MOS and P-MOS pair, and works as alternating switch controlled by the controller gate connection as shown on Fig. 5 [5].

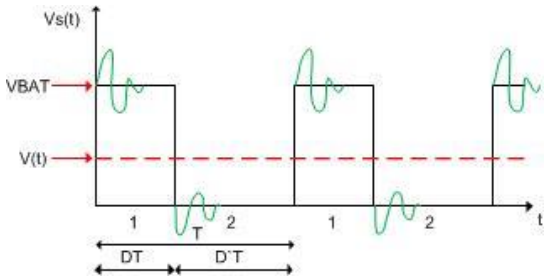

Fig. 5 Voltage waveform on N-MOS and P-MOS drain, measured with high parasitic inductance socket

After MOSSFET stops conduction, on SOURCE node rapid increase of the potential to reference for P channel, or decrease of potential for N channel can be seen (as on Fig. 5 Note that the overshoot and undershoot can be as high as 1V with VBAT set to 4V!!). Taking into account that output stage MOSFETs can be integrated into the 250µm (or lower) technology device, which can sustain not more than 6V of Vds, or Vgs, using high inductance Pogo-pin can cause output stage damage when the supply voltage VBAT is higher than 4V, which is the real case for single Li cell supply.

L2 parasitic inductor might have some influence on the stability of the pulse width generator, but this is not the subject of current study.

L4 influence is not important since in serial, much higher inductance is connected [6]. In this case, small value of Rs (see Fig. 2) might have some influence on degradation of convertor efficiency.

L5 influence reaction of the feedback compensation circuit. Ideal switching convertors must have very fast reaction time on load transient conditions. Having L5 parasitic inductor in serial with the capacitive feedback input creates low pass filter which slows down response time, producing very poor characteristics during transient load conditions.

2.1. Simulation of Pogo-pin parasitic inductance influence

Pogo-pin parasitic influence can be very well confirmed using Cadence simulation tool. On Fig. 6, real design model of Buck convertor output stage was used, consists of pair of MOSFET transistors and the driver circuit, simulating pulse width modulation process. On the source side of P-MOS transistor, we added small 2nH inductance [7] that represents real value of Pogo-pin parasitic inductance. Output inductor was simulated by the ideal inductor in serial with small resistor representing parasitic resistance. Real capacitor is simulated with the ideal capacitor in serial with the small value of resistance, which represents real capacitor impedance on the capacitor resonance point. Note that the parasitic Pogo-pin inductance is not introduced to the controller supply, since the effect is negligible.

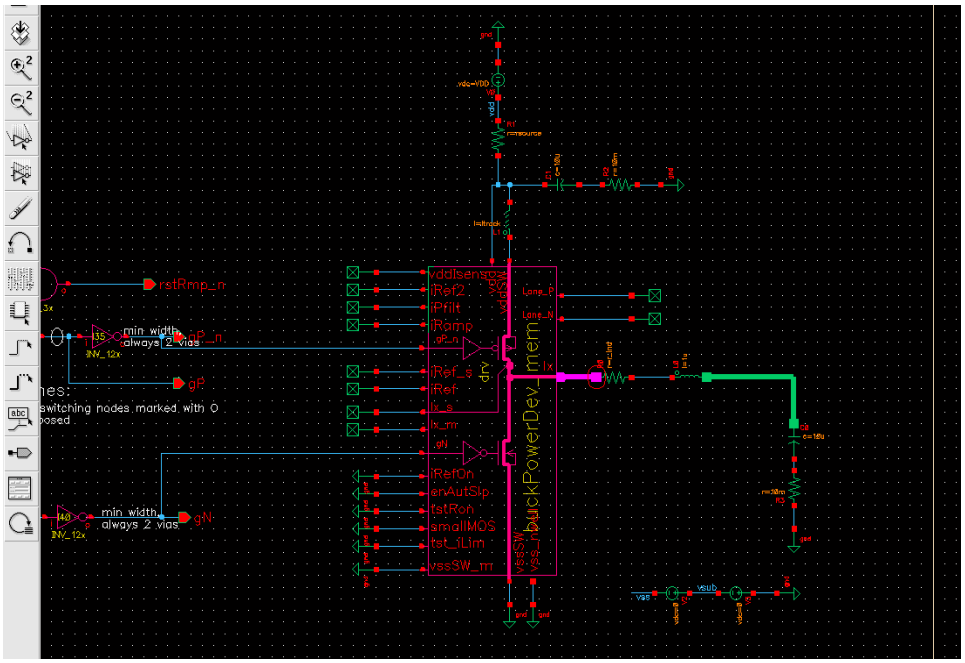

Fig. 6 Simulation schematic of Pogo pin (2nH parasitic inductance) influence on P-MOS source side without load

As explained in previous chapter, semiconductor devices used in modern integrated circuits have certain limitations regarding voltage between Drain and Source terminals. When being used under light load, or without load, output inductance L0 will build negative current as long as the N-MOS is switched on (presented as IL current on Fig. 4). There must be the time when neither N-MOS, nor P-MOS are conducting, in order to compensate switching time of the transistors and to prevent cross-conduction. When turning the N-MOS off, the output inductor current will not stop (from the physics law it is impossible), causing the voltage on the point between two MOSFET Drains (called also switching node, or Lx node) to jump drastically. As the P-MOS is still off a peak of approximately VDD+0.7V is expected, where VDD presents the simulation supply voltage source. 0.7V is explained by the voltage drop on the body diode integrated into the MOSFETs used for the buck output stage.

However, a parasitic inductance we added into the simulation to represent Pogo-pin, will introduce another potential difference in serial with voltage drop that will act against this current flow. Consequently the voltage on the switching node will be VDD+0.7V+VLpogo which are strongly dependent of the value of the Pogo pin parasitic inductance.

The simulation results below (Fig. 7), shows the differences of the waveform on Lx node with (purple graph) and without (orange graph) influence of the Pogo-pin parasitic inductance. Green graph presents the output voltage waveform, while the red graph presents inductor current.

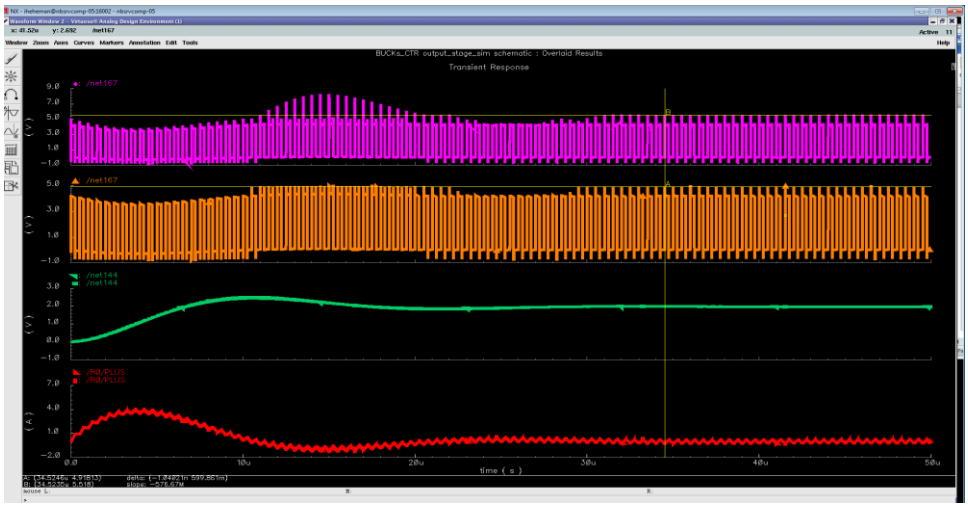

Fig. 7 Simulation results present Lx node with/without parasitic influence, output voltage and inductor current. Purple is with Pogo pin inductance influence

At the start up the simulation, VDD (main supply power) is applied and the Buck is activated. The start-up inductor current increases in order to establish the steady output voltage (green). Undershoots and overshoots of 0.7V are present on both of the graphs, but the simulation case with the Pogo-pin impedance applied shows additional overshoot due to the voltage drop on the parasitic inductance. From the simulation results, we can conclude that even the small Pogo parasitic inductance of 2nH (which is quite realistic case), can cause Lx node spikes up to 7V, which could potentially damage the MOSFETs.

It would be useful to state that current simulation case is also valid to the PCB trace simulation influence, while the impedance structure of the trace is approximately the same as the Pogo-pin structure.

3. MEASUREMENT SETUP AND RESULTS

Most of the Pogo-pins are made with the spring inside, or outside the pin body, as shown on Fig. **8**. In the real application, spring is compressed, providing us the smaller length. Smaller length of conducting surface brings the smaller parasitic impedance. Unfortunately during the network analyze measurement; we cannot compress Pogo-pin in the same way, introducing slightly different measurement result.

Pogo-pin impedance measurement can be done by using Network analyzer and appropriate aperture. We successfully performed the measurement using Agilent E5061B network analyzer, 16092A spring clip fixture and 16201A terminal adapter as on Fig. 9.

Fig. 8 Pogo pin internal structure

Fig. 9 Measurement setup includes network analyzer and appropriate fixture for reflection measurements

Frequency range is from 1 to 100MHz. Before we start any measurement, terminal adapter and fixture must be calibrated using open and short application provided by Agilent. Following steps needs to be applied:

- Set the X-axis to the log sweep from 1MHz to 100MHz
- Set the IFBW to 100Hz
- Set the measurement parameter to impedance magnitude |Z|
- Set the Y-axis to the log scale from 1 ohm to 10 MΩ
- Perform the calibration at the 7mm connector plane of the 16201A terminal adapter (with disconnected fixture)
- Connect the 16092A fixture on the 16201A terminal adapter
- Calibrate 16092A fixture
- Insert Pogo-pin (very sensitive operation, since the dimensions of Pogo-pins are really small. Great care must be taken in order not to damage measured pin)
- From "Analyze" MENY, chose calculate command and display the parasitic parameters on the display

Fig. 10 Spring clip fixture and terminal adapter used for Pogo pin impedance – frequency measurement

Fig. 11 Impedance – frequency characteristic of Pogo pin from Supplier 1 measurement result, measured with Agilent E5061B network analyser

From the network analyzer, following results are delivered:

- **Lpogo** (L1 on the equivalent schematic) = **1.878nH**
- **Rs** (serial active impedance) = **50.5mΩ**

Measurement results of Pogo-pin from "Supplier 1" are shown on Fig. 11. Measured inductance is above **1nH** (limit which we consider as a safe value). "Supplier 1" still did not provide reports for their Pogo-pin.

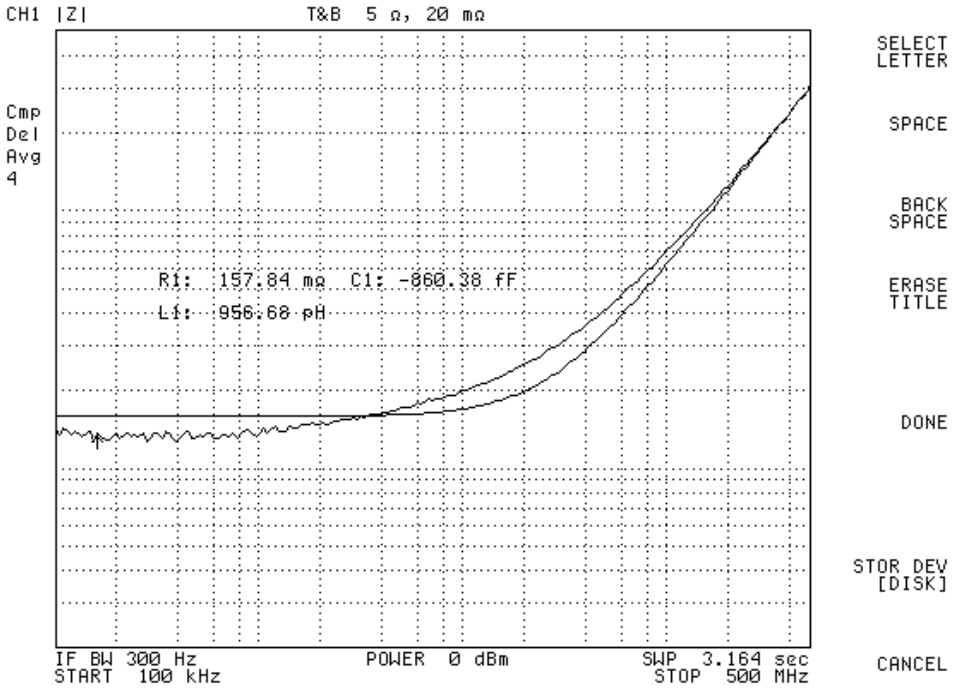

Fig. 12 Impedance – frequency measurement of Pogo pin with extended frequency range from 100kHz to 500MHz (Supplier 2)

ZIF socket with Pogo-pin from "Supplier 2" has significantly lower parasitic inductance **(0.956nH)** and can be considered "safe" for validation and stress tests (extended temperature and current load, with input power above recommended range). "Supplier 2" reports the value of **1nH**, which correlate with measurement in our laboratory.

ZIF socket with Pogo-pin from "Supplier 3" has a parasitic inductance of **0.668nH** and can be also considered "safe" for validation and stress tests. "Supplier 3" reports the value of **0.6nH**, which correlate with measurement in our laboratory.

Note that for the Fig. 12 and Fig. 13, inverted color scheme is used from the network analyzer setup, as a printer-friendly option.

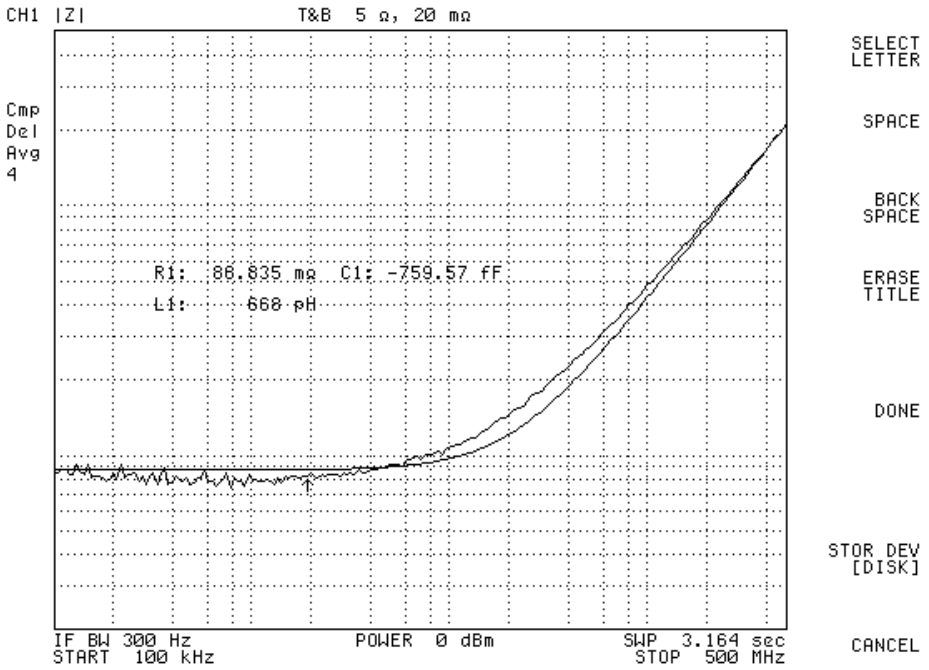

Fig. 13 Impedance – frequency measurement of Pogo pin characteristics from "Supplier 3"

4. CONCLUSION

PMIC integrated circuits are complex devices consists of many different power blocks like DC-DC convertors and LDOs, equipped with standard interfaces like I2C, or SPI and different dedicated digital and analog lines [8].

Not all the manufacturers are able to quickly provide requested data for the Pogo-pin used for ZIF socket ("Supplier 1" example). Since the design-to-market time is always critical, project leader is forced to order large quantity of sockets without really knowing the socket characteristics (price of one ZIF socket is usually more than 1000 EUR and the usual quantity is more than 200 pcs.), which can lead to the measurements mistakes and very often semiconductor destruction during the test.

Contribution of in-house measurement of Pogo-pin parasitic impedance can be seen from the following example: Measurement is performed on 3 different supplier samples and the results are matching with "Supplier 2" and "Supplier 3" data sheet results. ZIF socket from "Supplier 1" was considered to be used in the next design validation, as a "cheaper" variant, but due to the bad parasitic characteristics it would be rejected.

Simple method described in previous chapter can give enough accurate measurement to influent decision which ZIF socket supplier should be considered for project and drastically lower the design cost.

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