

AN APPROACH TO DESIGN OF DC-DC BOOST CONVERTER WITH DIGITAL CONTROL

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Abstract. *This paper deals with the design of digital controller for DC-DC boost converter. This controller is a combination of a generalized minimum variance control and one-step-delayed disturbance estimator. The generalized minimum variance control algorithm design is based on the input/output converter model. It should provide the output voltage stability, whereas the disturbance estimator increases the robustness and the steady-state accuracy of converter in the presence of input voltage and load resistance variations. With these control techniques, the converter can achieve better power efficiency. Finally, the effectiveness of the proposed design procedure is verified by a digital simulation, showing satisfactory DC-DC boost converter performances.*

Key words: *generalized minimum variance control, sliding mode, equivalent control, one-step-delayed disturbance estimator*

1. INTRODUCTION

In modern devices, such as industrial applications (spacecraft power systems, DC motor drives, telecommunication equipment) or personal applications (PCs, office equipment, electrical appliance), the need for power supplies with high performance of regulation is increasing in practice because of the stochastic disturbances, so the control system must be more reliable, stable, and economic. The DC-DC boost converters are power supplies, which are used in applications where the required output voltage needs to be higher than the source (input) voltage.

Most of control methods, applied in converter design, are based on pulse-width-modulation (PWM) fixed frequency techniques, also known as a duty cycle controls [1]. The implementation of PWM techniques in control of DC-DC boost-type converter,

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operating in continuous conduction mode (CCM), may cause the appearance of right-half-plane-zero (RHPZ) in its duty-cycle-to-output-voltage transfer function [2,3]. To deal with input voltage and load resistance variations, robust control techniques are preferable for DC-DC converter design. Sliding mode (SM) control [4-6] belongs to this class of control algorithms. The system dynamics with SM controller is equivalent to the system dynamics with PWM controller [7] so that SM equivalent control [8, 4] u_{eq} is equal to the duty cycle control signal d . It has been proven in [9] that a generalized minimum variance (GMV) control corresponds to digital SM equivalent control, when the controller design is based on input/output plant models. On the other hand, GMV control algorithm [10] was first introduced by Clarke to control non-minimum phase systems. This qualifies GMV control as a good candidate for digital control of DC-DC boost converter.

In this paper, we present a digital control designed by using the input-output model of boost converter in the form of a discrete-time transfer function, which eliminates the need for additional current sensor. This means that the measuring of inductor current is not mandatory. The proposed control is the combination of GMV control algorithm and one-step-delayed disturbance estimator [9,11,12]. GMV control is suggested herein to cope with RHPZ of duty-cycle-to-output-voltage transfer function and to enable the controller design based only on converter output voltage measuring. To the authors' knowledge, there are only few papers dealing with the controller design for DC-DC converters based on their input/output models [13,14].

The paper is organized as follows: The model of DC-DC boost converter in discrete-time domain is derived in Section 2. Based on this model, the digital controller is designed in Section 3 for this type of converter. The results of digital simulation, which validate the proposed approach, is discussed in Section 4. Section 5 contains some concluding remarks.

2. MODEL OF DC-DC BOOST CONVERTER

The diagram of boost converter with the digital controller is presented in Fig. 1. In order to design digital control input, the DC-DC boost converter model is derived first as the discrete-time transfer function, which is obtained from the state-space model given in [15].

In Fig. 1, L , C_k and R_L denote an inductance, a capacitance and a load resistance of the converter, whereas i_L , i_c , i_{out} are inductor, capacitor, and output (load) currents, respectively. Reference, input and output voltages are denoted by V_{ref} , v_{in} , v_{out} , respectively, a sensor gain is marked by β , and u represents the signal driving the power switch S_w . It is assumed that the boost converter operates in CCM. By choosing the output voltage and its time-derivative as the state coordinates ($x_1=v_{out}$, $x_2=dv_{out}/dt$), the linearized small signal state-space model of boost converter in continuous-time domain is obtained in the form of [15]:

$$\begin{aligned} \dot{x}(t) &= \begin{bmatrix} 0 & 1 \\ 0 & -\frac{1}{R_L C_k} \end{bmatrix} x(t) + \begin{bmatrix} 0 \\ \frac{V_{in} - V_{out}}{L C_k} \end{bmatrix} u(t), \\ y(t) &= [\beta \quad 0] x(t), \end{aligned} \quad (1)$$

where V_{in} and V_{out} are the boost converter input and output nominal voltages, and the appropriate transfer function model is:

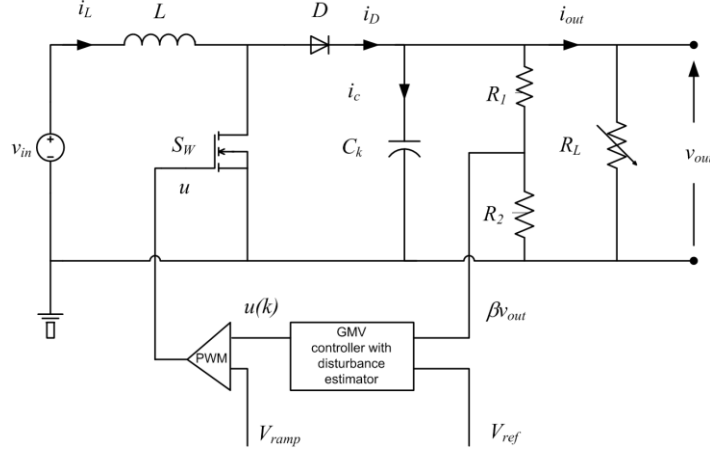


Fig. 1 Boost converter with digital controller.

$$W_{boost}(s) = \frac{Y(s)}{U(s)} = \frac{\beta(V_{in} - V_{out})}{s^2 + \frac{1}{R_L C} s}. \quad (2)$$

Under the assumption that $u(t) = u(kT)$, $kT < t < (k+1)T$, where k is a time instant and T is a sampling period, the discrete-time input-output model of boost converter can be written as:

$$y(k+1) = \frac{B(z^{-1})}{A(z^{-1})} u(k), \quad (3)$$

where z^{-1} is the unit delay i.e. $z^{-1} = e^{-sT}$, s is a complex variable and $\bullet(k) = \bullet(kT)$. Due to the input voltage and load resistance variations, the polynomials $A(z^{-1})$ and $B(z^{-1})$ are expressed in the following form:

$$A(z^{-1}) = A_n(z^{-1}) + \Delta A(z^{-1}), \quad B(z^{-1}) = B_n(z^{-1}) + \Delta B(z^{-1}), \quad (4)$$

where $A_n(z^{-1})$, $B_n(z^{-1})$, $\Delta A(z^{-1})$ and $\Delta B(z^{-1})$ denote the polynomials with nominal and perturbed values of boost converter parameters, respectively. Therefore, the equation (3) can be rewritten in the next form:

$$y(k+1) = \frac{B_n(z^{-1})}{A_n(z^{-1})} u(k) + \frac{1}{A_n(z^{-1})} h(k), \quad (5)$$

where:

$$h(k) = \Delta B(z^{-1}) u(k) - \Delta A(z^{-1}) y(k+1) \quad (6)$$

is considered as a disturbance caused by the input voltage and load resistance variations. The latter model will be used for design purposes of the digital controller.

3. DIGITAL CONTROLLER DESIGN PROCEDURE

The controller should ensure that the sensed output voltage $y(k)=\beta v_{out}(k)$ is stable, constant and equal to some reference voltage $V_r(k)=V_{ref}$ in the presence of input voltage v_{in} and load resistance R_L variations. To reach this goal, GMV control is suggested herein due to its analogy to digital equivalent control approach, as mentioned earlier in this paper:

$$u(k) = -\frac{F(z^{-1})y(k) - C(z^{-1})V_r(k+1) + E(z^{-1})h(k-1)}{E(z^{-1})B_n(z^{-1}) + Q(z^{-1})}, \quad (7)$$

where $C(z^{-1})$ is a polynomial with all zeros inside the unit disk of z -plane and $Q(1)=0$. $E(z^{-1})$ and $F(z^{-1})$ are solutions of the so-called Diophantine equation:

$$C(z^{-1}) = E(z^{-1})A_n(z^{-1}) + z^{-1}F(z^{-1}). \quad (8)$$

To cope with (6), one-step-delayed disturbance estimator defined by:

$$h(k-1) = A_n(z^{-1})y(k) - B_n(z^{-1})u(k-1), \quad (9)$$

is introduced in the control law (6). This will lead to the minimization of variance of a variable:

$$s(k+1) = C(z^{-1})(y(k+1) - V_r(k+1)) + Q(z^{-1})u(k), \quad (10)$$

also known as a switching function of digital sliding mode control, whose design is based on input/output plant model [9,12]. Substituting (7) in (5), taking into account (8), the $O(T^2)$ accuracy of (10) is attained, i.e.:

$$s(k+1) = E(z^{-1})(h(k) - h(k-1)) = O(T^2) \quad (11)$$

The closed-loop dynamics is directly derived from (5) and (10) in the form of [12]:

$$y(k) = \frac{B_n(z^{-1})C(z^{-1})V_r(k) + B_n(z^{-1})s(k) + Q(z^{-1})h(k-1)}{B_n(z^{-1})C(z^{-1}) + A_n(z^{-1})Q(z^{-1})}, \quad (12)$$

It is obvious from (12) that, in order to guarantee the system stability, all roots of equation $B_n(z^{-1})C(z^{-1}) + A_n(z^{-1})Q(z^{-1}) = 0$ should be inside the unit disk in the z -plane, and the pairs $(B_n(z^{-1}), Q(z^{-1}))$, $(C(z^{-1}), A_n(z^{-1}))$ and $(C(z^{-1}), Q(z^{-1}))$ should not have common zeroes outside this disk. The system steady-state accuracy can be obtained from (12) for $z=1$ and $Q(1)=0$ as:

$$y(\infty) = V_r(\infty) + \frac{1}{C(1)}s(\infty). \quad (13)$$

As $s(k+1)$ is $O(T^2)$, in accordance with (13), the steady-state converter accuracy will be within $O(T^2)/C(1)$ boundaries.

4. SIMULATION RESULTS

The validation of the proposed control algorithm for DC-DC boost converter is done by using digital simulation and the results are presented in this section. The nominal values of converter parameters are given in Table 1.

Table 1 Boost converter parameter nominal values

Description	Parameter	Value
Input voltage	V_{in}	12 V
Desired output voltage	V_{out}	24 V
Capacitance	C_k	1470 μ F
Inductance	L	330 μ H
PWM frequency	f_{pwm}	7.874 kHz
Sampling period	T	1 ms
Minimum load resistance	R_{L_min}	22.67 Ω
Maximum load resistance	R_{L_max}	68 Ω

Based on these values, the discrete-time model of boost converter (5) is determined for $T=1$ ms by $A_n(z^{-1})=1-1.9802z^{-1}+0.9802z^{-2}$ and $B_n(z^{-1})=1.3515-1.3425z^{-1}$. Then, the parameters of GMV controller are selected and calculated as: $C(z^{-1})=1-1.067z^{-1}+0.2846z^{-2}$, $Q(z^{-1})=0.05(1-z^{-1})$, $E(z^{-1})=1$, $F(z^{-1})=0.9132-0.6956z^{-1}$ and $\beta=0.1$. The switching frequency of PWM is $f_{pwm}=7.874$ kHz so that the influence of RHPZ in duty-cycle-to-output-voltage transfer functions is significantly suppressed, but at the cost of lower bandwidth [2].

In order to show load and line regulation properties of the proposed DC-DC boost converter with GMV control incorporating disturbance estimator, the step load changes from $R_L=68 \Omega$ to $R_L=34 \Omega$, from $R_L=34 \Omega$ to $R_L=22.67 \Omega$, and from $R_L=68 \Omega$ to $R_L=22.67 \Omega$ and *vice versa* are applied at three different input voltage values: minimum ($V_{in}=10.5$ V), nominal ($V_{in}=12$ V) and maximum ($V_{in}=13.5$ V). The step load variations occur at 0.5 s and 1.5 s time instants. The output voltage v_{out} waveforms are depicted in Figs. 2-4 both for GMV control without and with disturbance estimator.

The digital simulation results show that the use of disturbance estimator is mandatory in order to obtain the robust performances of DC-DC boost converter. GMV controller with disturbance estimator gives better steady-state accuracy, which means that it will provide zero error tracking of the reference input signal, both in the case of the input voltage and the load resistance variations. The implementation of the GMV with disturbance estimator has the same effect as adding additional integral term in control algorithm [9].

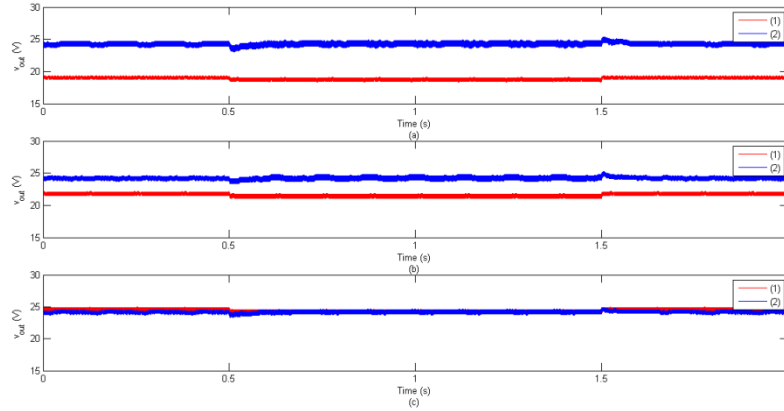


Fig. 2 The output voltage v_{out} waveforms of DC-DC boost converter with GMV control law without (1) and with (2) disturbance estimator alternating between load resistance 68Ω and 34Ω and operating at $V_{in} = 10.5 \text{ V}$ (a), $V_{in} = 12 \text{ V}$ (b) and $V_{in} = 13.5 \text{ V}$ (c).

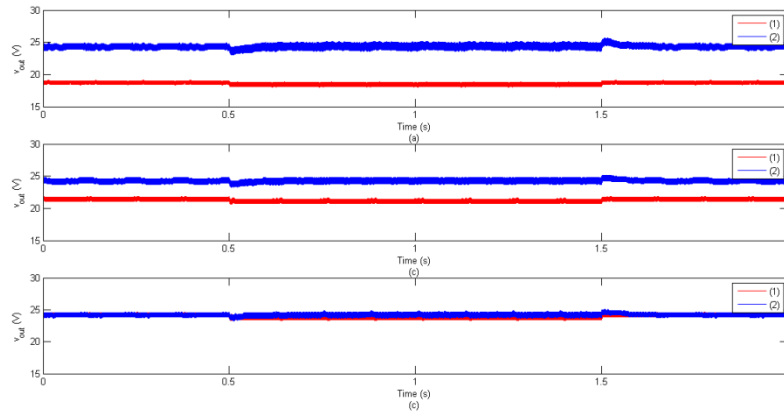


Fig. 3 The output voltage v_{out} waveforms of DC-DC boost converter with GMV control law without (1) and with (2) disturbance estimator alternating between load resistance 34Ω and 22.67Ω and operating at $V_{in} = 10.5 \text{ V}$ (a), $V_{in} = 12 \text{ V}$ (b) and $V_{in} = 13.5 \text{ V}$ (c)

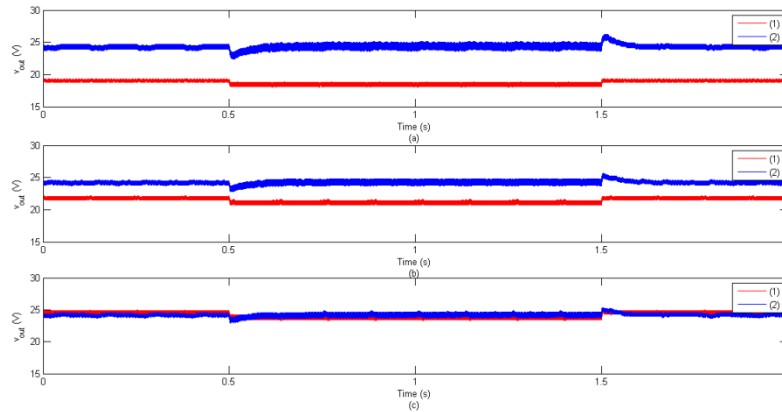


Fig. 4 The output voltage v_{out} waveforms of DC-DC boost converter with GMV control law without (1) and with (2) disturbance estimator alternating between load resistance 68 Ω and 22.67 Ω and operating at $V_{in} = 10.5$ V (a), $V_{in} = 12$ V (b) and $V_{in} = 13.5$ V (c)

5. CONCLUSION

This paper considers the use of generalized minimum variance control algorithm with one-step-delayed disturbance estimator in the control of DC-DC boost converter. The whole controller design procedure is based on the converter model given by the discrete-time transfer function. Therefore, there is no need for using additional current sensor. The presence of disturbance estimator increases the converter robustness to input voltage and load resistance variations, as well as the overall converter accuracy in the steady-state. Since GMV control term may be considered as the counterpart of digital equivalent control [9], there are no obstacles for the practical realization of the proposed control as one of the pulse-width-modulation (PWM) fixed frequency techniques.

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REFERENCES

- [1] S.-C. Tan , Y. M. Lai, Chi K. Tse, M. K. H. Cheung, "A fixed-frequency pulse-width modulation based quasi-sliding-mode controller for buck converters", *IEEE Trans. on Power Electron.*, vol. 20, no. 6, pp. 1379-1392, 2005, [Online]. Available: <http://dx.doi.org/10.1109/TPEL.2005.857556>
- [2] C. Basso, "Understanding the right-half-plane zero - Analytical description of the right-half-plane zero for voltage-mode and current-mode converters", available from <http://powerelectronics.com/power-management/understanding-right-half-plane-zero>, cited July 2017., 2009.
- [3] K. Wu, *Power converters with digital filter feedback control*, Elsevier Inc., 2016.

- [4] V. I. Utkin, *Sliding modes and their applications in variable structure systems*, Moscow, Nauka, Mir, 1978.
- [5] J. Y. Hung, W. Gao, J. C. Hung, "Variable structure control: A survey", *IEEE Trans. Ind. Electron.*, vol. 40, no. 1, pp. 2-21, 1993.
- [6] C. Edwards, S.-K. Spurgeon, *Sliding mode control: theory and application*, Taylor & Francis, London (UK), 1998.
- [7] H. Sira-Ramirez, "A geometric approach to pulse width modulated control in nonlinear dynamical systems", *IEEE Trans. Autom. Contr.*, vol. 34, no. 2, pp. 184–187, 1989, [Online]. Available: <http://dx.doi.org/10.1109/9.21094>
- [8] B. Draženović, "The invariance conditions in variable structure systems", *Automatica*, vol. 5, no. 3, pp. 287-295, 1969, [Online]. Available: [http://dx.doi.org/10.1016/0005-1098\(69\)90071-5](http://dx.doi.org/10.1016/0005-1098(69)90071-5)
- [9] D. Mitić, *Digital Variable Structure Systems Based On Input-Output Model*, Ph. D. Thesis, University of Niš, Faculty of Electronic Engineering, 2006.
- [10] D. W. Clarke, R. Hastings-James, "Design of Digital Controllers for Randomly Disturbed Systems," in *Proc. of IEE*, vol. 118, no. 10, pp.1502-1506, 1971.
- [11] W.C. Su , S. V. Drakunov, U. Ozguner, "An $O(T^2)$ boundary layer in sliding mode for sampled-data systems," *IEEE Transactions on Automatic Control*, vol. 45, no. 3, pp. 482-485, 2000, [Online]. Available: <http://dx.doi.org/10.1109/9.847728>
- [12] D. Mitić, Č. Milosavljević, "Sliding mode based minimum variance and generalized minimum variance controls with $O(T^2)$ and $O(T^3)$ accuracy, *Electrical Engineering (Archiv fur Elektrotechnik)*, vol. 86, no. 4, pp. 229-237, 2004, [Online]. Available: <http://dx.doi.org/10.1007/s00202-003-0198-y>
- [13] D. Mitić, D. Antić, M. Milojković, S. Nikolić, S. Perić, "Input-output based quasi-sliding mode control of dc-dc converter", *Facta Universities, Ser: Elec. Energ.*, vol. 25, no. , pp. 69-80, 2012, [Online]. Available: <http://dx.doi.org/10.2298/FUEE1201069M>
- [14] M. D. Almalawawe, D. Mitić, D. Antić, Z. Ičić , "An approach to microcontroller-based realization of boost converter with quasi-sliding mode control", *Journal of Circuits, Systems and Computers*, vol. 26, 1750106, 2017, [Online]. Available: <http://dx.doi.org/10.1142/S0218126617501067>
- [15] S. C. Tan, Y .M. Lai, Chi K. Tse, "A unified approach to the design of PWM-based sliding-mode voltage controllers for basic dc-dc converters in continuous conduction mode", *IEEE Trans. Circuits Syst.*, vol. 53, no. 8, pp. 1816–1827, 2006, [Online]. Available: <http://dx.doi.org/10.1109/TCSI.2006.879052>