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DESIGN OF A FOUR STAGES VCO USING A NOVEL DELAY CIRCUIT FOR OPERATION IN DISTRIBUTED BAND FREQUENCIES

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Abstract *The manuscript proposes a novel architecture of a delay cell that is implemented in 4-stage VCO which has the ability to operate in two distributed frequency bands. The operating frequency is chosen based on the principle of carrier mobility and the transistor resistance. The VCO uses dual delay input techniques to improve the frequency of operation. The design is implemented in Cadence 90nm GPDK CMOS technology and simulated results show that it is capable of operating in dual frequency bands of 55 MHz to 606 MHz and 857 MHz to 1049 MHz. At normal temperature (27^0) power consumption of the circuit is found to be 151μW at 606 MHz and 157μW at 1049 MHz respectively and consumes an area of 171.42μm^2. The design shows good tradeoff between the parameters-operating frequency, phase noise and power consumption.*

Key words: *Ring oscillator, Voltage controlled oscillator (VCO), Tuning Range*

1. INTRODUCTION

Phase Lock Loop (PLL), one of the key elements of contemporary wireless digital signal processing and instrumentation systems, is crucial for improving the performance of this electronic component. The parameters associated with VCO like operating frequency range, power dissipation and phase noise have important contribution towards the improvement of the PLL.

There are two widely used VCOs topologies and they are LC and ring VCOs. The former has a high resolution and frequency, but the operating frequency range is limited and the chip surface is big. The latter has many advantages like wide tuning range, easy integration, low chip area, multiphase clock and low power consumption; however, it has a low resolution and poor phase noise performance [1]. Ring VCOs are divided into two sorts based on their delay stages. 1) VCO with a single-ended ring (SERO) and 2) VCO with a differential ring

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(DRO). SEROs consume less area compared to DROs but have more noise and hence less efficient [3-7]. DROs are more resilient to common mode noise and have a lower swing.

Delay cell is the basic element of differential configuration oscillators. Many such delay cells were proposed by different researchers at different times. Maneatis et al proposed a delay cell that was used to design a ring oscillator which could oscillate with an operating frequency of 141 MHz. The delay cell was based on a source coupled pair [8]. A wide operating frequency three stage VCO was proposed by Yan et al that could operate in frequency range of 1.3 to 1.8 GHz, however the power consumption was comparatively high [9]. Park et al designed a 4 stage ring oscillator with low phase noise and operates in 900 MHz. The phase noise was found to be -101 dBc/Hz at 100 kHz [10]. Tu et al. proposed a novel delay circuit and used it to design two stages voltage controlled oscillator whose operating range was from 2.5 GHz to 5.2 GHz for a supply voltage of 1.8V. However due to lesser number of stages the phase noise achieved was -90.1 dBc/Hz at offset frequency of 1 MHz [11]. Sheu et al proposed a new differential delay cell which was implemented in three stages VCO, the tuning range was found to be 479 MHz to 4.09 GHz with phase noise -93.3 dBc/Hz at offset frequency of 1 MHz [12]. Parvizi et al. proposed design of ring oscillators using two topologies which are differential and single-ended. To reduce stage delay and boost tuning range, the VCO used a feed-forward technique and load in terms of inductive impedance [13]. A PLL was designed by Shruti Suman et al by proposing an improved performance VCO. The operating frequency varied from 2.26 GHz to 3.44 GHz with the help of a controlled voltage changed from 1V to 3V but they did not focus on phase noise[14]. A delay cell for using in ring oscillator with dual loop was proposed by Gao et al, where they also used controlled voltage to tune the frequency range. The design was efficient enough to achieve wideband tuning range while maintaning low phase noise [15]. To determine the optimal dimensions of the VCO, Gargouri et al proposed a systematic and efficient optimization method and found an optimal trade-off between various specifications [16]. Salem et al proposed a fault tolerant delay cell to be used for designing ring oscillator that uses redundant transistor methods to improve relaibility, power dissipation and phase noise [17]. Kumar et al presented a VCO using Nor gate and varactor tuning method with inversion mode [18]. The changes in the varactor width is considered for variation in the operating frequency. However there is still scope for improve in the phase noise. A low noise injection locked VCO was proposed by Lee et al in which a separate injection signal is employed and the oscillator output locks to the frequency of the injection signal [19]. The circuit showed tuning range having wide frequency and low phase noise with low power consumption. Ramazani et al presented some delay cells using basic inverters and current starved inverters to be used for designing VCO to achieve better frequency stability [20].

The proposed circuit is oriented towards designing of ring VCO with the ability to operate in disributed tuning range while maintaininng decent tradeoff between phase noise and power consumption in differential configuration. Thus the novelty of the work lies in allowing the same VCO to work in the high as well as low frequency ranges without altering the physical design of the circuit. The subsequent sections of the paper are organized as follows: section 2 deals with proposed VCO, section 3 deals with delay circuit analysis, section 4 deals with implementation and section 5 deals with conclusion.

2. PROPOSED VCO

Even and odd numbers of stages can be used in differential ring oscillators, but an odd number of stages cannot produce both in phase and quadrature phase outputs. Frequency of oscillation depends on factors like driving capability, load and number of stages. In addition, when the number of phases increase, the quantity of energy used, the amount of space needed, and the cost increased. Additionally, there will be greater phase noise with fewer stages. Therefore, maintaining adequate tradeoff between the various performance characteristics requires an optimal design. Two stages DRO will have tight constrains particularly in oscillations to occur, while three stages limit the output of in phase and quadrature phase, hence we choose to design a four stages VCO [21-23].

The designed VCO will be applicable in communication systems where multiphase signals are needed like phase array transceivers, fractional frequency synthesizers and clock data recovery circuits. Moreover, communication systems demand the need of wide range oscillators to cover a variety of standards across multiple frequency bands [24].

Proposed Delay cell of the VCO is designed using two control frequencies hence this technique is also known as dual frequency control technique [25-26]. It comprises of input V_{in1+}, V_{in2+}, V_{in1-} and V_{in2-}, output voltages V_{out+} , and V_{out-} , control voltages V_{cntr1} and V_{cntr2}. Considering T_{delay} as the delay time of the cell then total delay time of four stages VCO will be $4T_{delay}$ and hence the operating frequency will be $1/(4T_{delay})$. The proposed delay cell and four-stage VCO are depicted in Fig.1 and Fig.2.

The time constants τ_c and τ_d estimated during charging and discharging provide a generic equation for finding the oscillation frequency. The following formula is used to compute the time constant:

$$\tau = rc \tag{1}$$

Where, r is the resistance offered by the charging and discharging path, c is the lumped capacitance that is the combined parasitic capacitances.

Using τ_c and τ_d, time intervals T_1 and T_2 which are the charging and discharging time intervals of the delay cell are calculated. They are used for determining the oscillating frequency which is given by:

$$f_a = \frac{1}{T_1 + T_2} \tag{2}$$

Resistance(r) in the time constant formula is the resistance of PMOS and NMOS transistors respectively, and is given by:

$$r_p = \frac{1}{\mu_p C_{ox} \frac{W}{L} \left(|V_{gs}| - |V_{tp}|\right)} \tag{3}$$

$$r_n = \frac{1}{\mu_n C_{ox} \frac{W}{L} \left(|V_{gs}| - |V_{tn}|\right)} \tag{4}$$

Where μ_p and μ_n are the mobility of PMOS and NMOS transistors, C_{ox} is the oxide capacitances, both transistors channel width and length are W and L, respectively. V_{gs} is the applied gate to source voltage, V_{tp} and V_{tn} are the PMOS and NMOS threshold voltages. The

transistors are assumed to be working in triode region and small drain to source voltage V_{ds} is neglected.

Thus, from the formulae it can be clearly interpreted that higher the mobility lower will be the resistance or in other words resistance is inversely proportional to mobility. Moreover, resistance is directly proportional to time constant hence oscillating frequency is inversely dependent on resistance and directly dependent on mobility. So, transistor with higher mobility can play crucial role in improving the oscillating frequency.

Since the mobility of electrons is larger than that of holes, this has an effect on the current flow and time constant, or delay time, which has an additional impact on oscillation frequency. Lowering the resistance will result in a shorter delay time and a greater oscillation frequency. Since the NMOS time constant is lower than the PMOS time constant, the oscillation frequency will be higher. This idea inspired us to suggest the delay circuit depicted in Figure 1 and utilise it to create the VCO depicted in Figure 2.

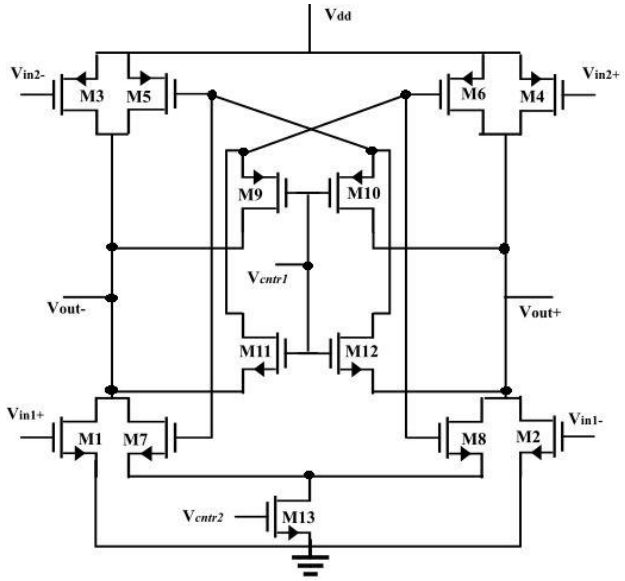

Fig. 1 Delay Cell

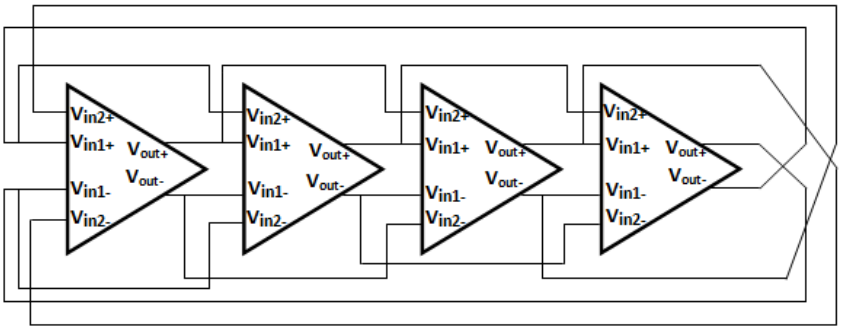

Fig. 2 Four stages VCO

3. DELAY CIRCUIT ANALYSIS

The proposed delay cell is for dual loop ring based voltage controlled oscillator [27-29]. The primary loop's inputs are M1 and M2, while the secondary loop's inputs are M3 and M4. The dual-loop technique amplifies the oscillation. M13 controls the ring VCO's frequency. The latch's feedback strength is made up of M5, M6, M7, M8, M9, M10, M11 and M12. Thus, it is simple to control the delay time of the latch by controlling V_{cntr2} while V_{cntr1} helps in maintaining the VCO to operate both in the low frequency and high frequency bands.

Considering the left part of the delay circuit which deals with V_{out-}, the charging and discharging time can be calculated as shown below:

Initial condition be $V_{out-}=V_l$ and $V_{out+}=V_o$, V_l and V_o being the minimum and maximum output voltages.

The charging time is controlled by V_{in2-} and the transistor M3, based on the initial condition M5 will be off, is given by

$$\tau_1 = r_3 C_{load} \tag{5}$$

r_3 is equivalent resistance of MOSFET M3 and C_{Load} is the parasitic capacitive load associated with V_{out-}.

$$r_3 = \frac{1}{\mu_p C_{ox} \frac{W}{L}\left(|V_{gs}| - |V_{tp}|\right)} \tag{6}$$

$$\begin{aligned} C_{Load} = {} & C_{db1} + C_{gd1} + C_{db3} + C_{gd3} + C_{ds3} + C_{db5} + C_{gd5} + C_{db7} \\ & + C_{gd7} + C_{db9} + C_{gd9} + C_{db11} + C_{gd11} + C_{in\_x} \end{aligned} \tag{7}$$

Where, C_{in_x} is the next stage input capacitance, C_{db} is drain to body, C_{gd} is gate to drain and C_{gs} is gate to source capacitances of the transistor. Across the load capacitance voltage will be

$$V_{C_{Load}} = V_0 - (V_0 - V_l)\exp\left(-\frac{T_1}{\tau_1}\right) \tag{8}$$

Suppose in the time interval T_1 capacitor charges upto αV_0 then

$$\alpha V_0 = V_0 - (V_0 - V_l)\exp\left(-\frac{T_1}{\tau_1}\right) \tag{9}$$

α is a constant with a value ranging from 0 to 1.

$$T_1 = \tau_1 \ln\left\{\frac{V_0 - V_l}{V_0(1-\alpha)}\right\} \tag{10}$$

In the next state when $V_{out-}=V_0$ and $V_{out+}=V_l$. The discharging phenomenon comprises of both charging and discharging time constants and the effective discharging time τ_2 is

$$\tau_2 = \{(r_1||(r_7 + r_{13})) - (r_3||r_5)\}C'_{Load} \tag{11}$$

r_1, r_5, r_7 and r_{13} represents the equivalent resistances of MOSFET M1, M5, M7 and M13.

$$C'_{Load} = C_{db1} + C_{gd1} + C_{ds1} + C_{db3} + C_{gd3} + C_{db5} + C_{gd5} + C_{db7} + C_{gd7} + C_{gd9} + C_{db9} + C_{db11} + C_{gd11} + C_{inx} \quad (12)$$

C'_{load} is node capacitance during time T_2

Now voltage across capacitor C'_{load} can be given by

$$V_{C'_L} = V_l - (V_l - \alpha V_0)\exp\left(-\frac{T_2}{\tau_2}\right) \quad (13)$$

Suppose the capacitor C'_{load} discharges to, βV_l in the time interval T_2 such that $\beta>1$ then

$$\beta V_l = V_l - (V_l - \alpha V_0)\exp\left(-\frac{T_2}{\tau_2}\right) \quad (14)$$

$$T_2 = \tau_2 \ln\left\{\frac{V_l - \alpha V_0}{V_l(1-\beta)}\right\} \quad (15)$$

$$T = T_1 + T_2 = \tau_1 \ln\left\{\frac{V_0 - V_l}{V_0(1-\alpha)}\right\} + \tau_2 \ln\left\{\frac{V_l - \alpha V_0}{V_l(1-\beta)}\right\} \quad (16)$$

And finally, f_{osc}=1/4T, for four stage ring VCO.

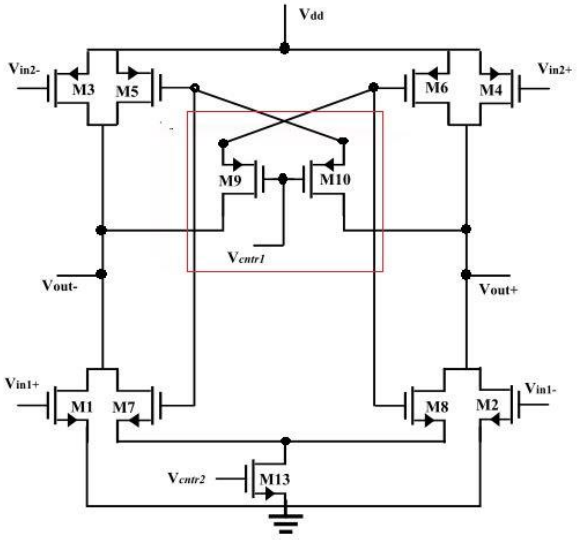

Fig. 3 Delay circuit for low voltage of V_{cntr1}

Case 1: When V_{cntr1} is low (0 to 0.3v), the transistors M9 and M10 become more dominant as both are PMOS transistors and they operate in low gate voltage than the M11 and M12 transistors. Hence the circuit is found to operate similar to the circuit shown in Fig. 3. The normal delay loop's input pair is M1 and M2, while the skewed delay loop's input pair is M7 and M8 in the circuit depicted in Fig. 3. Transistor M1 shuts off when the voltage connected to gate terminal of M1, V_{in1+}, is less than the threshold value. The source current

of the secondary input transistor M3 is already flowing towards the capacitor associated with output node, V_{out-}, because the input voltage at V_{in2-} reaches earlier than at V_{in1+}. This results in reduction of the output node's rise time.

In the delay cell, M5 and M6 combine to form a latch. M9 and M10 are cross-coupled transistors that control the load transistors' maximum gate voltages, as well as the latch strength and frequency of operation. Now varying the control voltage V_{cntr2} will vary the frequency of oscillation. The path delay increases due to the action of PMOS transistors M9 and M10, which causes the VCO to operate in the low frequency band.

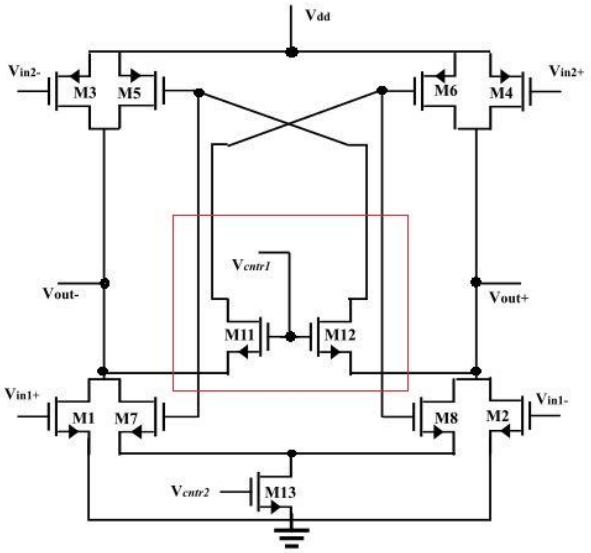

Fig. 4 Delay Cell due to high V_{cntr2}

Case 2: When V_{cntr1} is high (0.7V to 1V) the transistors M11 and M12 are more dominant as both are NMOS transistors and they operate in higher gate voltage than M9 and M10. The delay circuit is found to work as shown in Fig. 4. In this case M11 and M12 are cross-coupled transistors that govern the maximum voltages associated with the gate terminal of the transistors in the load and hence the latch strength and so the frequency of operation.

Phase Noise: Several noise elements influence the phase noise in a ring oscillator. The most prevalent types of noise are white noise and flicker noise. In contrast to inverter-based delay cells, differential delay cells operate in class A and consume a steady state current [30]. The main source of flicker noise is the FET that powers the common gate line for all the currents in the delay cells [31].

Equation (17) and (18) shows the SSB (Single Side Band) phase noise because of white noise and flicker noise respectively in differential oscillators.

$$L(f) = \frac{2kT}{I.\ln 2}\left[\gamma\left(\frac{\frac{3}{4}}{V_{effd}} + \frac{1}{V_{efft}}\right) + \frac{1}{V_{op}}\right]\left(\frac{f_0}{f}\right)^2 \tag{17}$$

$$L(f) = A\frac{K_f}{WLC'_{ox}f}\left(\frac{1}{{V_{efft}}^2}\right)^2 {f_0}^2 \quad (18)$$

Where, γ is noise factor of FET, V_{effd} and V_{efft} are the effective gate voltages of the differential delay cell at balance and unbalanced conditions, V_{op} is actual output voltage, I is tail current, f_0 is oscillation frequency, W and L stand for FET's width and length, A is the ratio of width of FET to that of tail FET and C'_{ox} is the oxide capacitance of NFET (tail transistor). In our design A is considered to be 1 as both W and L are of same length. Figure of Merit which is used for characterizing VCO performance can be obtained from the equation (19) [32].

$$FOM = L(f) - 20\log\left(\frac{f_0}{f}\right) + 10\log\left(\frac{P_{dc}}{1mW}\right) \quad (19)$$

P_{dc} is the dc power consumption. The dimension of both, NMOS and PMOS, shown in Table 1 are maintained same as the goal is to get the functional circuit in order to confirm the topological idea.

Table 1 Device Dimension

Device Aspect Ratio	
NMOS	PMOS
M1,M2,M7,M8, M11,M12,M13	M3,M4,M5,M6, M9,M10
120/100	120/100

Table 2 Variation of the parameters at different temperatures when V_{cntr1}=0.2V and V_{cntr2} is varied from 0 to 1V (Pre Layout)

Temp	Tuning Range	Power Consumption	Phase Noise 1M	Phase Noise 10M
0^0	42 MHz-672 MHz (93.75%)	160 µW	-93.10 dBc/Hz	-112.36 dBc/Hz
10^0	47 MHz-647 MHz (92.73%)	155 µW	92.94 dBc/Hz	-112.05 dBc/Hz
27^0	55MHz- 606 MHz (90.9%)	151 µW	-92.07 dBc/Hz	-111.25 dBc/Hz
70^0	63 MHz-487 MHz (87%)	144 µW	-91.86 dBc/Hz	-111.09 dBc/Hz

Table 3 Variation of the parameters at different temperatures when *Vcntr1*=0.77 V and *Vcntr2* is varied from 0 to 1V (Pre Layout)

Temp	Tuning Range	Power Consumption	Phase Noise 1M	Phase Noise 10M
0^0	1040 MHz-1230` MHz (15.44%)	169 µW	-93.42 dBc/Hz	-112.83dBc/Hz
10^0	969 MHz-1161 MHz (16.5%)	161 µW	-93.09 dBc/Hz	-113.23 dBc/hz
27^0	857MHz- 1049 MHz (18.3%)	157 µW	-93.50 dBc/Hz	-113.93dBc/Hz
70^0	585 MHz-771 MHz (24.12%)	152 µW	-92.88 dBc/Hz	-112.34 dBc/Hz

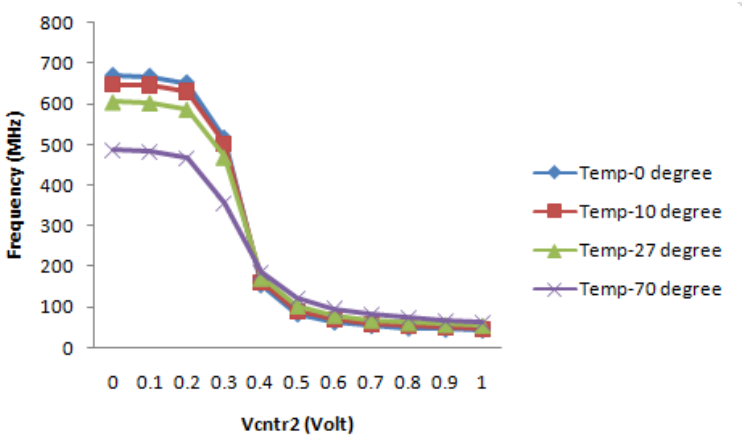

Fig. 5 Tuning range of VCO at different temperatures for *Vcntr1*=0.2V and *Vcntr2* varies from 0V to 1V (Pre layout simulation)

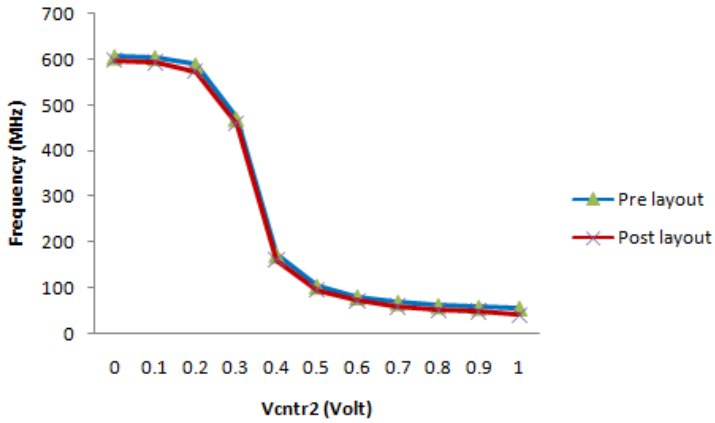

Fig. 6 Tuning range of VCO at normal temperature for V_{cntr1}=0.2V and V_{cntr2} varies from 0V to 1V (Pre and post layout simulation at 27^0)

Table 4 Corner Analysis at *Vcntr1*=0.2 V and *Vcntr2*=0.1V

Process Coners	Pre Layout @1MHz		Post Layout @1MHz		Pre Layout @10 MHz		Post Layout @10 MHz	
	Output Noise (dB)	Phase Noise (dBc/Hz)	Output Noise (dB)	Phase Noise(dBc/Hz)	Output Noise(dB)	Phase Noise (dBc/Hz)	Output Noise (dB)	Phase Noise (dBc/Hz)
NN	-93.10	-92.07	-93.23	-92.61	-112.26	-111.25	-113.00	-112.16
FF	-94.68	-93.32	-95.38	-93.87	-113.45	-112.33	-114.12	-113.11
FS	-96.12	-95.54	-96.62	-95.93	-116.10	-114.56	-116.96	-115.22
SF	-95.22	-94.56	-95.88	-94.89	-115.31	-113.34	-116.45	-114.31
SS	-94.20	-93.40	-94.66	-93.84	-112.87	-111.86	-113.10	-112.53

4. IMPLEMENTATION

The proposed four stages VCO design is implemented using cadence CMOS 90nm technology. Device dimension used in the circuit is mentioned in Table 1. Analysis of tuning ranges were carried out by varying V_{cntr2} from 0V to 1V for different values of V_{cntr1}. Mainly V_{cntr1} was divided into two ranges, the lower one 0 to 0.5V and upper 0.5V to 1.0V. Optimum values for maximizing tuning range in both cases were found to be 0.2V (lower) and 0.77V (upper). Oscillating frequency ranges from 55 MHz to 606 MHz (91% approx.) for lower band with the control voltage V_{cntr1}=0.2V as shown in Fig 5 and Table 2. Whenever path delay is high oscillating frequency is found to be low and vice versa. Fig 7 and Table 3 shows variation of tuning range due to change in V_{cntr2} keeping V_{cntr1}=0.77V. V_{cntr2} varies from 1V to 0V and the tuning range is found to be 857 MHz to 1049 MHz (18.30%) at normal temperature. Thus, it can be considered as operation in higher band frequency. So, the benefit of the circuit is that the same circuit can be operated in two different bands of frequency and thereby increasing the tuning range of the circuit.

Effect of Temperature: Due to the changes in transconductance gain (g_m), threshold voltage (V_{th}), electron and hole mobility (n and p) and parasitic capacitors, transistors have the biggest impact on the frequency drift and they are obtained as follows [33]:

$$g_m = \mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{th}) \tag{20}$$

$$V_{th} = V_{th_0} - \alpha(T - 27^0) \tag{21}$$

$$\mu(T) = \mu(T = 27^0)\left(\frac{T}{27^0}\right)^{-\frac{3}{2}} \tag{22}$$

The operation of the circuit is tested by varying the temperatures; it is found that the operating frequency is reduced with increase in frequency. Analysis of the circuit is carried out by varying the temperatures from 0^0C to 70^0C in both pre layout and post layout at V_{dd}=1V, V_{cntr1} equals to 0.77 V and 0.2 V respectively and V_{cntr2} is varied from 0 to 1V.

Comparative analysis between the pre and post layout simulation with respect to tuning range are shown in Fig. 6 and Fig. 8, it is found that the changes in frequency tuning range due to the control voltage V_{cntr2} are close to each other in both the cases. Corner analysis of

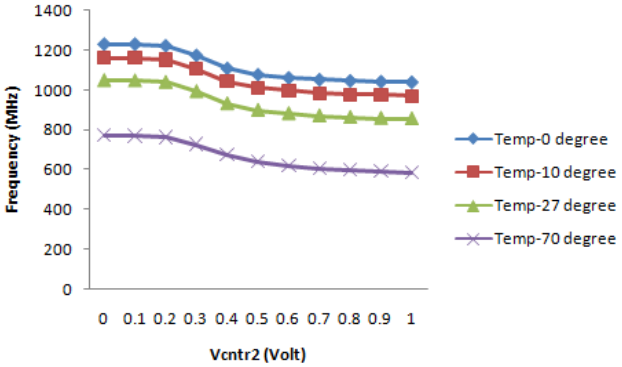

Fig. 7 Tuning range of VCO at different temperatures for *Vcntr1*=0.77 V and *Vcntr2* vary from 0V to 1V.

the circuit in terms of output and phase noise are depicted in Tables 4 and 5 for all the five processes namely NN, FF, FS, SF and SS and the results found are satisfactory. The delay circuit layout design is 5.87µm x 6.86µm, while the four-stage VCO layout design is 24.98µm x 6.86µm, spanning an area of 171.42m^2. They are depicted in Fig. 9 and Fig. 10.

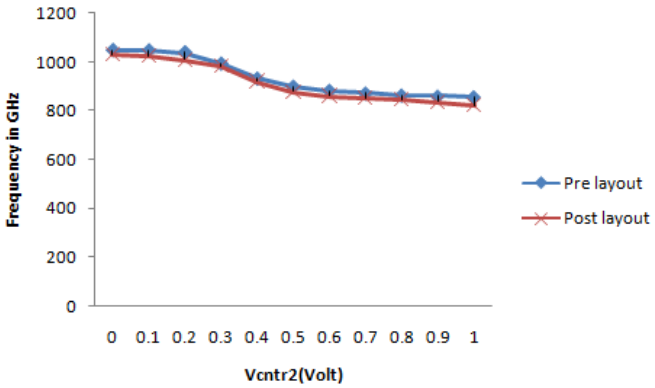

Fig. 8 Tuning range of VCO at normal temperature for V_{cntr1}=0.77V and V_{cntr2} varies from 0V to 1V (Pre and post layout simulation at 27^0)

Table 5 Corner Analysis at V_{cntr1}=0.77V and V_{cntr2}=0.1V

Process Coners	Pre Layout @1MHz		Post Layout @1MHz		Pre Layout @10 MHz		Post Layout @10 MHz	
	Output Noise (dB)	Phase Noise (dBc/Hz)	Output Noise (dB)	Phase Noise (dBc/Hz)	Output Noise (dB)	Phase Noise (dBc/Hz)	Output Noise (dB)	Phase Noise (dBc/Hz)
NN	-96.23	-93.50	-97.11	-94.78	-115.31	-113.93	-116.35	-114.42
FF	-95.68	-94.33	-96.28	-94.96	-116.20	-114.42	-116.85	-115.36
FS	-99.72	-97.23	-100.22	-98.17	-118.51	-117.81	-119.24	-119.42
SF	-98.22	-96.48	-98.89	-97.33	-117.54	-116.71	-118.21	-117.36
SS	-97.05	-93.60	-97.76	-94.28	-115.86	-114.11	-116.10	-115.06

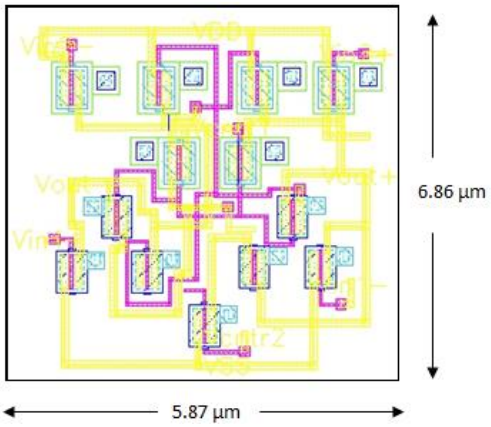

Fig. 9 Layout of the proposed delay cell

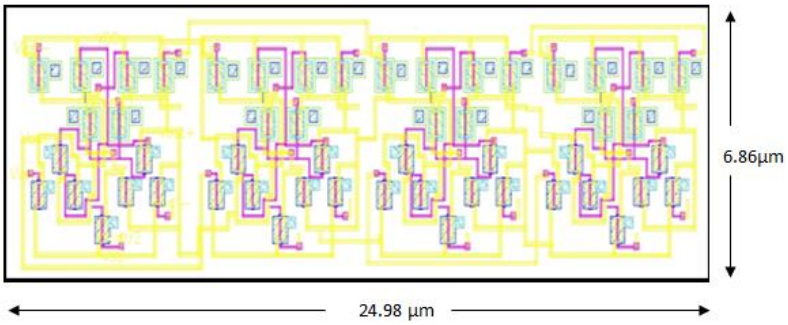

Fig. 10 Layout of the 4 stage VCO

The layout design shown in Fig. 9 and Fig. 10 can further be optimized to reduce the area significantly and get results closer to the obtained in the schematic level. One of the main advantages of the proposed circuit is that the same circuit can be used for working in low frequency range as well as high frequency range by varying the control voltages. However, the range of operations in terms of tuning range is comparatively low. Additionally, there is lot of transistors in the delay circuit which further raises the count in the oscillator even more.

In the realization column of Table 6 it is highlighted that the comparative parameters which are oscillation frequency, consumption of power and phase noise values are either measured or simulated. In our case post-layout values are considered.

Table 6 Comparison Parameters

References	Technology (nm)	Supply Voltage (V)	Number of Stages (N)	Oscillation Frequency range (GHz)	Power Consumption (mW)	Phase Noise (dBc/Hz)	FOM dBc/Hz	Realization Level
11	180	1.8	2	2.5-5.2 (74%)	17	-90.1 @ 1MHz	----	Measured
16	180	1	2	0.473-7.54 (93.72%)	7.41	-107.1 @ 10MHz	-150.44	Simulated
31	180	1.8	4	0.455 to 0.505 0.00139 to 0.00145	1.98 (Lower band) and 9.7 (Upper band)	----	----	Simulated
12	180	1	4	0.479-4.09 (88.28%)	10	-93.3 @ 1MHz	-154.4	Measured
18	90	1 to 3	3	1.379-1.970 (30%) 0.650-2.584 (74.84%) 0.556-2.584 (78.48%)	0.129 to 5685	-89.779 @ 1MHz	-154.51	Simulated
28	65	1.2	30	0.556	0.72	-101.7 @ 1MHz	-158	Simulated
15	65	1.8	3	0.470-0.964 (51.24%)	4.1	-116 @1 MHz	-169	Measured
29	90	1.2	4	9.21	2.092	-137.9 @ 1MHz	----	Post Layout
Proposed Work	90	1	4	0.048 to 0.57 (91.57%) and 0.82 to 1.01 (18.8 %) {Distributed band}	0.151 (Lower band) and 0.157 (Upper band)		-152.40 and -160.64	Post Layout

5. CONCLUSION

A four-stage VCO is designed using a novel differential delay circuit. The VCO is found to be operated in two distributed band of frequencies namely lower and upper which is one of its main advantages. Pre layout simulation result shows operating frequency bands are 55 MHz to 606 MHz (lower) at normal temperature when one of the control voltages V_{cntr1} is maintained at 0.77V while the other one V_{cntr2} varied from 0V to 1V. Phase noise at 1MHz and 10 MHz offset are found to be - 92.07 dBc/Hz and -111.25 dBc/Hz at lower frequency band. The VCO operates in 857 MHz to 1049 MHz (upper) when V_{cntr1} is 0.2V and V_{cntr2} varied from 0V to 1V. In this band the phase noise at 1MHz and 10 MHz offset are -93.50 dBc/Hz and -113.93 dBc/Hz. Pre Layout Power consumption of the VCO at 27^0 is found to be 151µW and 157µW for the operating frequencies of 606 MHz and 1049 MHz respectively.

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