FACTA UNIVERSITATIS
Series: **Electronics and Energetics** Vol. 35, N° 4, December 2022, pp. 619-634
https://doi.org/10.2298/FUEE2204619L

Original scientific paper

PERFORMANCE ANALYSIS AND OPTIMIZATION OF 10 NM TG N- AND P-CHANNEL SOI FINFETS FOR CIRCUIT APPLICATIONS

Abdelaziz Lazzaz[1], Khaled Bousbahi[2], Mustapha Ghamnia[1]

[1]Laboratoire des Sciences de la Matière Condensée (LSMC), département physique, Université d'Oran 1 Ahmed Ben Bella, Oran, Algérie
[2]ESGEE d'Oran, Oran, Algérie

Abstract. *This paper analyses the electrical characteristics of 10 nm tri-gate (TG) N- and P-channel silicon-on-insulator (SOI) FinFETs with hafnium oxide gate dielectric. The analysis has been performed through simulations by using Silvaco ATLAS TCAD with the Bohm quantum potential (BQP) algorithm. The influence of the geometrical parameters on the threshold voltage V_{TH}, the subthreshold swing (SS), the transconductance and the on/off current ratio, I_{ON}/I_{OFF}, is investigated. The two structures have been optimized for CMOS inverter implementation. The simulation results show that the N-FinFET and the P-FinFET can reach a minimum SS value with Fin heights of 15 nm and 9 nm, respectively. In addition, low threshold voltages of 0.61 V and 0.27 V for N- and P-channel SOI FinFETs, respectively, are obtained at a Fin width of 7 nm.*

Key words: *FinFET, CMOS, Quantum effect, Leakage current*

1. INTRODUCTION

Nanoelectronics is a field of engineering technology which is used for controlling device properties at the nanometric scale. To meet the increasing demands for high-performance and high-speed applications, transistors need to be aggressively scaled down. This poses huge modifications both in the development of new device structures and in the fabrication processes.

When the channel length is less than 20 nm, Short-Channel Effects (SCEs) become insurmountable and, consequently, the device performance degrades. Multi-gate FETs have successfully enabled CMOS scaling and are considered to be the best alternative structures that can extend to 10 nm node technology.

Received April 8, 2022; revised June 21, 2022 and June 26, 2022; accepted June 26, 2022
Corresponding author: Abdelaziz Lazzaz
Laboratoire des Sciences de la Matière Condensée (LSMC), département physique, Université d'Oran 1 Ahmed Ben Bella, Oran, Algérie
E-mail: lazzaz.abdelaziz@gmail.com

Most of the reported FinFETs are fabricated with a silicon channel, they present different advantages such as: i) reduced SCEs and a low leakage current, ii) superior electrostatic control through tri-gate structures, iii) reduced effect of substrate bias on the threshold voltage and excellent carrier transport properties along with more aggressive channel length scaling possibilities [1].

The conventional FinFET technology has to face the competition from other technology options because of its high access channel resistance due to its extremely thin body. To improve FinFET performance, one must address the quantum confinement problem. Hence, the use of the BQP algorithm, which is based on the Bohm interpretation of quantum mechanics [8], may become more important.

N.P. Maity *et al.* in 2017 [22] have explored the application of the promising high-k dielectric material, HfO_2, on MOS devices. They observed that the tunneling current is inversely proportional to the dielectric constant of the oxide material.

Niladri Pratap Maity *et al.* in 2016 [23] have developed an analytical model to evaluate the impacts of the HfO_2 on the current density model with a comparison between the theoretical model and the experimental measurements.

Lazzaz *et al.* in 2022 [27] have demonstrated that quantum effects play a dominant role in nanostructures. They used the BQP method to fit experimental measurement of the I_{DS}-V_{DS} characteristics for 14 nm TG N-FinFET.

Neha Gupta *et al*. in 2020 [28] have explored the performance evaluation of high-k gate stack on the analog and RF figure of merits (FOMs) of 9 nm SOI FinFET. The results of their simulation confirm that the limitations of the transistor device such as SCEs, leakage current and parasitic capacitance have been reduced and pave the way for high-speed switching and RF application due to the use of high-k dielectric material with SiO_2 between gate and fin.

Anisur Rahman *et al.* in 2018 [29] found that Intel's 10 nm technology achieved scaling benefits over its preceding 14 nm generation at matched or better transistor reliability.

Marupaka Aditya *et al.* in 2021 [30] have confirmed that using high-k dielectric materials increase the ON current and improve the device performance.

Sanghamitra Das *et al.* in 2021 [31] have studied the effect of FinFET geometric parameters (channel length and fin height) on the RF FOMs by using TCAD simulations. Their results confirm that decreasing the channel length or increasing the fin height improves the RF parameters.

Mostak Ahmed et *al.* in 2021 [31] have simulated the electrical characteristics of a 3-D TG N-channel SOI FinFET with a channel length of 5 nm using different gate dielectric materials. The results of their simulation confirm that high-k dielectric materials are the better option in the fabrication for future TG FinFET devices.

The above literature survey indicates the importance of using high-k dielectrics in FinFET devices to reduce SCEs. In this paper, the transfer and the transconductance characteristics have been computed in order to find the electrical response of TG N- and P-channel SOI FinFETs with 10 nm channel length. The BQP algorithm has been used from Silvaco ATLAS TCAD software to simulate the I-V characteristics.

The simulated devices have been optimized in terms of geometry to have optimal voltage transfer characteristics (VTC) for a CMOS inverter [14], [15].

2. DEVICE STRUCTURE

The hafnium-based oxide is extensively used because of its low leakage property and its high thermal stability with silicon [25]. The geometric parameters used in this simulation are represented in Table 1 and the operating parameters of the two structures are presented in Table 2.

Table 1 Geometric parameters

Symbol	Designation	Value
L	Channel length	10 nm
L_D, L_S	Drain, source length	12 nm
EOT	Equivalent oxide thickness	0.68 nm
V_{DD}	Supply voltage (V)	0.75 V

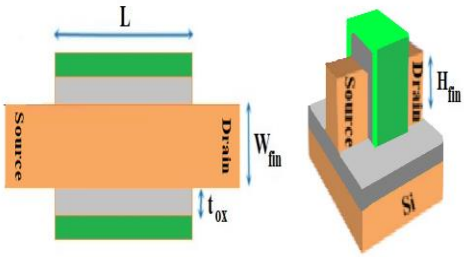
Table 2 Operating parameters

Symbol	Designation	Value
E_g	Gap energy	1.12 eV
k(Si)	Dielectric constant of silicon	11.9
k(HfO_2)	Dielectric constant of hafnium dioxide	24
N_{ch}	Channel doping concentration	10^{16} cm^{-3}
$N_{S/D}$	Source/drain doping concentration	10^{21} cm^{-3}
Φ_G	Gate work function	4.85 eV

TG FinFET technology is based on the following fin geometry: fin length (L), fin width, W_{fin}, fin Height, H_{fin}, and oxide thickness, t_{ox}.

The numerical resolution, which includes the gate work function and the choice of physical models, represents one of the two main steps in the Silvaco ATLAS tools. The Shockley-Read-Hall (SRH) theory has been used.

Figure (1a) shows the top-view layout of TG SOI FinFET with 10 nm gate length, and Figure (1b) illustrates the 3D schematic view of FinFET. The gate oxide thickness is the same for all three sides of the fin. The H_{fin} is considered as the distance between the top gate and the bottom gate oxides. The W_{fin} is represented as the distance between front gate and back gate. L_G is the gate length and BOX is buried oxide.



(a) (b)

Fig. 1 (a) Top-view layout of TG SOI FinFET [21], (b) 3D schematic view of TG SOI FinFET

All simulations have been performed using ATLAS and DEVEDIT 3D device simulator and different operating parameters such as the supply voltage, are extracted from the predictive technology model (PTM) [32].

3.Drain Current Model of the TG FinFET

The device electrostatics is governed by the 3-D Poisson's equation [5][19]:

$$\frac{d^2\phi(x,y,z)}{dx^2}+\frac{d^2\phi(x,y,z)}{dy^2}+\frac{d^2\phi(x,y,z)}{dz^2}=\frac{qn(x,y,z)}{\varepsilon_{Si}} \tag{1}$$

ϕ : Electrostatic potential; q: electron charge; ε_{Si}: silicon permittivity, n(x,y,z): electron density.

Quantum effects become more dominant and are difficult to control in the device. Hence, in this study, one must consider them by selecting the appropriate model such as the BQP.

The BQP model can also be used with the energy balance and hydrodynamic models, where the semi-classical potential is modified by the quantum potential in a similar way as for the continuity equations [20].

According to the Bohm interpretation of quantum mechanics, the wave function can be represented in polar coordinates by the following expression [8]:

$$\psi = Rexp(\tfrac{iS}{\hbar}) \tag{2}$$

R: Probability density per unit volume; S has the dimension of an "action" (energy × time)

The Schrödinger equation can be written as:

$$-\frac{\hbar^2}{2}\nabla\left\{M^{-1}\nabla\left[\operatorname{Re} xp(\frac{iS}{\hbar})\right]\right\}+V\operatorname{Re} xp(\frac{iS}{\hbar})=E\operatorname{Re} xp(\frac{iS}{\hbar}) \tag{3}$$

$M^{-1}\nabla S$: The local velocity of the particle associated with the wave function.
E is conserved and equal to the sum of the potential energy and V is the kinetic energy [8].

The quantum potential is derived from the use of the Bohm interpretation of quantum mechanics and it is described by the following equation [8][20]:

$$Q=-\frac{\hbar^2}{2}\frac{\nabla(M^{-1}\nabla R)}{R} \tag{4}$$

The threshold voltage expression in the case of a FinFET structure can be defined by [18]:

$$V_{th}=V_{fb}+|2\phi_B|+\frac{\lambda_b}{C_{ox}}\sqrt{(2qN_D\varepsilon_S(|2\phi_B|+V_{sb}))}-\lambda_d\lambda_{ds} \tag{5}$$

V_{fb}: Flat band voltage; $\emptyset_B$: Body potential; C_{ox}: Gate oxide capacitance; q: electron charge; N_S: Doping concentration; ε_s: dielectric constant of the semiconductor; V_{sb}: the reverse bias between the source and the body; λ_d: drain-induced barrier lowing (DIBL) coefficient; λ_{ds}: channel length modulation; λ_b: barrier variation coefficient.

The transconductance, g_m, represents the drain current variation with respect to gate voltage. It is represented by the following equation [4][13]:

$$g_m = \frac{dI_D}{dV_{GS}} \tag{6}$$

SS is a major parameter for calculating the leakage current, and is calculated as [13]:

$$SS = \frac{dV_{GS}}{d(\log_{10} I_{DS})} \tag{7}$$

The value of the DIBL is [3]:

$$DIBL = \frac{\Delta V_{TH}}{\Delta V_{DS}} \tag{8}$$

V_{TH}: threshold voltage; V_{DS}: drain-source voltage.

4. Results

FinFET is considered to be a promising candidate for ultimate CMOS device structure because it has robustness against SCEs and higher current drivability. SOI FinFETs have shown several advantages over bulk FinFETs. SOI FinFET could suppress the leakage current between source and drain through the body below the channel fin, and it has low source/drain-to-substrate capacitance, thereby improving the speed characteristics.

In this section, the effect of changing the fin width and the fin height is analyzed and investigated for FinFET structures. The different electrical parameters which are derived in this simulation, such as leakage and SS, are compared with other published results [9][12][17] in order to validate our model.

The BQP model has better convergence properties in many situations and it can be calibrated against results from the Schrödinger-Poisson equation under conditions of negligible current flow.

4.1. Simulation and analysis

SRH theory accounts for the generation and recombination of charges carriers through electron and hole capture and emission states within the energy gap.

The software TCAD was used to simulate the structure and the characteristics of the TG FinFET. Figure 2 represents I_{DS}-V_{GS} transfer characteristics of the N-channel FinFET in linear scale with V_{DS} = 0.7 V, which is higher than the threshold voltage. The ON current in this simulation is 4 μA when $V_{GS} = V_{DD}$.

One can observe that the threshold voltage, V_{TH}, in this simulation is 0.62 V.

The V_{TH} of the device is related to the position of the fermi level with respect to the sub-bands energy levels. Increasing the fin height will actually reduce the carrier quantum confinement, thereby reducing the sub-band energy.

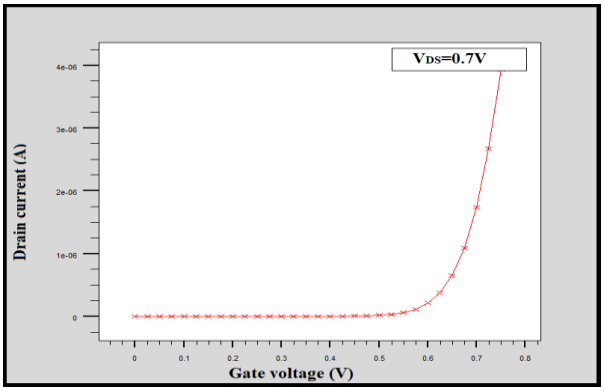


Fig. 2 Transfer characteristics for N-channel FinFET

To include quantum confinement in the computation of the I_D-V_{GS} characteristics, BQP has been used. As a result, a correction of the value of drain current has been achieved. Figure 3 represents the transfer characteristics in logarithmic scale. The gate voltage is swept from 0 to 0.75 V. We note that the leakage current is 10^{-14} A when V_{GS} = 0 V. The leakage current obtained in this simulation is less than that obtained by Dhananjaya Tripathy et al [26].

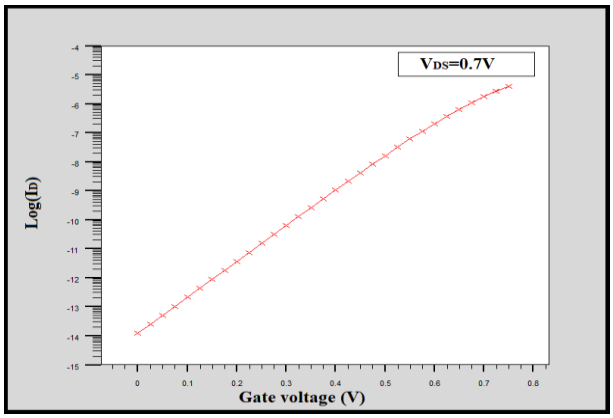


Fig. 3 Transfer characteristics N-channel FinFET in logarithmic scale

Figure 4 represents the output characteristics for N-channel SOI FinFET. We note that the drain saturation current is $2x10^{-6}$A at V_{DS} = V_{DD} = 0.75 V. We observe that the Early effect is more pronounced.

We find that an increase in V_{GS} will result in higher channel conductivity. The output characteristics have been obtained for V_{GS} = 0.7 V.

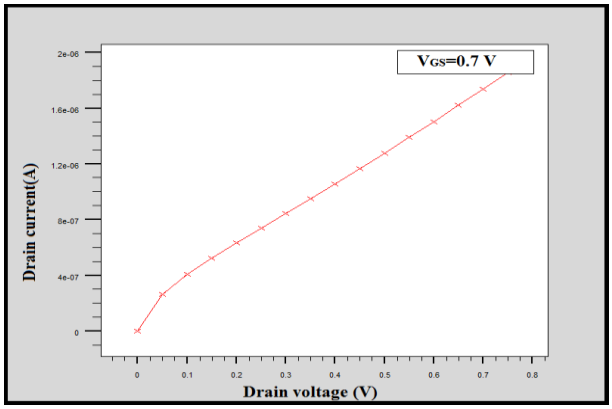


Fig. 4 Output characteristics of N-channel FinFET

Figure 5 represents the transconductance of N-channel FinFET. The gate voltage is swept from 0 to 0.75 V. We note that the maximum value of the transconductance at V_{DS} = 0.7 V is 5x10^{-5} A/V.

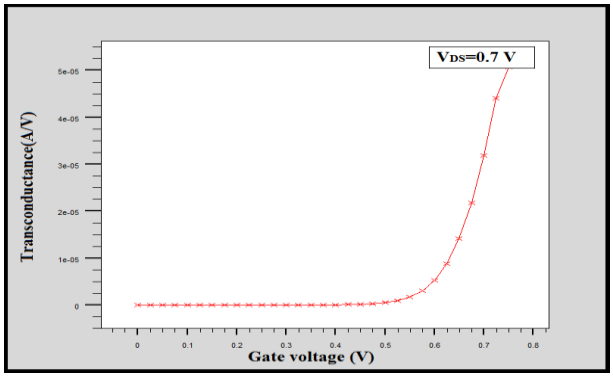


Fig. 5 Transconductance characteristics of N-channel FinFET

The higher value of the transconductance can be attributed to the higher strain in the short channel device. The transconductance peak can be reduced by reducing the channel length. Shorter gate length, L_G, provides less resistance and lower surface-roughness scattering, which leads to a higher transconductance and mobility. The higher mobility is induced by the quasi-ballistic transport instead of mobility increase.

Table 3 represents the different performance parameters of N-channel SOI FinFET [6][11]:

Table 3 Performance parameters of N-channel FinFET

Parameter	Value
I_{ON}	4 µA
I_{OFF}	10^{-14} A
I_{ON}/I_{OFF}	$4x10^{8}$
V_{TH}	0.62 V
DIBL	21.05 mV/V
SS	79.48 mV/dec

The values of SS and DIBL indicate a performance comparable with the state of the art obtained in PTM 10 nm HP NMOS and PMOS, such as the value of SS which is 102.4 mV/dec and DIBL which is 212 mV/V. But, we must optimize these values in order to have a good performance of the device [17].

The SS provides a good performance comparable to the one obtained by Ajay Kumar *et al* [12], and the calculated performance ratio is better than that obtained by Buryk *et al* [9].

Figure 6 represents the transfer characteristics of P-channel FinFET in linear scale with V_{SD} = 0.7 V. We note that the ON current in this structure is 6.25x10^{-5} A.

The ON current is measured at $V_{SG} = V_{DD}$= 0.75 V. The value of the threshold voltage in this simulation is 0.30 V.

The performance ratio, I_{ON}/I_{OFF}, calculated in this simulation is higher than that calculated by A.S. Opanasyuk *et al* [9].

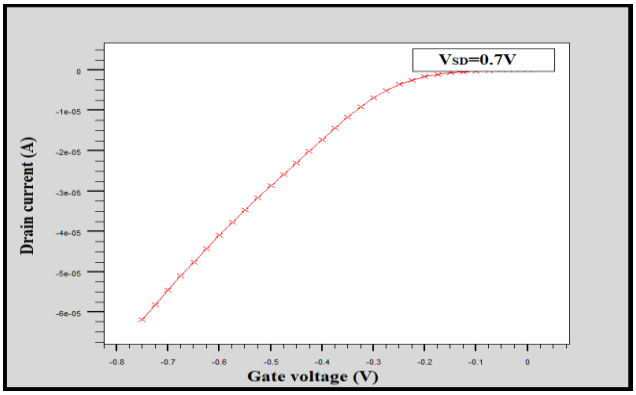


Fig. 6 Transfer characteristics of P-channel FinFET

Figure 7 represents the transfer characteristics of P-channel FinFET in logarithmic scale. We note that the leakage current is 1.58x10^{-8} A when V_{SG} = 0 V.

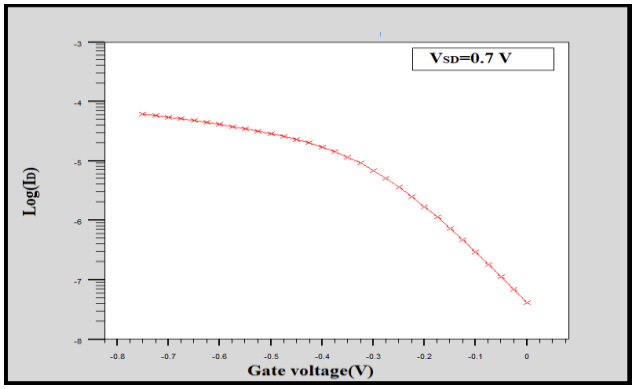


Fig. 7 Transfer characteristics in logarithmic scale of P-channel FinFET

Figure 8 represents the output characteristic of P-channel FinFET. We note that the drain current saturation is $5.5x10^{-5}$ A.

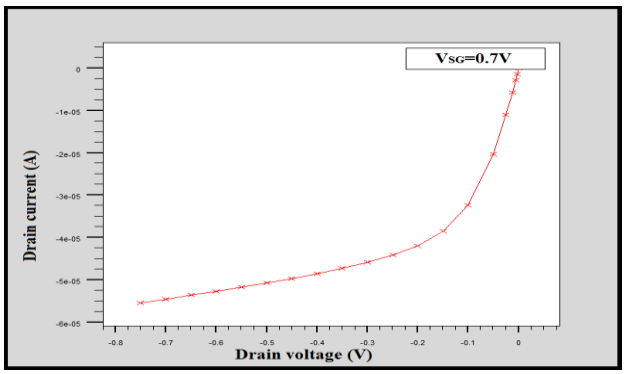


Fig. 8 Output characteristics P-channel FinFET

Table 4 represents the different performance parameters:

Table 4 Performance parameters of P-channel FinFET

Parameters	Values
I_{ON}	$5.5x10^{-5}$ A
I_{OFF}	$2.51x10^{-8}$ A
I_{ON}/I_{OFF}	$2.19x10^{3}$
V_{TH}	0.31 V
SS	133.50 mV/dec

4.2. Effect of the fin height

In this section, we investigate the impact of the fin height variation on I_D-V_{GS} characteristics. Quantum effects are included in the simulation. We think that the calculated optimized values of heights in N- and P-channel FinFETs can be used as geometric parameters in the PTM for the design of CMOS inverters.

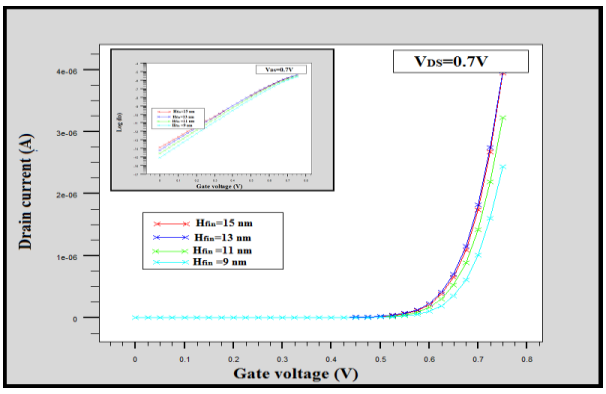


Fig. 9 Transfer characteristics with different fin heights for N-channel FinFETs

Figure 9 represents the transfer characteristics of N-channel FinFETs with different height values, 9 nm, 11 nm, 13 nm and 15 nm. It is clear that as we increase the fin height, the ON current increases from 2.5 μA up to 4 μA. The ON current allows the driving capability of the device. The increase of fin height increases the inversion charge density and thereby increases the ON current [24]. We note that the leakage current increases with the increase of the fin height because trap-assisted-tunneling is more important than direct tunneling.

Table 5 represents the impact of fin height on the subthreshold swing and the threshold voltage of the simulated device:

Table 5 Impact of fin height of N-channel FinFET

Parameter	9 nm	11nm	13nm	15nm
SS (mV/dec)	73.86	78.57	79.76	83.75
V_{TH} (V)	0.67	0.66	0.65	0.64

We note that the increase of fin height increases the subthreshold swing, and the threshold voltage decreases in the device. The increase of the subthreshold swing is due to the increase in the total capacitance, so we need to minimize the parasitic capacitance in order to reduce the power consumption. The decrease of the threshold voltage V_{TH} is due to the decrease of the fermi level.

Figure 10 represents the impact of fin height on the performance ratio (I_{ON}/I_{OFF}). We note that the increase of fin height up to 13 nm decreases the performance of the device. The performance ratio increases because of the decrease of leakage current [2].

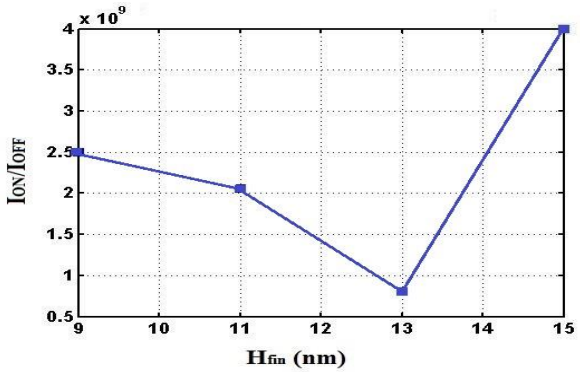


Fig. 10 The impact of fin height on the performance ratio of N-channel FinFET

The suitable value of fin height for the simulated device is 15 nm because it shows a larger performance ratio equal to $4x10^9$.

Figure 11 represents the impact of fin height variation on P-channel FinFET transfer characteristics. We note that the ON current increases with the increase of fin height.

We note that the leakage current increases with increase of fin height because direct tunneling is more important than trap-assisted-tunneling.

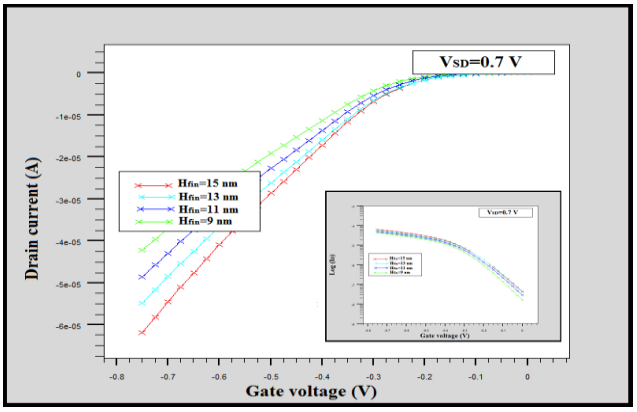


Fig. 11 Impact of Fin height on the transfer characteristics of TG P-channel FinFET

Table 6 displays the impact of fin height on subthreshold swing and V_{TH} in 10 nm P-channel FinFET.

Table 6 Impact of Fin height on P-channel FinFET

Parameter	9 nm	11 nm	13 nm	15 nm
SS (mV/dec)	129.62	137.50	133.33	133.50
V_{TH} (V)	0.35	0.33	0.32	0.31

The variation of subthreshold swing is due to the total capacitance of the device. The threshold voltage in P-channel FinFET decreases with increasing fin height.

Figure 12 illustrates the impact of fin height on performance ratio of P-channel FinFET. We note that the increase of fin height until H_{fin} = 13 nm decreases the performance ratio, then the performance ratio increases when H_{fin} > 13 nm because of the decrease of the leakage current[2].

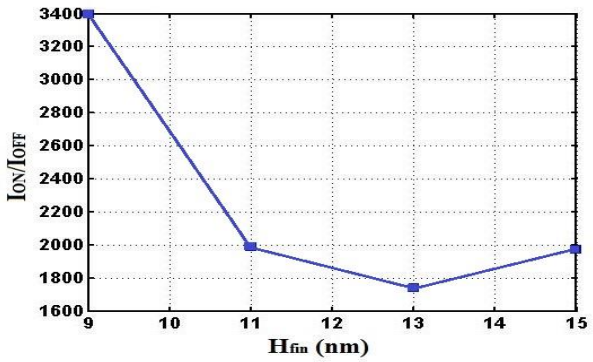


Fig. 12 Impact of fin height on the performance ratio of P-channel FinFET

The suitable value of this optimization is 9 nm because it allows a desirable performance ratio.

4.3. Effect of Fin width

In this section, we investigate the impact of fin width on the performance of N-channel FinFET.

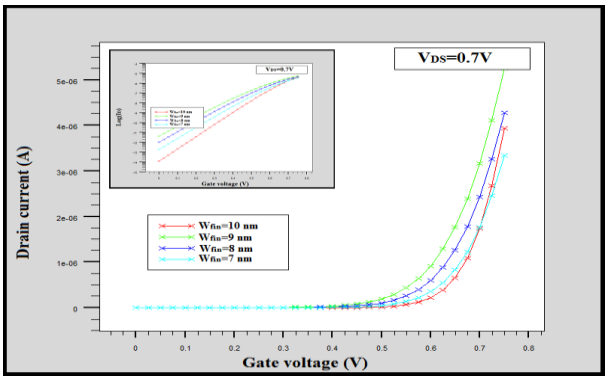


Fig. 13 Impact fin width on N-channel FinFET

Figure 13 shows the transfer characteristics of N-channel FinFET for different values of fin width. The gate voltage is swept from 0 V to 0.75 V. We note that the ON current increases from $4x10^{-6}$ A up to $5.25x10^{-6}$ A, then it falls down to $3.30x10^{-6}$ A because the strain effect in the channel increases. The large fin width decreases the mobility and the inversion charge and results in a smaller drain current.

The leakage current increases from 10^{-14} A up to $3.16x10^{-12}$ A when fin width is 9 nm. When fin width is greater than 9 nm, the leakage current decreases down to $1.58x10^{-13}$ A because direct tunneling is more important than the trap-assisted-tunneling.

The following Table 7 represents different values of subthreshold swing and V_{TH} for different fin widths. We note that the subthreshold swing and the threshold voltage increase with increasing fin width.

Because of the quantum effects along the W_{Fin} direction, the channel electrons will populate the discrete sub-bands. The V_{TH} will increase because more gate-bias is required to populate electrons into the lowest sub band, which is significantly above the bottom of the conduction band by eV_{TH}.

It should be underlined that a large fin width allows the enlarging of the total gate width therefore, the gate and depletion capacitance increases and subthreshold swing increases [16].

Table 7 Impact of Fin width of N-channel FinFET

Parameter	7 nm	8 nm	9 nm	10nm
SS (mV/dec)	95.31	106.89	114.54	171.05
V_{TH} (V)	0.61	0.62	0.63	0.65

Figure 14 illustrates the performance ratio of N-channel FinFET, we note that I_{ON}/I_{OFF} decreases down to $1.66x10^{6}$ with W_{fin} = 9 nm then, the performance ratio increases up to $4x10^{8}$.The increase of the performance ratio is due to the decrease of leakage current [2].

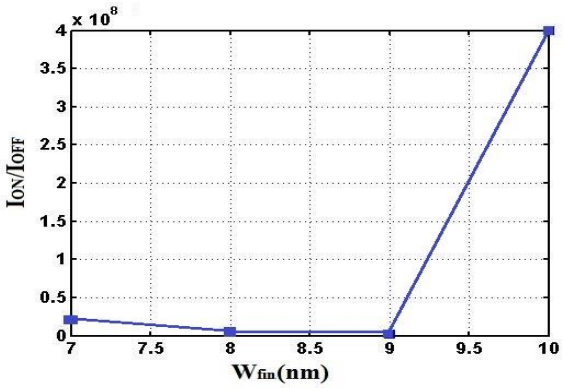


Fig. 14 Impact of width fin on the performance N-channel FinFET

Transistor dimensions are scaled down in order to improve drive current and circuit speed and the ratio I_{ON}/I_{OFF} is needed to exceed 10^6 [2].

The suitable value of fin width on N-channel FinFET is 10 nm because it has the best performance ratio $4x10^8$.

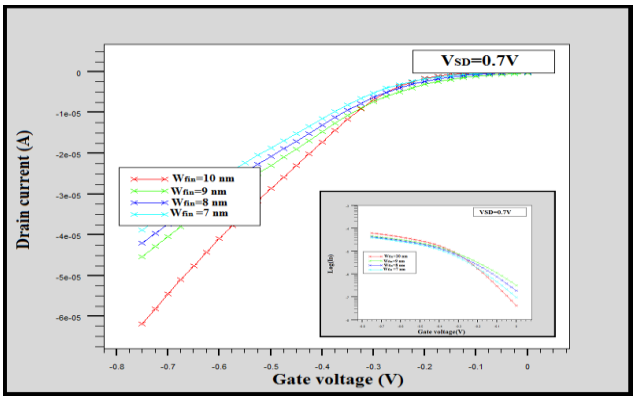


Fig. 15 Impact of fin width on P-channel FinFET

Figure 15 represents the impact of fin width on the transfer characteristics of P-channel FinFET, we note that the ON current increases and the maximum value is $6.25x10^{-6}$ A.

The increase of fin width increases the leakage current in the device after W_{fin}=9 nm because direct tunneling current is more important than trap-assisted-tunneling.

Figure 16 represents the impact of fin width on performance ratio of P-channel FinFET. We notice that the performance of device decreases with increasing fin width up to 9 nm, then above this value, it starts to increase [2].

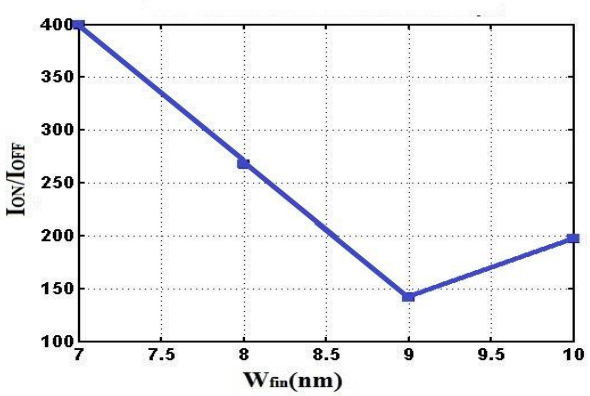


Fig. 16 Impact of fin width on the performance ratio of P-channel FinFET

Table 8 represents the different results of subthreshold swing and V_{TH} of P-channel FinFET:

Table 8 Impact of Fin width of P-channel FinFET.

Parameter	7 nm	8 nm	9 nm	10nm
SS (mV/dec)	168.75	175.01	132.01	137.25
V_{TH} (V)	0.27	0.28	0.33	0.35

The increase of threshold voltage is due to the presence of the sub bands. The quantum confinement raises the conduction band edge, E_C, to the lower order eigenvalues. This shift has a direct influence on the device threshold voltage because as it requires more band bending (potential energy lowering) in order to create the inversion layer [10].

The variation of subthreshold swing is due to the total capacitance of the device [7]. The suitable value of fin width in P-channel FinFET is 7 nm because it has a larger performance ratio of $4x10^2$.

5. Discussion and Conclusion

Throughout this study, we have shown that both N- and P-channel FinFETs have good performance ratios only when short-channel effects are minimized.

We have also shown that the BQP algorithm is a good simulation tool for computing parameters that control the quantum effects. It also allows the calculation of the optimal geometrical parameters for optimal performance of devices that can be implemented in CMOS circuits.

The results show that in order to have a good threshold voltage, one needs to increase the fin height that allows the increase of the energy level of the sub-bands.

To minimize the SCEs, the subthreshold swing must be around 60 mV/dec and the total capacitance must be decreased in both devices by using high-k oxides and wide thicknesses.

The integration of tri-gate SOI FinFET provides new opportunities in achieving high performance in CMOS technology. This requires the improvement of certain parameters such as leakage currents and the control the threshold voltages.

We have also shown that the device characteristics depends on fin widths and fin heights. As a result, 10 nm FinFET with hafnium dioxide using quantum confinement can be considered as a promising device for future CMOS manufacturing process. Our results can be used as Spice parameters for PTM in CMOS inverter design.

Acknowledgments: *The author Lazzaz wishes to thank Professor Ghibaudo of INP Grenoble and Professor Pierpaolo Palestri for their very helpful pieces of advice.*

REFERENCES

[1] B. Yu, L. Chang, S. Ahmed, H. Wang, S. Bell, C. Yang, D. Kyser, "FinFET scaling to 10 nm gate length", In Digest of the IEEE International Electron Devices Meeting, 2002, pp. 251-254.

[2] Y. Eng, L. Hu, T. Chang, S. Hsu, C. Chiou, T. Wang, M. Chang, "Importance of $\Delta DIBLSS/(Ion/Ioff)$ in evaluating the performance of n-channel Bulk FinFET Devices", *IEEE Electron Devices Society*, vol. 6, pp. 207-213, January 2018.

[3] M. Lundstorm, "Fundamentals of Nano transistors (Lessons from Nanoscience: A Lecture Notes)", WSPC, 2015, pp. 05-334

[4] J. Baker, "CMOS Circuit Design,Layout and Simulation, 3rd Edition (IEEE Press Series on Microelectronic Systems)". Wiley-IEEE Press, 2010, pp. 187-188.

[5] A. Tsormpatzoglou, "Characterization and modeling of modeling nanoscale multi-gate MOSFETs", Ph.D dissertation, Institut polytechnique de Grenoble, Grenoble, France, 2009.

[6] N. Collaert, "High mobility materials for CMOS applications", Woodhead Publisching series in Electonic and Optical Materials (1reed), Ed. Woodhead Publishing, 2018, pp. 297-298.

[7] Y. Chauhan, D. Lu, S. Venugopalan, S. Khandelwal, J. Duarte, N. Paydavosi, C. Hu, "FinFET modeling for IC simulation and design": Using the BSIM CMG Standard (1re éd), Ed. Academic Press, pp. 131-135, 2015.

[8] G. Iannaccone, G. Curatola, G. Fiori, "Effective Bohm Quantum Potential for device simulators based on drift-diffusion and energy transport", *Simulation of Semiconductor Processes and Devices*, Springer, Vienna, pp. 275-278, 2004.

[9] I. Buryk, M. Ivashchenko, A. Golovnia, A. Opanasyuk, "Numerical Simulation of FET Transistors Based on Nanowire and Fin Technologies", *IEEE*, pp. 257-259, 2020.

[10] W. Han, Z. Wang, "Toward Quantum FinFET", *Springer*, pp. 54-67, 2013.

[11] A. Zhang, J. Mei, L. Zhang, H. He, J. He, M. Chan, "Numerical study on dual material gate nanowire tunnel field-effect transistor", In proceedings of the 2012 IEEE International Conference on Electron Devices and Solid State Circuit (EDSSC), 2012, pp. 1-5.

[12] A. Kumar, S. Saini, A. Gupta, N. Gupta, M. Tripathi, R. Chaujar, "Sub-10 nm High-k Dielectric SOI-FinFET for HighPerformance Low Power Applications", In Proceedings of the 2020 6th International Conference on Signal Processing and Communication (ICSC), 2020, pp. 310-314.

[13] N. Bourahla, A. Bourahla, B. Hadri, "Comparative performance of the ultra-short channel technology for the DG-FinFET characteristics using different high-k dielectric materials", *Indian Journal of Physics*, pp. 1-8, 2020.

[14] C. Hu, "3D FinFET and other sub-22 nm transistors", In Proceedings of the 19th IEEE International Symposium on the Physical and Failure Analysis of Integrated Circuits, 2012, pp. 1-5.

[15] K. Kuhn, "CMOS scaling for the 22 nm node and beyond: Device physics and technology". In Proceedings of 2011 IEEE International Symposium on VLSI Technology, Systems and Applications, pp. 1-2, 2011.

[16] N. Boukortt, B. Hadri, S. Patane, "Investigation on TG n-FinFET parameters by varying channel doping concentration and gate length. Silicon", vol. 9, no. 6, pp. 885-893, 2017.

[17] A. Rassekh, M. Fathipour, "A single-gate SOI nanosheet junctionless transistor at 10-nm gate length: design guidelines and comparison with the conventional SOI FinFET", *Journal of Computational Electronics*, vol. 19, no. 2, pp. 631-639, 2020.

[18] O. Bonnaud, "Physique des Solides, des Semiconducteurs et Dispositifs. Université de Rennes", vol. 1, p. 78, 2003.

[19] K. Ren, Y. Liang, C. Huang, "Compact physical models for AlGaN/GaN MIS-FinFET on threshold voltage and saturation current", *IEEE Transactions on Electron Devices*, vol. 65, no 4, pp. 1348-1354, 2018.

[20] C. Mohan, S. Choudhary, B. Prasad, "Gate all around FET: An alternative of FinFET for future technology nodes", *International Journal Adv. Res. Sci. Eng.*, vol. 6, no. 7, pp. 563-569, 2017.

[21] A. Lazzaz, K. Bousbahi, M. Ghamnia, "Modeling and Simulation of DG SOI N FinFET 10 nm using Hafnium Oxide", In Proceedings of the IEEE 21st International Conference on Nanotechnology (NANO 2021), 2021, pp. 177-180.

[22] N. Maity, R. Maity, S. Baishya, "Voltage and oxide thickness dependent tunneling current density and tunnel resistivity model: application to high-k material HfO2 based MOS devices", *Superlattices and Microstructures*, vol. 111, pp. 628-641, 2017.

[23] N. Maity, R. Maity, R. Thapa, S. Baishya, "A tunneling current density model for ultra thin HfO2 high-k dielectric material based MOS devices", *Superlattices and Microstructures*, vol. 95, p. 24-32, 2016.

[24] N. Boukortt, "3-D Simulation of Nanoscale SOI n-FinFET at a Gate Length of 8 nm Using ATLAS SILVACO", *Transaction on electrical and electronic materials*, vol. 16, pp. 156-161, June 2015.

[25] N. Bourahla, A. Bourahla, B. Hadri, "Comparative performance of the ultra-short channel technology for the DG-FinFET characteristics using different high-k dielectric materials", *Indian Journal of Physics*, vol. 95, no. 10, pp. 1977-1984, 2021.

[26] D. Tripathy, D. Acharya, P. Rout, S. Biswal, "Influence of Oxide Thickness Variation on Analog and RF Performances of SOI FinFET", *Facta Universitatis, Series: Electronics and Energetics*, vol. 35, no 1, p. 001-011, 2022.

[27] A. Lazzaz, K. Bousbahi, M. Ghamnia, "Optimized mathematical model of experimental characteristics of 14 nm TG N FinFET", *Micro and Nanostructures*, p. 207210, 2022.

[28] N. Gupta, A. Kumar, "Assessment of high-k gate stack on sub-10 nm SOI-FinFET for high-performance analog and RF applications perspective", *ECS Journal of Solid-State Science and Technology*, vol. 9, no. 12, p. 123009, 2020.

[29] A. Rahman, J. Dacuna, P. Nayak, Pinakpani, "Reliability studies of a 10 nm high-performance and low-power CMOS technology featuring 3rd generation FinFET and 5th generation HK/MG", In Proceedings of the IEEE International Reliability Physics Symposium (IRPS 2018), p. 6F. 4-1-6F. 4-6, 2018.

[30] M. Aditya, K. Rao, Srinivasa, K. Sravani, "Design, simulation and analysis of high-K gate dielectric FinField effect transistor", *International Journal of Nano Dimension*, vol. 12, no 3, pp. 305-309, 2021.

[31] M. Ahmed, S. Islam, D. Al Mamun, "Numerical Simulation of the Electrical Characteristics of Nanoscale TG n-FinFET with the Variation of Gate Dielectric Materials", *International Journal of Semiconductor Science & Technology (IJSST)*, vol. 11, no. 3, 2021.

[32] S. Sinha, G. Yeric, V. Chandra, B. Cline, Y. Cao, "Exploring sub-20 nm FinFET design with predictive technology models", In Proceedings of the IEEE DAC Design Automation Conference, 2012, pp. 283-288.