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PERFORMANCE ANALYSIS OF FINFET BASED INVERTER, NAND AND NOR CIRCUITS AT 10 NM ,7 NM AND 5 NM NODE TECHNOLOGIES

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Abstract. *Advancement in the semiconductor industry has transformed modern society. A miniaturization of a silicon transistor is continuing following Moore's empirical law. The planar metal-oxide semiconductor field effect transistor (MOSFET) structure has reached its limit in terms of technological node reduction. To ensure the continuation of CMOS scaling and to overcome the Short Channel Effect (SCE) issues, a new MOS structure known as Fin field-effect transistor (FinFET) has been introduced and has led to significant performance enhancements.*
This paper presents a comparative study of CMOS gates designed with FinFET 10 nm, 7 nm and 5 nm technology nodes. Electrical parameters like the maximum switching current I_{ON}*, the leakage current* I_{OFF}*, and the performance ratio* I_{ON}/I_{OFF} *for N and P FinFET with different nodes are presented in this simulation.*
The aim and the novelty of this paper is to extract the operating frequency for CMOS circuits using Quantum and Stress effects implemented in the Spice parameters on the latest Microwind software. The simulation results show a fitting with experimental data for FinFET N and P 10 nm strctures using quantum correction. Finally, we have demonstrate that FinFET 5 nm can reach a minimum time delay of t_d*=1.4 ps for CMOS NOT gate and* t_d*=1 ps for CMOS NOR gate to improve Integrated Circuits IC.*

Key words: *FinFET, Quantum effect, CMOS NOT gate, CMOS NOR gate, CMOS NAND gate, Microwind*

1. INTRODUCTION

The rapid development of nanoelectronics technology is closely related to solving the problem of minimum layout dimensions. The efficient miniaturization of a transistor has been one of the most important topic for integrating a greater number of electronic components in a single chip.

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FinFET is one of the best alternative for replacing MOSFET which encounter the problem of the SCE like Drain Induced Barrier Lowering (DIBL), and the increase of leakage current when the channel length is reduced below 32 nm. Researchers around the world have tried to improve the performance of FinFETs by the introduction of high k dielectric materials and strained silicon technology [1].

Since the conventional MOSFET has reached its limit, the multi gate FinFET has been one of the most promising devices for CMOS technology and the different analytical studies of FinFET is a current topic of research in large foundries like TSMC[6], Samsung and Intel, they are aiming to create the most efficient CMOS circuits.

Shiqi Liu et *al.* in 2021[21] have simulated an ultra-thin Si FinFET with a width of 0.8 nm by using ab initio quantum transport simulations. The results of their simulation confirm that even with the gate length down to 5 nm, the on-state current, delay time, power dissipation, and energy-delay product of the optimized ultra-thin Si FinFET still meet the high-performance applications.

Dhananjaya Tripathy et *al* in 2022 [22] have examined the impact of variation in the thickness of the oxide (SiO_2) layer on the performance parameters of a FinFET. The results confirm that a rise in SiO_2 thickness improves the energy and power dissipation of FinFET.

Lazzaz et *al.* in 2022 [23] have simulated a theoretical model based on the Bohm Quantum Potential (BQP) theory and compared it with experimental data. The theory fits with the experiment after optimization and correction using the right values of the geometric parameters.

Bourahla et *al.* in 2021 [24] have demonstrated that the Ta_2O_5 material of gate with high permittivity (k = 27) turns out better values for performance parameters such as (V_{TH}, SS, I_{ON}, I_{OFF} current and I_{ON}/I_{OFF} ratio current, gm, and electrical field (E)) in comparison with other dielectrics such as SiO_2, SnO_2, ZrO_2 which improve the performance of the device.

Lazzaz et *al.* in 2021 [2] have demonstrated the impact of the metal gate work function on the performance of the DG FinFET 10 nm with SILVACO TCAD tools.

Uttam Kumar Das et *al.* in 2021 [25] have examined a comparative study between Silicon FinFET With Carbon Nanotube and 2D-FETs for Advanced Node CMOS Logic Application.The results of this simluationn confirm that the FinFET delivers more than three times higher drive current, as well as five times better energy-delay performances.

Rajeev Ratna Vallabhuni et *al.* in 2020 [26] have simulated a 2-bit comparator designed with 18nm FinFET technology. The simulation shows the CMOS comparator in terms of power and delay using the Cadence Virtuoso tool. The result of this simulation confirm that FinFET can be used where a fast switching rate is required, to improve the efficiency of control devices and to make compact device.

J. Jena et *al.* in 2022 [27] have simulated FinFET-Based Inverter Design and Optimization for 7 nm Technology Node. The result of their simulation confirm that according to the sidewall orientation (<100 > or < 110>), the amount of mobility enhancement of both the electrons and holes results in more than 100% (>100%) and less than 25% (<25%) respectively.

C. Auth et *al.* in 2017 [32] have an industry leading 10 nm CMOS technology node with excellent transistor such as FinFET with interconnect performance and aggressive design rule scaling.The results of their simulation show a higher performane high density SRAM featuring 0.0312µm² cell size fabricated using all 10 nm process features.

S.Panchanan et *al*. in 2021 [35] have simulated an analytical model of Tri-gate metal-oxide-semiconductor field effect transistor (TG MOSFET) for short channel lengths

below 10 nm using TCAD software. The model is examined by varying channel length, oxide thickness, gate voltage, drain voltage and doping concentration. The result of their simulation confirm that to obtain identical surface potentials, the oxide thickness of HfO_2 must be larger than SiO_2. Unlike SiO_2, the minima of surface potential remain constant with channel length for HfO_2.

B. Vandana et *al.* in 2018 [36] have explored the analog analysis and higher order derivatives of drain current (I_D) at gate source voltage (V_{GS}), by introducing channel engineering technique of 3D conventional and Wavy Junctionless FinFETs (JLT) as silicon germanium ($Si_{1-0.25}Ge_{0.25}$) device layer. The results of their simulation confirm that a better channel controllability over the gate is observed for Wavy structures and high I_D is induced as L_G scales down.

N. P. Maity et *al.* in 2019 [37] have simulated A double-gate (D_G) heterojunction tunnel FinFET structure with a source overlap region to optimize its performance and validate its Technology Computer-Aided Design (TCAD) simulation results by modeling of the surface potential, electric field, and threshold voltage.

Suparna Panchanan et *al.* in 2021[38] have analysed an analytical model for surface potential and threshold voltage for undoped (or lightly) doped Tri-gate Fin. Field Effect Transistor (TG-FinFET) is proposed and validated using transistor computer aided design (TCAD) simulation.

Suparna Panchanan et *al.* in 2022 [39] have studied Lambert W function-based a drain current model of lightly doped short channel tri-gate fin fashioned field effect transistor (TG-FinFET). Their results confirm that A precise drain current is obtained by adding quantum mechanical effect (QME) which also improves the efficiency of the model.

Shaheen Saleh et *al.* in 2018 [41] have demonstrated the roles and impacts of various effects and aging mechanisms on FinFET transistors compared to planar transistors on the basic approach of the physics of failure mechanisms to fit to a comprehensive aging model.

So, the above literature survey indicates the importance of using high-k dielectrics in FinFET devices and the importance of multi gate FinFET to overcome the SCE and to improve the channel control.

In this paper, we present a comparative study of different CMOS gates (Not gate, NAND and NOR gate) based on 10 nm, 7 nm and 5 nm technology node to extract optimul geometric parameters to have an operational FinFET device for future applications like SRAM circuits.

2. DEVICE STRUCTURE AND SIMULATION

Tri Gate (TG) FinFET technology is based on the vertical Fin represented by the Fin length (L), Fin height (H_{fin}) and Fin width (W_{fin}) as show in Figure 1.

FinFET devices have been used in a variety of innovative digital and analog circuit designs. TG (Tri gate) has been recently developed and its ability to control three channel sides has been used in order to reduce circuit area, its capacitance and the variation of the threshold voltage.

Throughout the last few years, CMOS scaling and improvement in processing technologies have led to continuous enhancement in circuit speeds due to the miniaturization of FinFET device. The main difference between the BULK FinFET and SOI FinFET is the buried oxide (BOX) which isolate the body from the subtrate, minimizes the leakage current due to quatntum effect, reduces the parasitic junction capacitance and source/drain capacitance.

Despice the use of the SOI FinFET technology in term of enhancement of the device, one of the drawbacks is the self heating effect because the active thin body is on silicon oxide which is good thermal insulator. During an operation, the power consumed by the active region cannot be dissipated easily therefore, the temperature of thin body rises and this decreases the mobility and the current of the device [32].

In this work, FinFET structure has been simulated with Microwind 3.8 Software using parameters that are provided in table 1. Figure 1 in the right shows the 3D schematic of simulated FinFET 10 nm and in the left Figure shows the design layout of the device:

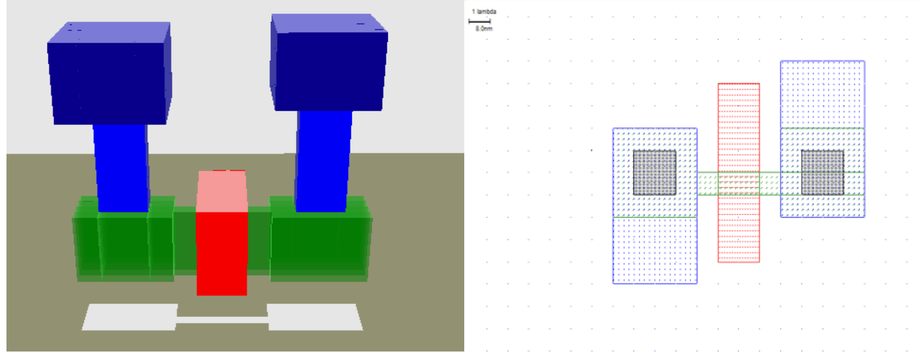


Fig. 1 N FinFET 10 nm

Table 1 Different parameters of the simulated device [6] [7][12]

Notation	Description	FinFET 10 nm	FinFET 7 nm	FinFET 5 nm
L_S,L_D	Length of drain /source	22nm	16 nm	12 nm
L_G	Gate length	18 nm	16 nm	14 nm
t_{ox}	Oxide thikness	1 nm	0.9 nm	0.9 nm
H_{Fin}	Fin height	46 nm	46 nm	46 nm
W_{Fin}	Fin width	7 nm	6 nm	5 nm

Table 1 shows the design parameters that we have employed for the circuit simulations in our present work.

The primary obstacles to the scaling of CMOS gate lengths to 10 nm and beyond are short channel effect and leakage current which lead to low yield. FinFET offers better control over of the SCE and hence overcome the obstacles of scaling.

The circuit simulation is done using Microwind 3.8 which we have used to simulate electrical circuits in transient domain. Microwind tool facilitates circuit level analysis of performance simulation of the integrated circuits. The Predictive Technology Model (PTM) integrated in Microwind provides accurate, customizable, and predictive model files for future transistor and interconnect technologies[28][29].

We have simulated different logic circuits such as the NOT gate,2 input NAND and 2 input NOR gates for leakage power dissipation, delay time and power delay product (PDP) at 10 nm, 7 nm and 5 nm technology nodes and a comparison is made to check the technology scaling.

The threshold voltage expression can be represented by the following equation [11]:

$$V_{TH} = \phi_{ms} + 2\phi_f + \frac{Q_D}{C_{OX}} + \frac{Q_{SS}}{C_{OX}} + V_{in} \quad (1)$$

ϕ_{ms}: work functions difference between gate and Fin, Q_{SS}: charge in the gate dielectric, C_{OX}: Oxide capacitance, Q_D: depletion charge, ϕ_f : fermi potential V_{in} : input voltage.

Power dissipation plays a crucial role in the overall performance of the circuits in sub 10 nm regime and it represents an important performance metric to check the effectiveness of the proposed technique.

Time delay is a performance metric to evaluate the switching speed of the circuit, it is calculated by following equation [9]:

$$t_d = \frac{t_{phl} + t_{plh}}{2} \quad (2)$$

t_{phl}: high to low transition delay; t_{plh}: low to high transition delay.

Leakage power dissipation is also an important parameter for research designers because it affects performance and reliability of the electronic device. The leakage power dissipation is calculated using following equation [8]:

$$P_{leakage} = V_{DD} \times I_{leakage} \quad (3)$$

where V_{DD} is supply voltage and $I_{Leakage}$ is the leakage current.

Scaling of FinFET plays a very important step in FinFET structure where the scaling factor λ is given in following equation [6]:

$$\lambda = W_{fin} + 2t_{ox} \quad (4)$$

W_{fin}: fin width; t_{ox}: oxide thickness.

PDP (Power Delay product) is an essential requirement for better performance of the circuits. Technology scaling increases power dissipation and delay values Therefore, lowest value of PDP depicts better performance at the scaled technology nodes. PDP is given by following equation [17]:

$$\text{PDP} = \text{Power dissipation x delay} \quad (5)$$

The following equation represents the drain current equation on the sub-threshold mode used in this simulation:

$$I_{DS} = I_{DS}(V_{on}, V_{ds}) e^{\left(\frac{q(V_{GS}-V_{on})}{nkT}\right)} \quad (6)$$

V_{GS}: gate source voltage , n: body coefficient , k: Boltzman coefficient , T:temperature, q:electron charge.

$$Ids0 = \frac{W_{eff}}{L_{eff}} \mu_{eff} \frac{\varepsilon_0 \varepsilon_r}{TOXE} V_{gsteff} \left(1 - \frac{A_{bulk} V_{dseff}}{(2V_{gsteff} + 4.vt)}\right) \frac{V_{dseff}}{\left(1 + \frac{V_{dseff}}{\varepsilon_{sat} L_{eff}}\right)} \quad (7)$$

W_{eff}: effective width, L_{eff}: effective length , ε_0: vacuum permittivity, ε_r: relative permittivity, TOXE: oxide thichness, V_{gsteff}: gate source effective voltage, V_{dseff}: drain source effective voltage, ε_0: Saturation permittivity, v: carrier velocity.

In 3D nanochannel devices, the SCE modifies the drain current expression by a correction factor CF for the post-threshold voltage regime:

$$CF = \frac{\lambda}{\lambda + L} \tag{8}$$

λ : Mean free path, L: channel lengh, CF: is also called transition coefficient.

Figure 2 represents the transfer characteristics of N FinFET 10 nm and illustrates a comparison between the theoretical and experimental transfer characteristics in subthreshold regime. The gate voltage is swept from 0 V to 0.8 V for different drain values 0.05 V, 0.1 V and 0.2 V. The maximum value of drain current represents the ON current when V_{GS}= V_{DD}=0.8 V and the value of ON current is 10.5 µA.The leakage current is 2.75 nA and it represents the value of the current when V_{GS}=0.

To fit the experimental results, the drain current is modified by correction factor CF represented in equation 8. This coeffcient represents the transport mode transition factor. The transport is quasi balistic in the channel. This transition coefficient takes into consideration the type of charge carrier N or P therefore, the correction value distinguished between both structures.

The fitting of the simulated results with the experimental data is due to the quantum correction that gave a good convergence between two curves. The cacultated parameters are used to compute the means free path used in the equation number (8) such as, effective mobility in th N channel, diffusion coefficient and unidirectional thermal velocity.

The electron carrier mobility used in this simulation of N FinFET 10 nm is 350 cm²/V.S. The average mobility value has been extracted from Berkley Spice model for FinFET 10 nm [28].

It is noted that for the gate voltages 0.1 V and 0.2 V, the simulation curves fit very well with the experimental [31], there is therefore a good convergence between the theoretical model and the experimental points curves at these gate voltages. The discrepancy at 0.4 V and 0.5 V voltages can be explained by the presence of complex scattering phenomena which are very difficult to model.

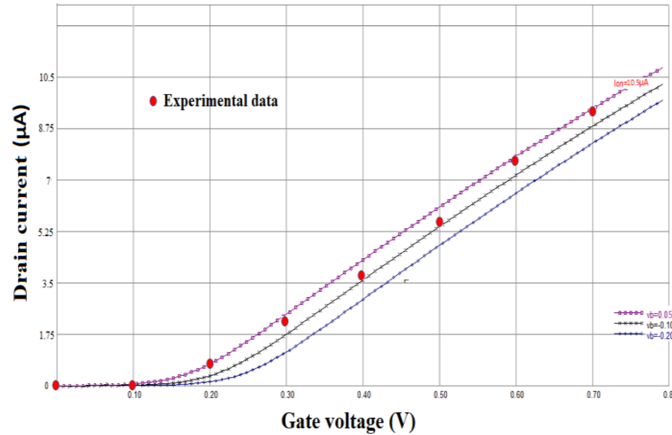


Fig. 2 Transfer characteristics of N FinFET 10 nm [31]

Figure 3 represents transfer characteristics of P FinFET 10 nm and illustrates a comparison between the theoretical and experimental transfer characteristics. We note that the ON current is 50 µA and the leakage current is 44.76 nA. The threshold voltage in this simulation is 0.20 V and the decrease of threshold voltage is due to the increase of the Quasi-Fermi level. The values of drain voltage have been chosen to calculate the threshold voltage and to fit the curve with experimental data [31].

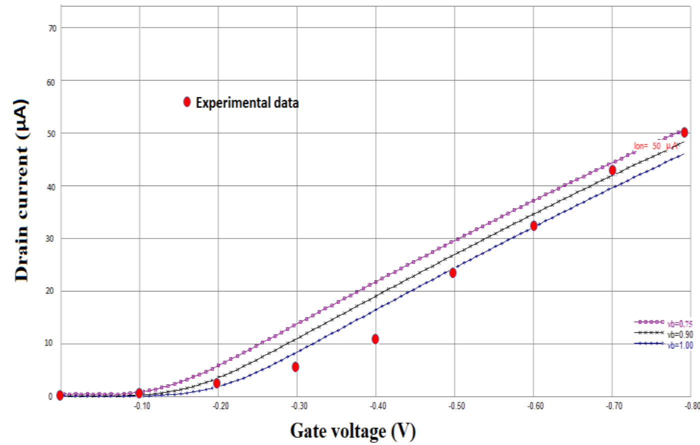


Fig. 3 Transfer characteristics of P FinFET 10 nm

Figure 4 represents the transfer chrematistics of N FinFET 7 nm, we note that ON current is 0.306 mA and leakage current is I_{OFF} is 82.536 nA.

Various low static power technology needs higher threshold voltage but the miniaturization of integrated circuits and channel length decreases the threshold voltage. The threshold voltage in this simulation is 0.22V [33].

The leakage current in this simulation of N FinFET 7 nm is lower than calculated by Suyog Gupta et *al* [4].

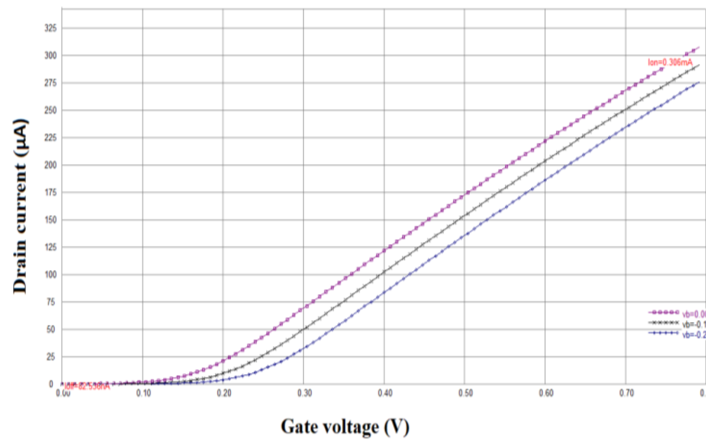


Fig. 4 Transfer characteristics of N FinFET 7 nm

Figure 5 represents the transfer characteristics of P FinFET 7 nm, we note that I_{ON} is 0.250 mA and leakage current is I_{OFF}= 221.571 nA.

We note that ON current in this simulation of P FinFET 7nm is higher than calculated in T.Dash et *al* [18] and leakage current is lower than calculated by Suyog Gupta et *al* [4].

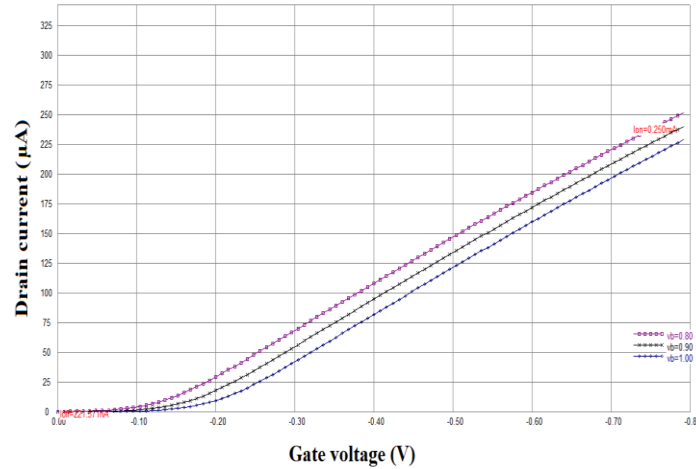


Fig. 5 Transfer characteristics of P FinFET 7 nm

Figure 6 represents transfer characteristics of N FinFET 5 nm, we note that the ON current is 0.240 mA and the leakage current is 81.694 nA.

The threshold voltage is 0.23 V for this simulation and the increase of its value is due to the fermi level and to have better threshold voltage, we need to increase the Fin height [3][14].

ON current in this simulation is higher than calculated by N. P. Maity et *al* [5].

We can control and minimize the leakage current in this structure with different channel length by optimizing the geometric parameters in order to have optimal results.

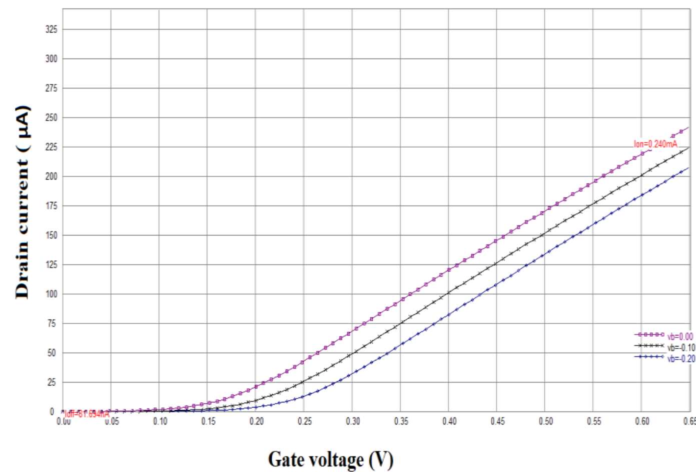


Fig. 6 Transfer characteristics of N FinFET 5 nm

Figure 7 represents the transfer characteristics of P FinFET 5 nm, we note that the maximum current I_{ON} is 0.199 mA and leakage current is 219.31 nA.

We think that the problem to the increase of the leakage current is the leaked quantum confinement and the choice of geometric parameter like the gate oxide which leads to the raising of the conduction band, so we need more potential to create an inversion layer [13].

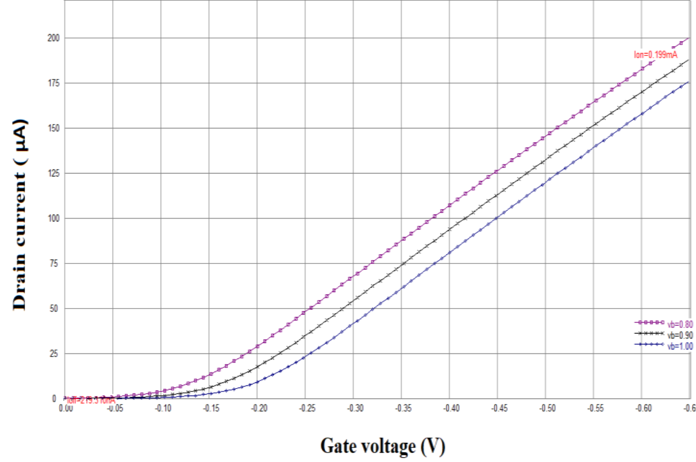


Fig. 7 Transfer characteristics of P FinFET 5 nm

The following table 2 represents the performance ratio I_{ON}/I_{OFF} the threshold voltage V_{TH} and DIBL calculated for different structures of FinFET 10 nm, 7 nm and 5 nm [10]. The table presents a comparatice study with International Roadmap for Device and Systems (IRDS) results [30].The supply voltage for FinFET 10 nm and 7 nm is 0.8 V and 0.65 V for FinFET 5 nm.These parameters are extracted from Berkley Spice model [28].

Table 2 Performance ratio of FinFET 10 nm,7 nm and 5nm

Device	FinFET 10 nm	FinFET 7 nm	FinFET 5 nm
I_{ON}/I_{OFF} values for N structure	3818.18	3707.36	2937.79
I_{ON}/I_{OFF} values for P structure	1117.6	1128.30	907.36
V_{TH} (V) for N structure	0.24	0.22	0.23
V_{TH} (V) for P structure	0.20	0.20	0.22
I_{ON}/I_{OFF} for N strcture (IRDS)[30]	950	930	840
DIBL N FnFET (mV/V)	49.5	45.5	40.5
DIBL P FinFET (mV/V)	50.5	46.5	41.5

We note that the better performance ratio of N FinFET is for FinFET 7 nm due to the leakage current and the higher ratio performance of P FinFET is for FinFET 10 nm due to the minimum strain effect of ON current.

3. CMOS GATES DESIGNS

This paper has considered three design styles for digital logic circuits structures using FinFETs. The circuit diagram of different FinFET-based NOT gate, NAND, NOR gate designs along with the ordinary CMOS is shown in the Figure 8.

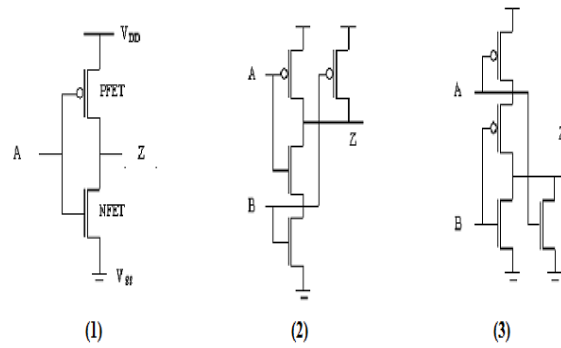


Fig. 8 (1): NOT gate, (2): CMOS NAND, (3) CMOS NOR [8]

The three different circuits of CMOS (NAND NOR and inverter) based of FinFET have been analyzed using the Microwind 3.8 tool. The first step is the implementing of three different circuits of FinFET based NAND and NOR gates in order to create the layout styles [16].

The design rule must be checked before applying the inputs. The design rule which is used in this simulation is lambda-based design rule. The value of lambda is fixed to 8 nm [6] [15].

Figure 9.a represents the layout design of CMOS Not gate with FinFET 5 nm using Microwind 3.8 and figure 9.b represents the structure of CMOS Not gate in 3D with FinFET 5nm.[19]

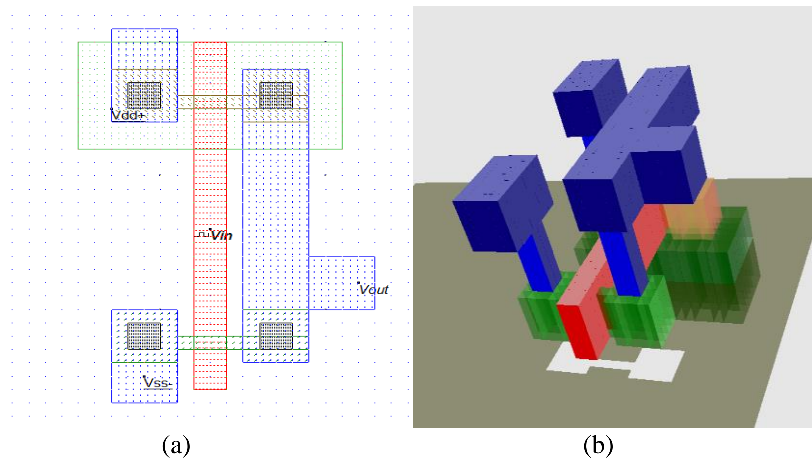
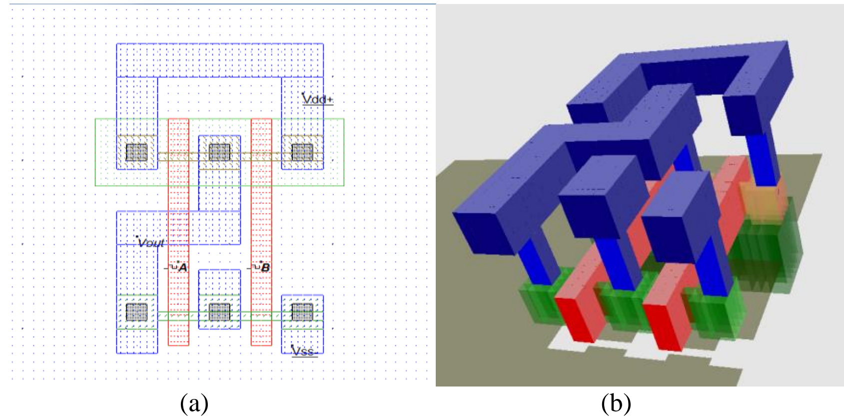


Fig. 9 (a) Design layout CMOS inverter , (b) CMOS inverter 3D structure

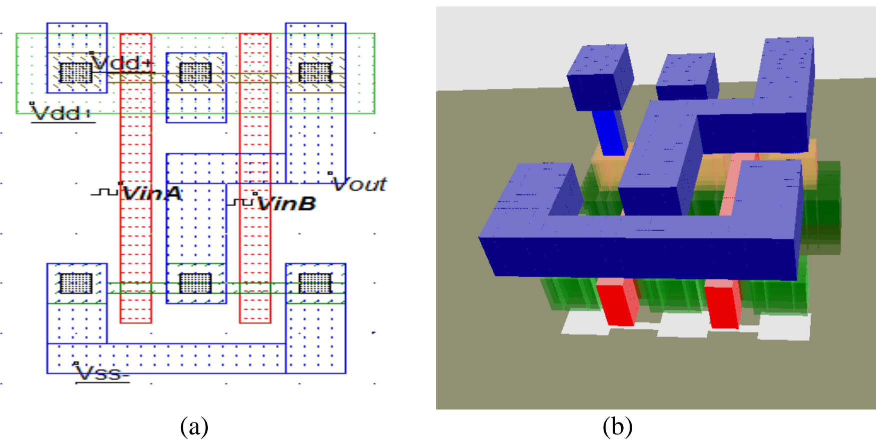
Figure 10.a represents the design layout of CMOS NAND with FinFET 5 nm using Microwind 3.8 and figure 10.b represents the structure of CMOS NAND in 3D with FinFET 5nm.



(a) (b)

Fig. 10 (a) Design layout CMOS NAND gate, (b) CMOS NAND 3D structure

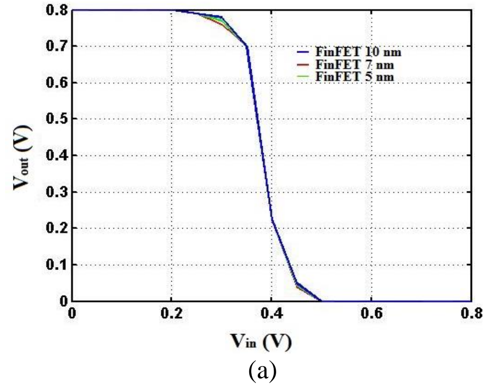
Figure 11a represents the design layout of CMOS NOR gate with FinFET 5nm using Microwind 3.8 and figure 10.b represents the structure of CMOS NOR gate in 3D with FinFET 5nm.



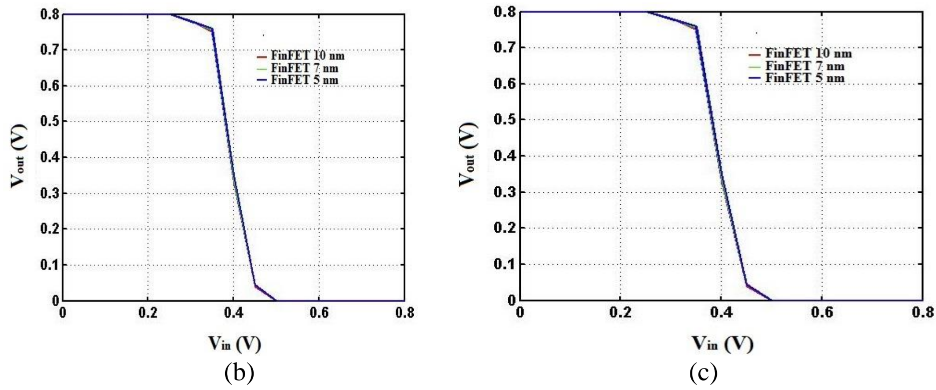
(a) (b)

Fig. 11 (a) Design layout CMOS NOR gate, (b) CMOS NOR gate 3D structure

Figure 12 represent the different VTC curves of different CMOS circuits:



(a)



(b) (c)

Fig. 12 (a) VTC curves of CMOS NOT GATE, (b) VTC curves of CMOS NOR GATE, (c) VTC curves of CMOS NAND GATE

Noise margin is a measure of design margins to ensure circuits operation within specified conditions and it is closely related to the DC transfer curve [40]. This parameter allows to determine the allowable noise voltage on the input of a gate so that the output will not be corrupted.

The specification most commonly used to describe noise margin (or noise immunity) uses two parameters: the low noise margin NM_L and the High noise margin NM_H [8]. Table 3 represents calculated parameter from VTC (Voltage Transfer Curve):

Figure 13 represents the values of Power Delay Product (PDP) with different CMOS gates. We note that the better value of PDP in NOT gate is for FinFET 5 nm and for CMOS NAND, NOR gates is FinFET 7 nm.

Table 3 Calculated parameters of different CMOS FinFET gates

Device	FinFET NOT gate			FinFET NAND gate			FinFET NOR gate		
Technlogy node	10 nm	7 nm	5 nm	10 nm	7 nm	5 nm	10 nm	7nm	5 nm
V_{DD}	0.80	0.8 0	0.65	0.80	0.80	0.65	0.80	0.80	0.65
V_{SP}(V)	0.385	0.385	0.386	0.397	0.391	0.3999	0.379	0.373	0.371
V_{IL}(V)	0.3243	0.3243	0.3189	0.3445	0.3445	0.3351	0.3148	0.3189	0.3202
V_{OH}(V)	0.7750	0.7687	0.7656	0.7509	0.7562	0.7562	0.7187	0.7718	0.7562
V_{IH}(V)	0.4378	0.4391	0.4418	0.4513	0.4472	0.4472	0.4189	0.4216	0.4437
V_{OL}(V)	0.0531	0.0406	0.0406	0.0375	0.0437	0.0406	0.0343	0.05	0.0437
NM_L(V)	0.2712	0.2836	0.2782	0.3070	0.3007	0.2944	0.2804	0.2689	0.2764
NM_H(V)	0.3372	0.3296	0.3238	0.2996	0.3090	0.3090	0.2998	0.3502	0.3125
t_d (ps)	1.6	1.5	1.4	2.20	2.20	2.10	1.10	1.10	1.0
P(μW)	0.446	0.357	0.460	0.475	0.686	0.5950	0.325	0.416	0.401
PDP (10^{-18}W.s)	0.7136	0.5355	0.6440	1.0450	1.5092	1.2495	0.3575	0.4576	0.4010

P: power dissipation in static CMOS, PDP: Power Delay Product. t_d: time delay; V_{OL}: maximum low output voltage, V_{OH}: minimum high output voltage, V_{IL}: maximum low input voltage, V_{IH}: minimum high input voltage, V_{SP}: switching point voltage.

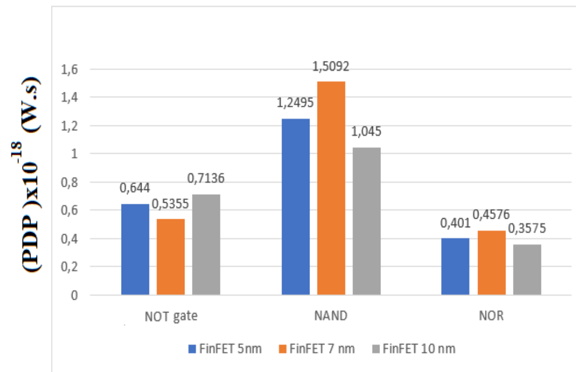


Fig. 13 Power delay product (PDP) for different CMOS gates

Figure 14 represents the values of times delay of different CMOS gates, we note that the optimal device is FinFET 5 nm due to the low time delay.

The results obtained for each of the digital application at 10 nm, 7 nm and 5 nm of FinFET shows a system tradeoff. We note that as we scale down the device from 10 nm to 5 nm, the time delay decreases because the supply voltage has been decreased [34].

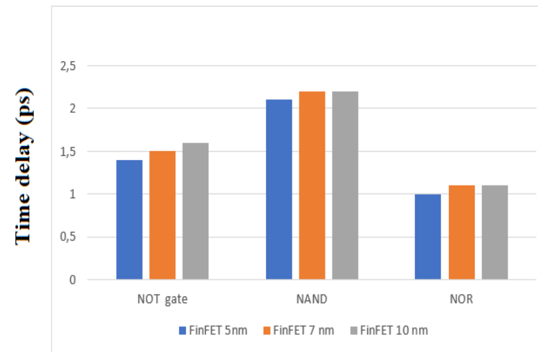


Fig. 14 Time delay for different CMOS gates

The fluctuation in power delay product (PDP) is due to the fluctuation of static power dissipation and it is a minor issue because the system reliability has improved [20].

CONCLUSION

As Ultra Large Semiconductor Integration (ULSI) moves towards new advancement, new challenges have been arisen such as SCE which are generated because of scaling of the transistors. From the simulation results, it has been observed that the leakage power dissipation is the major issue in modern semiconductor industry and FinFET devices have the advantages to overcome these issues. The simulation results for FinFET based digital application at nanometer regime of 10 nm ,7 nm and 5 nm technology are studied here in the educational tool Microwind and a comparative and analysis is carried out in this paper for comparison between the different nodes technology of FinFET device.

From the simulation results, one can conclude that the impact of the time delay and power dissipation product on CMOS based FinFET device are crutial parameters for improvements of the performance of CMOS circuits.

We confirm in this study that significant progresses have been made by introducing a new generation of 5 nm FinFET device which improves the switching performances and decrease the time delay as compared to different nodes such as 10 nm and 7 nm for CMOS circuits.

The results in this simulation confirm that the proper selection of supply voltage and geometric parameters is important for obtaining a high speed and stable CMOS circuits.

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