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ENHANCED DYNAMIC VOLTAGE CLAMPING CAPABILITY OF CLUSTERED IGBT AT TURN-OFF PERIOD

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Abstract. *One of the critical requirements for high power devices is to have rugged and reliable capability against hash operating conditions. In this paper, we present the dynamic voltage clamping capability of 3.3kV Field Stop Clustered IGBT devices under extreme inductive load condition. It shows that PMOS trench gate CIGBT structure with outstanding performance of fast turn-off time and low over-shoot voltage. Further optimization of current gain of CIGBT structure is analyzed through numerical evaluation. A step further in the safe operating area has been achieved for high voltage devices by CIGBT technology.*

Key words: *Insulated Gate Bipolar Transistor (IGBT), power semiconductor devices, Clustered IGBT*

1. INTRODUCTION

Similar to short circuit device failure, dynamic latch-up of high voltage IGBTs represents another practical failure mode during device turn-off under dynamic avalanche conditions. Overshoot of anode voltage occurs during device turn-off, especially for parallel connected power modules is very critical for IGBT operation and should be protected within the limited Safe Operating Area (SOA). Manufacturers and circuit designers have been trying to suppress the peak voltage by reducing anode current turn-off di/dt or de-rating and the use of voltage clamping circuits, snubbers to achieve sustainable capability. However, these methods unavoidably increase the turn-off switching loss, cost and the complexity of the system. The self-voltage clamping characteristics of IGBT have been reported in [1-4]. It must be capable of absorbing all the energy stored in the inductance during abnormal conditions [5]. It is important to develop IGBT without destruction even under the condition of dynamic avalanche [6].

During turn-off, the abruptly reduction of gate voltage seizes the injection of electron from the n-channel. The anode current continues to flow due to the inductive load. It must be sustained by the hole current. The hole carriers flows across the and modifies the

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effective carrier concentration in the N-drift region. The profile of electric field is determined by the Poisson equation in e.g. (1)

$$\frac{\mathrm{dE}}{\mathrm{dx}} = \frac{\rho_{\mathrm{tot}}}{\varepsilon_{\mathrm{s}}} = \frac{q_{\mathrm{e}}}{\varepsilon_{\mathrm{s}}} \times (\mathrm{N}_h - \mathrm{N}_e + \mathrm{N}_d) = \frac{q_{\mathrm{e}}}{\varepsilon_{\mathrm{s}}} \times \mathrm{N}_{\mathrm{eff}} \quad (1)$$

Wherein Neff is the effective carrier concentration in the N-drift region. These extra carriers lead to an increase in Neff. It can modify the profile of the electrical field and may force the device into a dynamic avalanche mode by the high peak electric field. This process is stable if the extra generated electrons and holes are balanced in numbers and will continue until all the remaining excess carriers are eliminated and subsequently, the dynamic avalanche mode is suddenly eliminated. Otherwise, the process can get out of control by the avalanche-generated carriers and would lead to a device failure.

Due to the stray inductance in the circuit, the IGBT anode voltage over-shoots and eventually the electric field could punch through the N-drift region. When the anode voltage reaches the DC bias voltage, the anode current begins to fall as the current is transferring to the diode in a rate depending on the stray inductance and peak anode voltage. The capability for the power devices to dissipate a large amount of power dissipated during the period could be improved by employing a high IGBT internal PNP gain, β [1]. More hole carriers will balance the effective carriers in the N-drift region, but this approach would have increased turn-off loss and higher leakage current in the off-state.

In this paper, we demonstrate the dynamic avalanche ruggedness of 3.3kV Field-Stop Clustered IGBT (CIGBT) [7-10] with self-voltage clamping capability. The technology shows improved safe and efficient operation and will ease the design constrictions on the system level.

2. Self-clamped Inductive Switching Capability

2.1. Device structure

CIGBT is a MOS-bipolar device employing a controlled thyristor concept to significantly reduce on-state voltage drop. It has the unique capability to clamp the cathode cell potential by punch-through of an n-well region between the P-base and P-well, termed as "self-clamping". The feature improves current saturation characteristics and enables better short circuit performance [11].

The single cell schematic structures of 3.3kV class, conventional, PMOS trench gate CIGBT and Field-Stop IGBT structures are shown in Fig. 1(a)-(c) respectively. The IGBT structure model is optimized for comparable purpose [11]. As a result, all structures have the same cell dimensions. The PMOS trench CIGBT [12], Fig. 1(b), is identical to that of the conventional CIGBT, Fig. 1(a), except that a PMOS trench gate (width=1μm, depth=4μm) connects the P-base to gate. The PMOS and NMOS gates are connected together to form a three terminal device. The PMOS channels are only conducted during the turn-off cycle when the gate voltage is negative and is used for hole current pass. A constant lifetime of 50μs is chosen for both electrons and holes and it is assumed that the edge termination does not have any impact upon device performance under this condition. The simulated CIGBT structures have only one full cell considered although in reality each cluster can consist of 50 to 100 cathode cells.

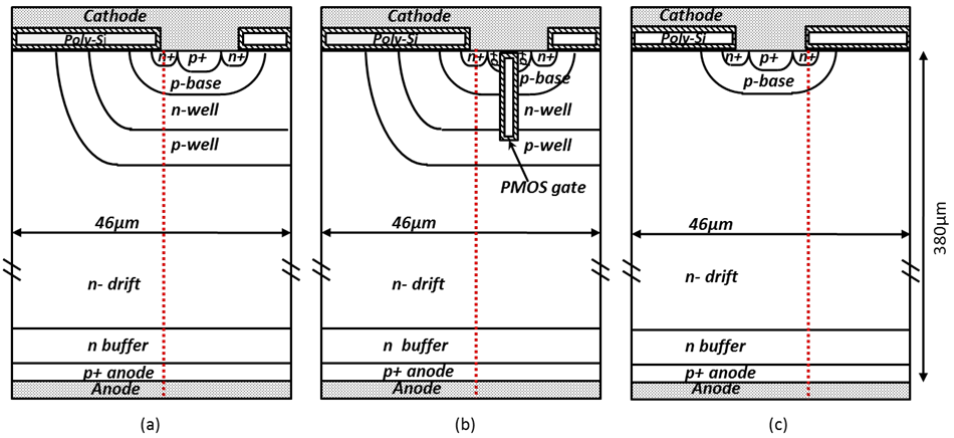


Fig. 1 Schematic Structure diagram of (a) planar gate CIGBT, (b) planar gate CIGBT with deep PMOS trench channel and (c) conventional planar gate IGBT.

2.2. Device turn-off performance

The 3.3kV FS CIGBT and IGBT structures listed in Fig. 1 are simulated to compare their capability to clamp voltage under such extreme condition. The circuit configuration for the inductive turn-off is shown in Fig. 2. These devices are turned-off at V_{DC}=2500V, I_{anode}=150A and T_j=25˚C. A large stray parasitic inductance of L_C=2.4µH is also included in the circuit. It is important to point out that there is no gate resistor used in the circuit. Because conventional technology normally requires large gate resistance to suppress the dynamic avalanche generation, but the turn-off loss increases in this case mainly due to the change of the reduction of dV/dt and longer turn-off time [13]. A further increase in turn-off losses and applying de-rating factor to power devices will cause a significant loss in SOA capability. The reduction of R_g in new technology will provide much lower power losses, shorter delay time during turning-off transient when compared to conventional technology.

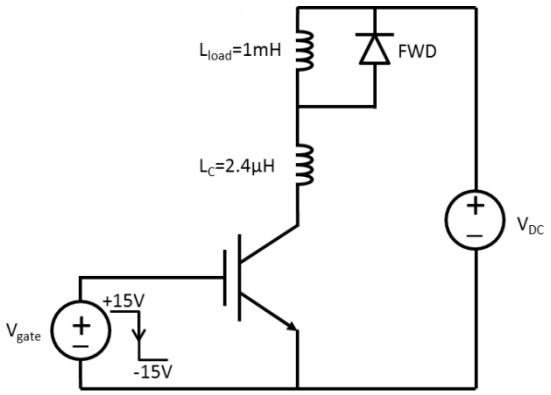


Fig. 2 Circuit setup of inductive load turn-off simulation.

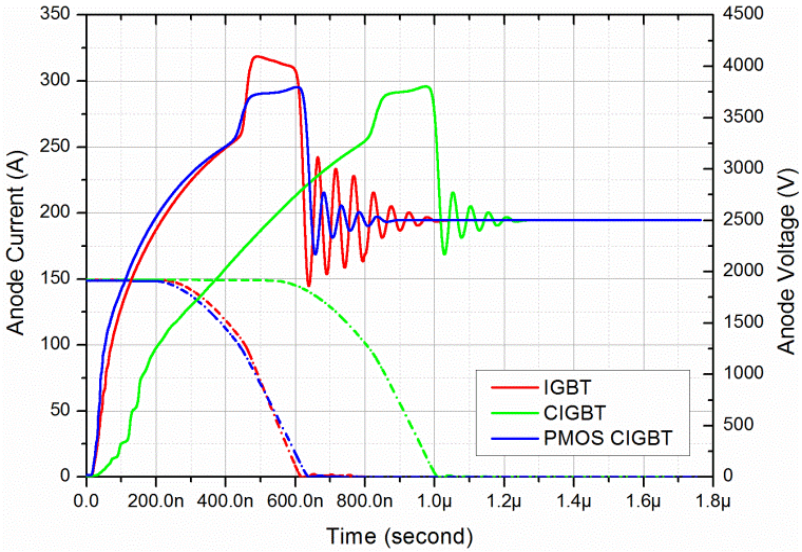
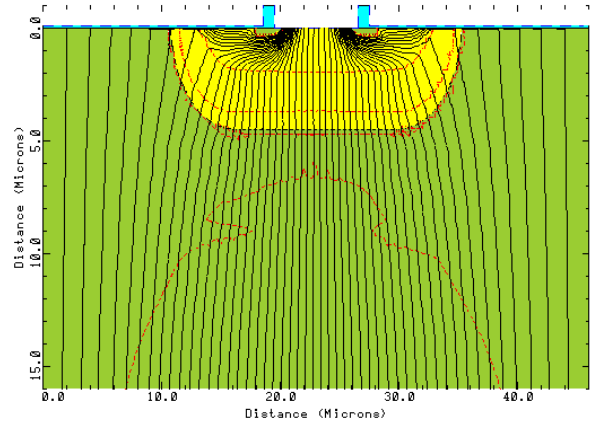


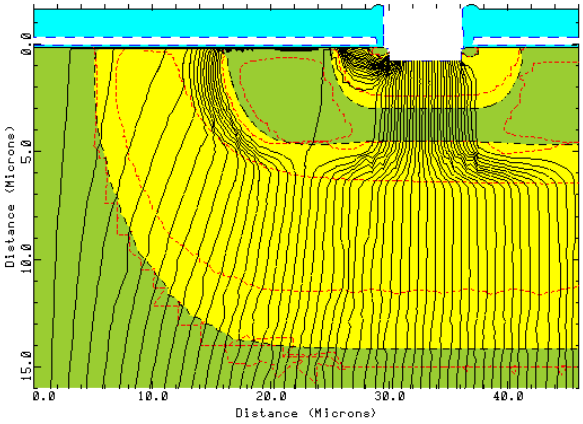
Fig. 3 IGBT and CIGBT turn-off waveforms (V_{DC}=2500V, I_a=150A, T_j=25˚C, solid line: anode voltage; dashed line: anode current).

Fig. 3 shows the turn-off waveform of planar gate CIGBT, PMOS trench gate CIGBT and conventional IGBT. The maximum voltage peak across the IGBT during the transient is about 400V higher than the other CIGBT devices and associated with strong voltage oscillation. The planar gate CIGBT has a slow dV/dt in comparison to IGBT device. This is because CIGBT has several times higher conductivity modulation of the N-drift region due to thyristor conduction [10]. It takes longer time to remove excess carriers from its N-drift region. On the other hand, the low dV/dt helps to maintain current and voltage levels within the SOA, ease the high power stress across the device and less voltage peak and oscillation are found. PMOS trench gate CIGBT is the best performed device by displaying both fast turn-off time and low voltage peak in contrast to the other two structures.

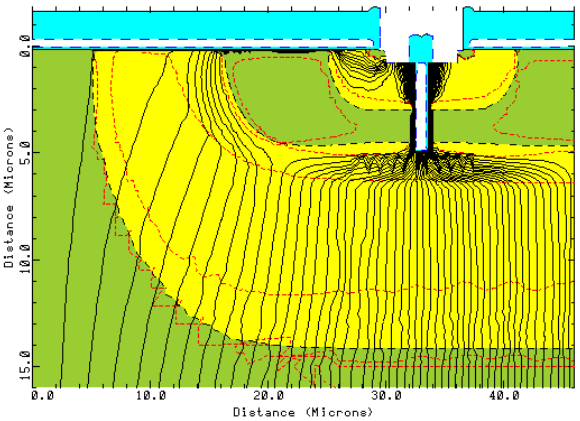
The current flow lines of planar gate IGBT, planar gate CIGBT and PMOS trench gate CIGBT at 200ns after the gate turn-off, when the MOS channel of these devices has cut-off and enters dynamic avalanche in the N-drift region, are shown in Fig. 4 (a)-(c), respectively. The CIGBT devices behave differently to that of IGBT due to its current is carried by a controlled thyristor. The holes within the P-well region flow through the depleted N-well at the saturated hole velocity and are collected at the cathode contact. It should be noted that the N-well is completely depleted when the anode voltage exceeds the self-clamping value of the N-well. Avalanche-generated electron and hole carriers can also be found by the laterally displayed current flow lines. With PMOS trench gate, it conducts during turn-off period when the gate voltage goes negative. It extracts the holes vertically by the trench gate channels and enhanced the capability of CIGBT to remove charges underneath the cathode region. Lower current density can thus be achieved.



(a)



(b)



(c)

Fig. 4 Current flow lines of (a) IGBT, (b) CIGBT, and (c) PMOS trench gate CIGBT structure at time=200ns.

After the turn-off of the gate voltage, the DC voltage is then supported within the structure by the formation of the depletion region. Depending on the concentration of the excess carriers in the depletion region, the width of the depletion region expands with time allowing the device to support larger anode voltage. The electric field profiles in the N-drift region during turn-off period are plotted in Fig 5. The electric field expands towards anode contact to support higher voltages and eventually punches through to the N-buffer region at their maximum clamped voltage. It should be noted that the different positions of electric field peaks at the cathode side are due to the forward blocking voltage is support by the P-base/N-drift junction for IGBT whereas it is supported by the P-well/N-drift junction for CIGBT devices.

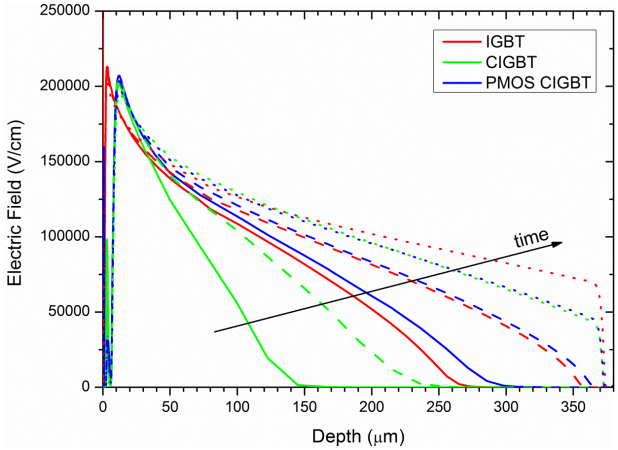


Fig. 5 Simulated electric fields distribution of structures after gate turn-off (solid line: time=200ns, dash line: time=400ns, and dotted line: time at maximum anode voltage).

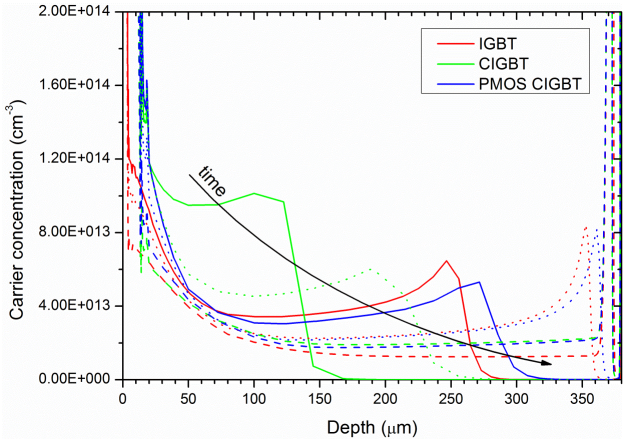


Fig. 6 Simulated effective carrier concentration of structures based on the results shown in Fig. 5 (solid line: time=200ns, dotted line: time=400ns, and dash line: time at maximum anode voltage).

The electric field of planar gate CIGBT expands at a slower rate in comparison to the other two devices. This could be explained by the N_{eff} concentration across the structures as shown in Fig 6. Planar gate CIGBT has a significant high portion of carriers are concentrated at the cathode side than the other two structures. In the process of time, N_{eff} is moving towards anode contact and becomes more evenly distributed across the whole region. It is important to notice that the with the help of PMOS trench gate, the number of hole carriers at the cathode side has greatly reduced in comparisons to the conventional CIGBT. This technology provides an efficient way to remove excess carriers.

3. Optimization of Current Gain of FS-CIGBT

The self-clamping of the over-shoot voltage can be achieved by optimization of N-buffer layer in FS technology. This results larger SOA required for high voltage devices. Like short circuit condition, the self-clamped voltage is influenced by the internal PNP current gain, β_{pnp}, which is a function of anode emitter efficiency, γ_{anode}, base transport factor, α_T and also the effective N-buffer thickness, W_{eff}, as stated in the e.q.(2).

$$\beta_{pnp} = \frac{\gamma_{anode}\alpha_T}{1-\gamma_{anode}\alpha_T} \cong \frac{\gamma_{anode}}{\cosh(W_{eff}/L_p)} \quad (2)$$

where, L_p is the hole diffusion length. It depends on the carrier mobility, lifetime and temperature. It thus requires optimum parameters of β_{pnp} for the FS CIGBT to enable the device to withstand over-shoot voltage successfully.

The 3.3kV planar gate FS CIGBT is simulated under the same circuit configuration in the section A to determine the influence of PNP current gain on the dynamic clamping performance of CIGBT with different N-buffer thicknesses, and anode peak doping concentrations. Fig. 7 shows the turn-off waveforms with N-buffer thicknesses varying from 5μm to 30μm with the same peak concentration of $5.0\times10^{15}cm^{-3}$. It can be observed that the dV/dt of anode voltage after MOS channel turn-off is greatly influenced by the N-buffer thickness. It also leads to reduction of over-shoot voltage as the N-buffer thickness reduces. But this sacrifices the current fall time during the transient.

In comparison, the turning-off waveforms of the structure with varying anode peak concentration with a constant N-buffer thickness (15μm) and doping concentration ($5.0\times10^{15}cm^{-3}$) are demonstrated in Fig. 8. As expected from the increase in current gained by increasing peak anode doping concentration, a reduced self-clamped voltage is achieved at the expense of turn-off loss.

Fig. 9 has illustrated the peak power density during turning-off transient with a function of N-buffer thickness and anode peak doping concentration. The peak power density decreases with decreasing N-buffer thickness. The same trend can be found for IGBT plotted in comparison. As a thinner buffer enhances the number of holes injected into the N-drift region during the transient, the peak power density reduced. But the reduction is less significant when the N-buffer thickness is less than 15μm. Other constraints, such as stray inductance and carrier mobility, limit further improvement in the peak power density when there are sufficient holes to maintain a normal electric field distribution in the N-drift region. In the case of the IGBT, its peak power density is higher for the same N-buffer thickness due to a higher electric field peak across the N-drift region than that exhibited by the CIGBT as explained in the previous section.

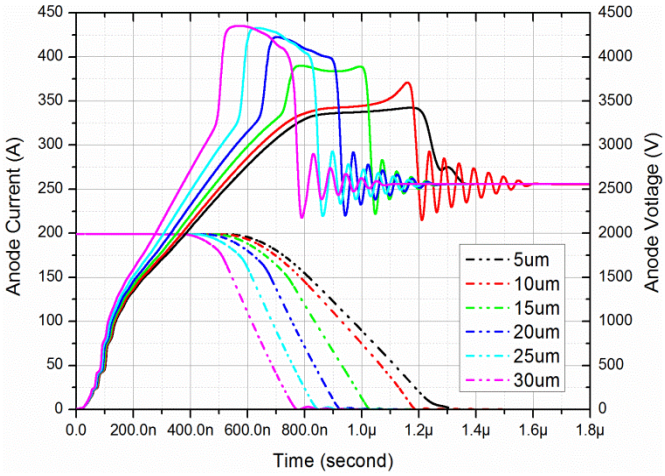


Fig. 7 CIGBT turn-off waveforms with variable N-buffer thickness from 5μm to 30μm (VDC=2500V, Ia=200A, Tj=25˚C, Rg=0Ω).

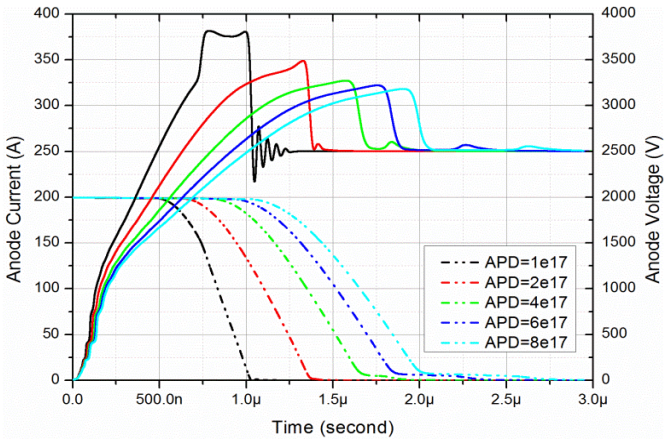


Fig. 8 CIGBT turn-off waveforms with variable anode peak concentration (V_{DC}=2500V, I_a=200A, T_j=25˚C, R_g=0Ω).

For a constant N-buffer thickness of 15μm, the peak power density of CIGBT with increasing peak anode doping concentration is also plotted in the same figure. With a higher anode peak concentration, it also increases the PNP current gain. But the peak power density only shows a slight reduction when compared to the variation of N-buffer thickness. Because as e.q. (2) suggested, N-buffer thickness causes β_{pnp} change exponentially whereas γ_{anode} changes linearly with the current gain.

A trade-off relationship between turn-off power loss and maximum self-clamped voltage is plotted in Fig. 10 with N-buffer thicknesses from 5μm to 30μm. By controlling the N-buffer thickness, trade-off between voltage clamping capability and turn-off loss can be optimized. As can be concluded from the above results, the 3.3kV FS CIGBT device exhibits good voltage clamping capability and turn-off loss.

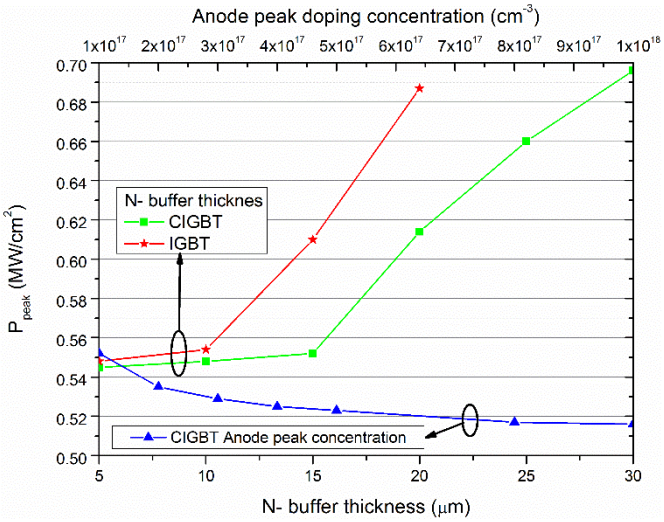


Fig. 9 Peak power density during turn-off.

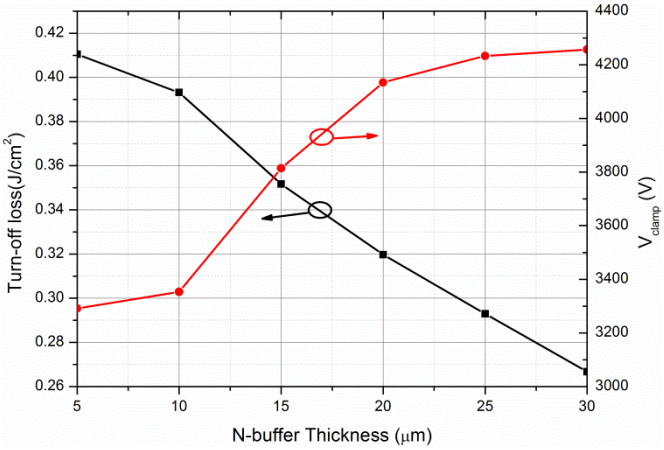


Fig. 10 Turn-off loss and clamped voltage dependence on the N-buffer thickness.

4. CONCLUSION

This paper has shown the dynamic voltage clamping capability of planar gate CIGBT, PMOS trench gate CIGBT and conventional IGBT under extreme stray inductance and zero gate resistance. The removal of excess charges stored in the N-drift region determines the turn-off time and maximum clamped voltage. PMOS trench gate provides a more efficient method to extract the hole carriers by the induced p-channel when the gate voltage goes to negative value. It has exhibited low losses, fast turn-off time and smooth switching waveforms among the three types of structures simulated.

The self-voltage clamping feature of CIGBT can be further improved through structural optimization of internal PNP current gain. A high current gain has better over-voltage protection, but would increase the turn-off power loss. A low current gain should also be avoided as it shifts the peak electrical field from cathode to anode side and induces oscillation during the process. The simulation analysis has shown that greater optimization of the performance of FS devices is achieved through the freedom provided by the N-buffer than by NPT technology. There is a considerable impact on SOA capability and power losses to FS CIGBT. The new protection feature of FS CIGBT can simplify the system design and offer greater optimization of performance of high voltage devices.

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