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REALIZATION OF KINK EFFECT IN THE DRAIN CHARACTERISTICS OF III-NITRIDE/B-GA2O3 NANO-HEMT DUE TO TRAPS AND SELF-HEATING

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Abstract. *In this research article, a field-plated and recessed gate III-nitride Nao-HEMT grown on β-Ga2O3 substrate is designed. The electrical characteristics of the proposed HEMT is investigated by using the thermal models of ATLAS TCAD simulations. The investigation focuses on the impact of traps and thermal influence that cause the Kink effect in DC characteristics of III-Nitride/β-Ga2O3 HEMT. A noticeable kink effect is observed in proposed III-Nitride/β-Ga2O3 HEMT. This phenomenon is typified by an abrupt rise in drain current at high gate voltages, which causes the device to behave non-linearly. The kink effect is most likely caused by traps in a barrier layer activating. A field-plate, gate length, and gate recessed depth of 20-nm each is considered for the analysis. Furthermore, self-heating effect in drain current characteristics are investigated with temperature changes. The findings demonstrated that scattering processes that emerge when temperature increases above a particular amount cause both the mobility and the carrier concentration of 2DEG to decrease. Consequently, the output current performance degrades as a result of the self-heating effect becoming more noticeable. In addition, the drain lag phenomenon is investigated in connection with the drain current's transient behavior. The duration of the channel's formation and ability to permit current flow between the drain and source terminals is the reason for this drain lag phenomenon. It is hypothesized that the device's channel length, trapping and de-trapping, and thermal influence are some of the factors that affect the drain lag. Finally, the implications with this drain lag phenomenon are investigated.*

Key words: *III-Nitride, β-Ga2O3, HEMT, Kink effect, Self-heating, Scattering, Drain Lag, TCAD*

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1. INTRODUCTION

HEMT devices, also known as High Electron Mobility Transistors, offer unique advantages in terms of high-speed operation and low noise characteristics. These transistors have gained significant attention in research and development due to their ability to provide valuable insights into the underlying physics of electronic devices [1]–[3]. Furthermore, HEMT devices playing a crucial role in advancing the performance of various electrical devices, such as amplifiers and oscillators, while also facilitating the advancement of simulators used for further technological advancements. HEMT devices are immensely beneficial for high-frequency and high-power based applications due to their excellent mobility and exceptional saturation velocity. Massive strides have been made in last few years in the research and development of GaN (gallium nitride) and its family of allied material for optoelectronics, communication, biomedical, and space applications, and it is prominently recognized that III-Nitride HEMTs have gained an enviable reputation in each of these fields [4], [5].

However, in order to achieve better mobility and reduced resistance, an AlN layer has been recently proposed as a spacer between the buffer and barrier [6], [7]. AlN utilizes the intriguing material characteristics of III-nitrides, including a substantial breakdown electric field, large band gap, and superior thermal properties [8]. The performance of AlGaN/AlN/GaN HEMTs can be enhanced by all of these material characteristics. AlGaN/AlN/GaN HEMTs arguably have a higher sheet carrier density than traditional AlGaN/GaN based HEMTs, making it possible with the use of an AlN spacer while maintaining an improved charge carrier density at hetero-junction [9].

In recent years, The III-nitride-HEMTs developed β-Ga_2O_3 substrate outperform traditional GaN based HEMTs and provide a contender to commercially available GaN technologies, promoting the development of faster, more compact devices with exceptional performance [10]. However, it is observed that some adverse outcomes, notably short channel, and hot electron effects, emerged with the decreasing of architectural device dimensions, especially the reduction of its gate size, and these outcomes are unavoidable [11], [12]. At that point, it becomes crucial to identify the optimal method to improve speed while simultaneously lowering device power consumption. However, improving the intrinsic transconductance with the most effective electrostatic regulation is crucial for ultra-scaled devices, in addition to keeping the parasitic current as minimal as possible that can potentially be realized in triangular quantum shaped well AlGaN/AlN/GaN/ architectures.

Thus, it is imperative to examine the performance characteristics over temperature and trap issues before utilizing III-Nitride/β-Ga_2O_3 Nano-HEMT for commercial applications. The performance of HEMTs is heavily reliant on the transport properties of 2DEG (Two Dimensional Electron Gas); and temperature stability to be crucial, especially at higher temperatures where ohmic and Schottky contacts degrade [13]. The present research work investigates the impact of thermal and traps influence on a different performance characteristics of proposed III-nitride HEMT.

The following are some examples of experimental research on the impact of traps on AlGaN/GaN HEMTs performance characteristics. Numerous methods have been used to examine the trapping seen in GaN HEMTs, and the findings indicate the presence of prominent trap centres inside the epitaxial layers [14]. The temperature-dependent transient study revealed deep traps in the band gap that exhibited drain lag. In [15] demonstrated that, a major cause of the kink effect is the de-trapping of charge carriers. The cause of kink is because carriers that were previously de-trapped at one electric field will receive additional

energy from temperature to de-trap at a different electric field. Numerous factors, including device size, ambient temperature, and semiconductor technology, and bias point, can alter operating conditions and result in the kink effect [16]–[19].

The main contribution in this piece of research work presents here a preliminary study of III-nitride/β-Ga_2O_3 Nano-HEMT, and it discusses the occurrence of kink-effect due to the influence of thermal and traps. Furthermore it discusses the effect of temperature and traps on different performance characteristics, and degradation in performance of HEMT due to self-heating issues. Finally, the implications caused due to drain lag are also discussed.

2. Device Structure and Simulation Framework

Figure 1 illustrates the structure and epitaxy details of investigated III-Nitride HEMT on β-Ga_2O_3 substrate material. The HEMT structure comprises of 24 nm GaN buffer, a 1nm AlN spacer, a 32 nm AlGaN barrier, and a 135 nm β-Ga_2O_3 substrate. At the Si_3N_4/AlGaN interface, donor type traps of 1×10^{12} cm^{-2} have been set at an energy level 0.2 eV beneath the conduction band. Donor type of traps are employed to simulate surface imperfections when passivation layers are being deposited; and acceptor type of traps in GaN buffer are used at a concentration of 4.5×10^{16} cm^{-3}. It is taken into consideration due to dislocations or real-time existing flaws in the GaN buffer.

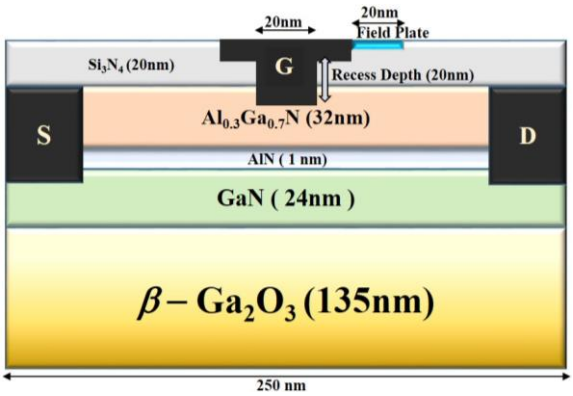

Fig. 1 Structure and epitaxy details of investigated III-Nitride HEMT on β-Ga2O3 substrate.

In the present investigation, simulation modeling of the considered HEMT is performed using ATLAS Silvaco TCAD [20]. The ATLAS dealt with device designing and subprogram calls, and the sub-modules of BLAZE, GIGA, and ATLAS carry out specific tasks essential to thermal modeling, advanced materials, and heterojunctions. In order to appropriately model III-V semiconductors and adapt computations involving energy bands at the heterostructure, ATLAS typically makes use of the BLAZE program extension. In order to determine current densities, recombination-production, and velocity saturation, the hetero-junctions must be changed. The hydrodynamic with a balanced energy carrier transportation approach is employed to attain the highest level of reliability and computational effectiveness.

However, to accomplish the desired simulations and make accurate predictions about characteristics of proposed HEMT, certain physical frameworks need to be included in

simulation when using TCAD simulation tool. These models address the carrier behavior, including trap impact and lattice temperature. Furthermore, simulation framework must consider self-heating effects into account due to the high operating voltages.

As previously stated, the hydrodynamic transport hypothesis, a physical simulation framework, can yield accurate simulation results [20]. Given that the temperature of the device varies, Giga ought to be utilized to mimic the heat transfer within the device. The avalanche trend and the gate/source diode's conduction current severely restrict the functionality of power field effect transistors. In this investigation, the "Selberherr" impact ionization approach is utilized to examine KINK effects [21], [22]. In [23], it is expanded the simulated range of temperatures to 400 K and designed an efficient model that accounts for how ionization is impacted by charge carrier's mobility.

The impact ionization-induced generation framework is required to be activated to mimic avalanche breakdown. This is accomplished by enabling the "Selberherr" impact approach by using impact "Selb" expression. Here, in addition to thermal production offered by recombination SRH, a beam expression is employed to define optical source of charge carrier pair origination. This investigation has considered fluctuations in lattice temperature and relied on the framework showed in [24], which incorporates all thermal sources and sinks. Finally, suitable boundary conditions must be specified for thermal simulation to be effective.

3. Results and Discussion

This Section provides a neat delineation to analyse the kink effect in the performance characteristics of proposed III-nitride/β-Ga_2O_3 Nano-HEMT with regards to the influence of traps and self-heating effects.

3.1. Kink Effect

The Drain characteristics of the proposed HEMT for different V_{GS} values at room temperature are illustrated in Fig. 2. It is explicitly observed that proposed III-nitride/ β-

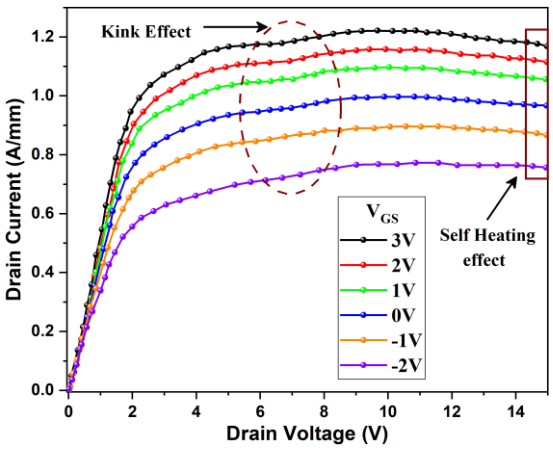

Fig. 2 The kink effect in an III-Nitride/β-Ga_2O_3 HEMT at room temperature, where V_{GS} varies with a step of 1 V from -2 V to 3 V.

Ga_2O_3 HEMT exhibits a discernible kink effect. The HEMT demonstrates a distinct kink effect (KE) that has a strong gate voltage-dependent locus of the kink effect [16], [25].

For different V_{GS} voltages, it can be observed that an increase after diminution with a sudden surge in drain current in a HEMT device signifies the presence of traps in device [26]–[28]. Thereby, the traps that become activated in a barrier layer are most likely responsible for kink effect, resulting in an abrupt rise in an output drain current at a specific voltage that enhances the output conductance. Hence, when the device is operating at a specific voltage, the trapping phenomenon that is directly impacted by conduction of current, thermal influence, and electric field, is a possible factor that causes the kink effect [28].

Additionally, the KINK effect amplifies the unwanted noise in the low frequency portion. This phenomenon occurs because de-trapping causes changes in the charge carrier mobility, leading to variations in the conductivity [29]. As a result, the noise generated at lower frequencies is expected to increase due to these fluctuations in conductivity. The output conductance's abrupt increase (g_{ds}) as an outcome of kink and traps is shown in Fig. 3. This phenomenon has been usually associated with a impact ionization, which causes the development of holes that regulate surface potentials or the channel/substrate junction [30], [31].

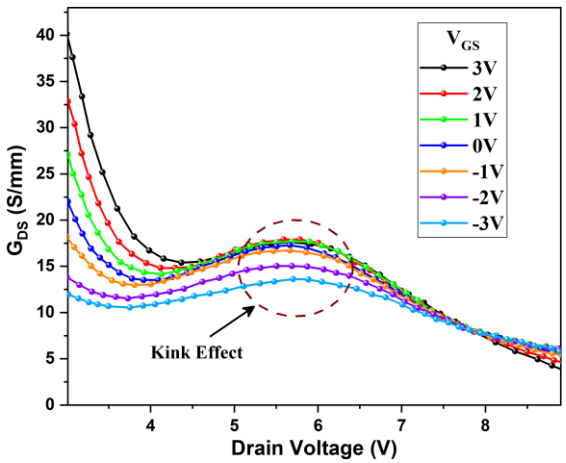

Fig. 3. Illustration of abrupt increase in output conductance (g_{ds}) as an outcome of kink and traps effect.

V_{KINK}, a critical drain voltage where the output conductance reaches its maximum, is addressed by surface imperfections in the buffer layer. VKINK becomes higher as gate voltage increases, indicating that a de-trapping process is field-assisted and directly associated with gate voltage (V_G), or an electric field. It is hypothesized that this kink is possibly a result of hot electron trapping and field-assisted de-trapping by means of donor type of traps in a GaN buffer layer.

As illustrated in Figs. 3 and 4, the kink effect is characterized by a sudden spike in conductance (output) g_{ds} in the saturation regime, and transconductance gm is compressing, both impair the functionality of the device.

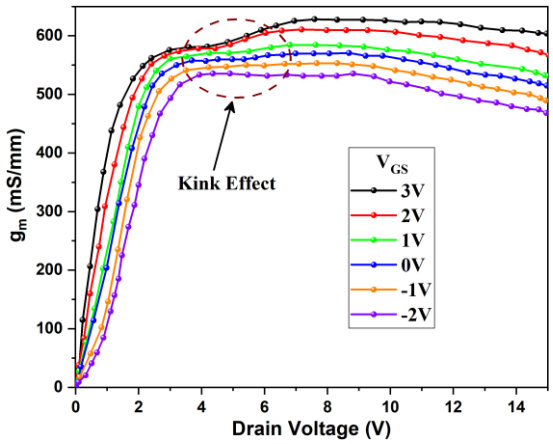

Fig. 4. The transconductance (g_m) emerged to be compressed as an outcome of kink and traps.

3.2. Self-Heating Effect

As stated earlier, the proposed HEMT is expected to operate at a high operating voltage; therefore the self-heating effects must be taken into account. The self-heating effect is associated with factors such as the semiconductor's surface trapping and the amount of thickness of the passivation layer expanding. Furthermore, the hot spot temperature is significantly impacted by the kind of passivation material [32]. Particularly at high voltages, surface trapped charge control can be greatly impacted by tunneling and leakage current processes [33], [34]. As illustrated in Figs. 5 and 6, it is evident that the drain current decreases at higher drain voltages of various gate voltages. The electric field accelerates the flow of electrons through the channel. Light emissions can result from this type of avalanche, where the gate electrode gathers holes and drain electrode gathers electrons.

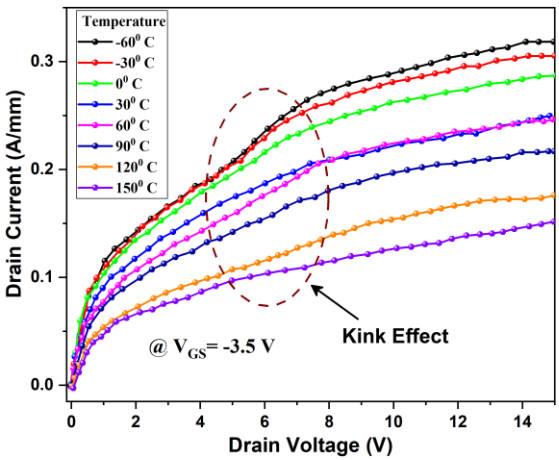

Fig. 5 Kink effect in drain characteristics of the HEMT at different temperature values of @ V_{GS}=-3.5V.

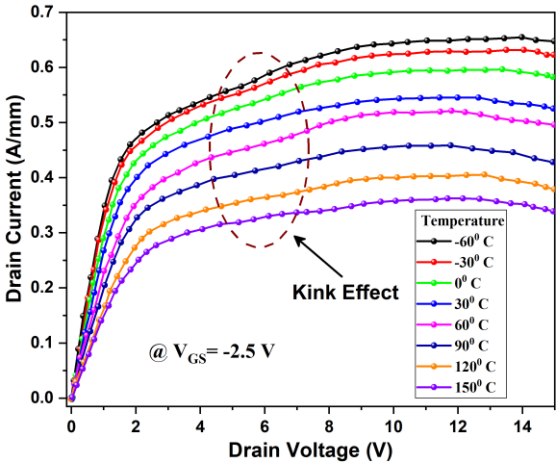

Fig. 6. Kink effect in drain characteristics of the HEMT at different temperature values of @ V_{GS}=-2.5V.

Electron mobility increases at low temperatures due to a reduction in polar optical phonon dispersion. The traps beneath the gate, particularly on drain area side, experience self-heating effects as a result of Joule electric power dissipation. Self-heating effects cause a decline in carrier mobility, an increase in threshold voltage, and a drop in conductance for both large drain and gate voltage. These effects can be particularly significant in high-power devices and can limit their overall performance. Additionally, self-heating can also result in increased power dissipation and device degradation over time, further impacting the reliability and longevity of device. Furthermore, Self-heating effects have an impact on the device's gain, which in turn has an impact on its effectiveness and power usage.

3.3. Drain Lag

The transient drain current that occurs when a drain voltage pulses from OFF state (V_{DS} = 0 V) to ON state (V_{DS} > 0 V) for a constant gate voltage is referred to as "drain lag" [35]–[38]. There is a subsequent drop in the current I_{DS} if this pulse continues for long enough. The factor influencing the traps' occupancy rates is a V_{DS} voltage.

Figure 7 shows a transient behavior of output drain current, pointing to an existence of the drain lag occurrence. As described in [39], electron injection into a buffer layer, where the charge carriers are trapped, results in GaN transistors' output current decreasing when a pulse voltage is applied at the drain.

As soon as the drain voltage moves from an off-state to on-state, or when there is a positive change in V_{DS}, electrons are accelerated by an electric field that V_{DS} creates and are trapped in a deep localized energy states in a substrate or buffer, and this happens as long as the pulse width is longer than a capture time constant and shorter than a emission time constant.

These electrons that have been trapped are not involved in the channel current as they are confined within the traps and cannot move freely. Instead, they remain localized and do not contribute to the flow of electric charge through the current-carrying path. When the traps become full, the direct result is a decrease in drain current until it attains its steady state.

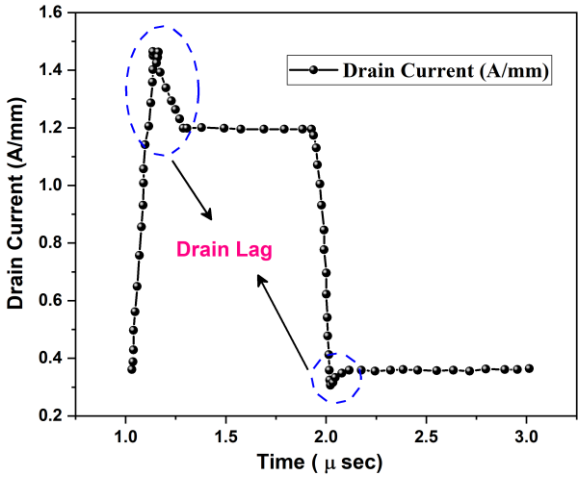

Fig. 7. Illustration of Drain Lag in output characteristics of the HEMT at different temperature values.

Here is an approach to express the drain lag (Eq. 1) [37]:

$$D_{Lag} = \frac{I_{Dss} - I_{Dss0}}{I_{Dss}} \cdot 100 \tag{1}$$

where I_{DSS0} represents the highest possible drain current at equilibrium and I_{DSS} represents the highest drain current. The low drain lag percentage indicates that the device quickly stabilizes and maintains a consistent performance, ensuring reliable operation. A satisfactory outcome is demonstrated by the proposed HEMT, which showed a drain lag of 3.12 %. It indicates that the proposed HEMT quickly and effectively reaches its steady state.

3.4. Limitations

There are two categories of GaN HEMT limitations [3]:

1) Technological, including temperature, chemical, and barrier scaling; and

2) Intrinsic related to current deteriorate, trapping effects and self-heating of the device

Trapping effects in AlGaN/GaN HEMTs during operation are one of the main factors affecting performance loss, creating current dispersion between DC to RF or otherwise, DC to pulsed I_D-V_D characteristics

1. A gate electron is injected onto the surface together with barrier traps under a high negative V_{GS}.
2. The barrier/buffer traps are injected by hot electrons under a high on-state V_{DS}.
3. The electrons that the deep layers capture are induced during material growth.

Therefore traps and temperature have a significant impact on the device's performance characteristics. This drain lag phenomenon arises from variations in the conductivity resulting from changes in the charge carrier mobility caused by de-trapping. These variations in conductivity are therefore anticipated to cause an increase in the noise produced at lower frequencies.

4. CONCLUSION

In a summary, the effect of traps and temperature which are the major issues for reliability at device level is discussed here. This work effectively investigates the origin of the kink effect associated with the traps and temperature analysis of the proposed field-plated recessed gate III-Nitride HEMT grown on β-Ga_2O_3 substrate towards various performance characteristics. It is observed that when the temperature rises, the drain current decreases, further impairing the device's performance. This phenomenon arises because of the decrement in electron mobility due to the increased scattering of electrons caused by the higher electric field. Further, the drain lag indicates that the decline in I_{DS} is due to the accumulation of charge carriers in channel region, resulting in a temporary reduction of current flow. It can be refer to as trapping-induced collapse of drain current. A reduction in the transistor's output current results from the buffer layer's trapped electrons causing a barrier that prevents current flow. All of these factors are recognized to be major concerns for ensuring the reliability and proper functioning of electronic devices. As an outcome, this research can offer insightful suggestions for reducing the detrimental effects of traps and temperature on device performance. Furthermore, by comprehending these effects, III-Nitride HEMT design can be made more reliable and efficient.

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