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EXPLORING SUPPLY VOLTAGE AND TEMPERATURE VARIATION ON XOR-XNOR CELLS WITH CONVENTIONAL / NON-CONVENTIONAL TECHNIQUES

Uma Sharma[1,2], Mansi Jhamb[2]

[1]Ajay Kumar Garg Engineering College, Ghaziabad, India
[2]University School of Information Communication and Technology, GGSIPU, New Delhi, India

ORCID iDs:	Uma Sharma	https://orcid.org/0000-0001-6156-0552
	Mansi Jhamb	https://orcid.org/0000-0002-7975-8505

Abstract. *This paper delves into a comprehensive exploration of conventional and unconventional design approaches applied in XOR-XNOR cells. These cells play a crucial role in various arithmetic logic circuits with substantial computational capacity within VLSI designs operating at low voltage and power levels. The paper investigates the difficulties linked with both conventional and non-conventional design strategies. Furthermore, it performs a relative evaluation of different XOR/XNOR cells documented in current literature concerning circuit design parameters. The results of this investigation indicate that the adoption of carbon nanotube field-effect transistor (CNTFET) technology in lower technology nodes significantly decrease circuit delay, while floating gate metal-oxide semiconductor (FGMOS) technology displays superior interpretation in terms of circuit power efficiency. The discussion also covers the utilization of FinFET technology in the creation of XOR/XNOR cells. This paper conducts an assessment of the voltage and temperature resilience of these XOR/XNOR cells. The analysis has been undertaken utilizing the HSPICE tool at 22nm technology node. The XOR/XNOR cell based on FGMOS demonstrates the highest resilience to voltage and temperature fluctuations. The major challenges encountered in the adoption of non-conventional technologies involve the lack of appropriate simulation models and the intricate fabrication processes. These challenges notably hinder the progress and adoption of these pioneering methodologies.*

Key words: *Supply voltage resilience, temperature resilience, CNTFET, XOR/XNOR implementation, static CMOS and domino logic style, FinFET and FGMOS*

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Corresponding author: Uma Sharma
Ajay Kumar Garg Engineering College, Ghaziabad, India.
E-mail: uma.banasthali@gmail.com

1. INTRODUCTION

The rapid proliferation of user-friendly, portable electronic devices in the electronics industry has elevated the importance of low-power applications in VLSI system design. This surge in electrical and electronic device usage has incentivized designers to focus on reducing silicon footprint, enhancing computational speed, minimizing power consumption, and bolstering resilience [1].In the present day, portable electronic devices like cell phones, tablets, laptops, and notebooks have become an essential aspect of our lives. To optimize the performance of these electronic systems, designers are working towards creating circuits that are small in size, high in speed, and energy-efficient.
XOR/XNOR cells find extensive application in various communication uses, serving as a sequence generator, parity checker, correlation and sequence detector, parity generator, as well as inmodulator and demodulator in (Phase lock loop)PLL [2-4]. With the rising demand for handheld devices like mobile phones, tablets, and notebooks, there's an increasing need for low-voltage, low-power solutions. This demand significantly influences the digital integrated circuit (DIC) design landscape, where XOR/XNOR cells stand out due to their unique and valuable characteristics [5].The literature presents numerous circuit design methodologies for the digital circuit designs [1-7], with complementary metal oxide semiconductor (CMOS) technology being the most prevalent for (Low Voltage Low Power) LVLP operations due to its lower threshold voltage and technology node. As CMOS technology has scaled, Si-MOS devices gate length has reached the nanoscale, pushing MOSFETs into the deep sub-nanometer regime. However, downsizing devices beyond a certain point poses significant obstacles and concerns in CMOS circuit design, including increased short channel effects, amplified transistor parameter variability, and reliability issues [8].

Consequently, advanced technologies like FinFET, and CNTFET have been explored. Among these CNFETs (carbon nanotube field-effect transistor) stand out as the most welcomed technology for (Ultra Large Scale Integration) ULSI design due to their enhanced scalability compared to standard MOS technology [9]. This characteristic makes it a promising alternative to replace MOS technology in ULSI circuit design. Additionally, floating gate MOS technology has been reported as nonconventional method in the literature [8-14] as alternative solution.

Building upon the groundwork laid in the prior publication titled "Design-Space Exploration of Conventional/Non-Conventional Techniques for XOR-XNOR Cell" [9], this paper further addresses the challenges inherent in non-conventional methodologies, as discussed in the referenced research article [9]. The primary focus of this current research article is to perform an analysis of voltage and temperature resilience specific to the XOR/XNOR cell designs previously scrutinized in the same referenced research paper [9].

Section II presents an overview of technologies employed for implementing XOR-XNOR cells. Section III focuses on the optimal selection of XOR/XNOR cell designs for low voltage, low power applications. Section IV of this paper addresses the analysis of voltage and temperature variations for both conventional and non-conventional XOR/XNOR cell designs. Finally, Section V delivers the conclusion derived from the comparative analysis.

2. Exploring Techniques for XOR-XNOR Cell Implementation: A Comprehensive Survey of Technological Approaches

Numerous design methodologies for implementing XOR/XNOR cells can be found in the literature [2, 5, 7-8, & 15-22]. In general, there are two main techniques for designing digital circuits: static and dynamic circuit design approaches. Multiple phase cascading is limited by dynamic logic; however, variant called domino logic permits multiple stage cascading [16].When it comes to the implementation of high-speed digital circuits, "dynamic complementary metal-oxide-semiconductor (CMOS) logic performs better than static CMOS logic" because it operates faster and uses less power [23]. CMOS technology is still widely used and preferred in chip design because of its low static power dissipation, which results in low power consumption. This attribute arises due to the absence of a direct connection between the ground terminal and the power supply in the circuit. CMOS devices do not generate superfluous heat, in contrast to other logic circuit methodologies such as transistor-transistor-logic or standard NMOS/PMOS logic, which have a tendency to maintain some residual current even during inactivity. An elevated volume of logic operations on an integrated circuit (IC) is made easier by these unique CMOS features. In the realm of digital circuit design, both static and dynamic technologies find application in literature. This discussion encompasses the implementations of XOR/XNOR using these various technologies.

2.1. Static XOR/XNOR cell

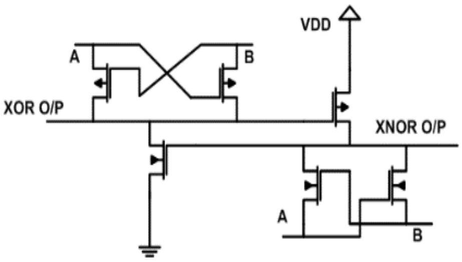
The choice of logic style used in logic gates fundamentally influences the speed, area, energy consumption, and connection complexity of a circuit. Radhakrishnan et al. [23], introduced a novel 6-T XOR/XNOR cell design depicted in Figure 1(a). This design integrates pass transistors (PT) and transmission gates (TG). The development of this XOR/XNOR cell employed Karnaugh map reduction techniques in combination with pass network theorems. This circuit experiences a prolonged worst-case delay when the input is either "11" or "00." In these situations, the outputs take two sequential steps to reach their ultimate voltage levels. Few XOR/XNOR cells have been reported in the literature that can produce both XOR and XNOR outputs simultaneously while maintaining good output levels across all possible input combinations. However, these cells utilize a static inverter in their critical path [24-27].

Goel et al. [3] presented an enhanced circuit for the simultaneous generation of XOR and XNOR outputs intended for application in designing the full adder module I. The newly proposed circuit, illustrated in Fig. 1(c), adopts a CPL (complementary pass transistor logic) style configuration. This configuration removed the static NOT gate from the critical path of XOR/XNOR outputs; nevertheless, the circuit's delay persists at a higher level, primarily due to the cross-coupled structure.

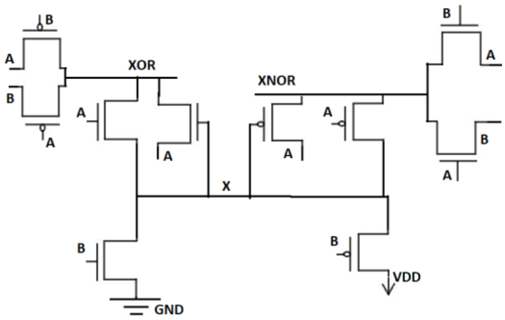
Further, this issue is resolved by Naseri and Timarchi [5] who presented the XOR/XNOR gate using 12 transistors. This design shown in Fig.1(e)also omits the requirement of static NOT gates along the circuit's critical path. Consequently, it exhibits reduced delay and enhanced driving capability compared to designs employing CMOS inverters to generate the XNOR output. Nevertheless, an external inverter is necessary for this circuit to generate the complement of the input (A). To enhance the performance of the circuit, it is possible to achieve improvement by removing the need for this external inverter.

Kandpal [2] suggested XORX/NOR circuit relies on a complementary pass-transistor logic (CPL) and cross-coupled structure. This configuration incorporates two pMOS and three nMOS transistors at the XOR output, and conversely, two nMOS and three pMOS at the XNOR output. In the XOR segment, both pMOS are linked in parallel as pass-transistor logic (PTL). Similarly, at the XNOR output, the nMOS transistors are connected in parallel as PTL. This circuit shown in fig.1 (b) enables the simultaneous generation of full-swing XOR–XNOR outputs. Additionally, efforts were made to boost the performance of the XOR-XNOR circuit by independently designing XOR and XNOR components. This design presented in [28] for XOR-XNOR functionality is implemented using CPL logic, incorporating a single static inverter. Shown in Fig.1(d), this circuit enables the independent realization of both XOR and XNOR outputs within the design framework that utilizes CPL logic with a solitary static inverter.

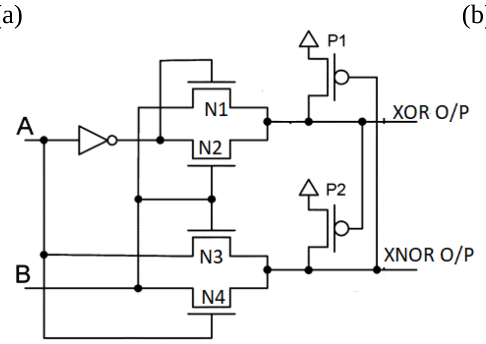
In deep-submicron technologies, the static leakage power escalates owing to short-channel effects. Therefore, it is crucial to formulate circuit designs with low power consumption in deep-submicron technologies. M. Moradi et al. introduce a ground-breaking approach in their work [22], presenting the input-controlled leakage restrainer transistor (ICLRT) technique. This innovative method aims to mitigate both leakage power and short-circuit power, crucial concerns particularly at lower technology nodes. The ICLRT technique is harnessed for designing various logic gates, enabling the attainment of full output voltage swing while consuming considerably less power compared to the existing state-of-the-art designs examined in the article. The design of XOR/XNOR gate with ICLRT technique is shown in Fig. 1 (f).



(a)



(b)



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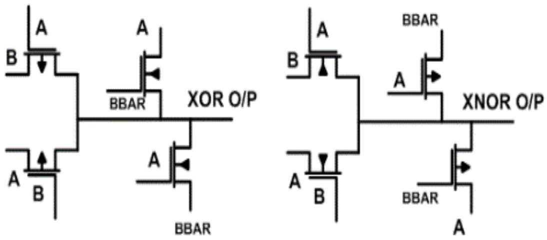
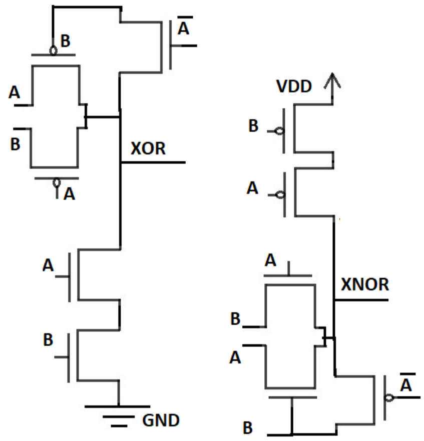
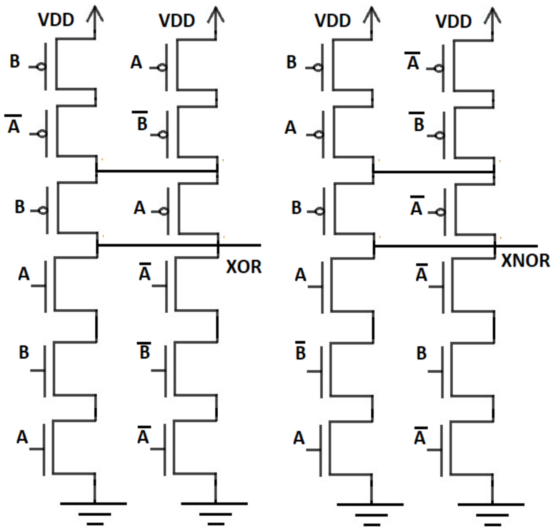


(d)



(e)



(f)

Fig. 1 Static XOR/XNOR cell designs (a)Radhakrishnan[23] (b)Kandpal [2] (c) Goel [3] (d) Kandpal [28] (e) Naseri[5] (f) Moradi [22]

2.2. Dynamic XOR/XNOR cell

The Fig.2 illustrated a fundamental n-type dynamic CMOS logic circuit [29] consists of key components: a precharge transistor (Mp), an evaluation transistor (Me), and an nMOS logic block. The nMOS logic block is dedicated to realizing a Boolean function, and the circuit's effective functioning relies on the presence of a clock signal, essential for the operation of both the precharge and evaluation transistors.

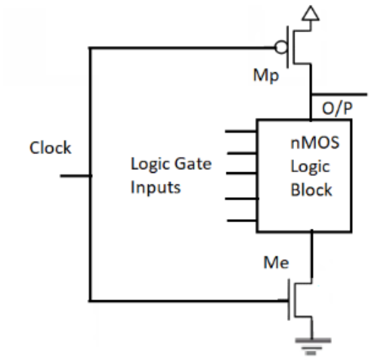
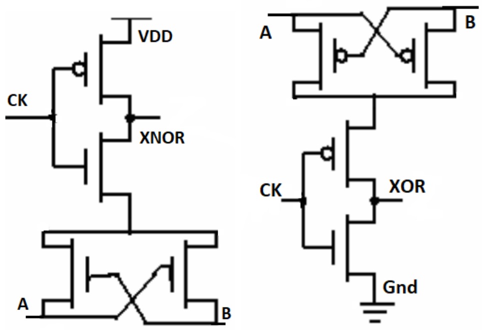


Fig. 2 Structure of dynamic logic [29]

During the precharge phase, when the clock signal is low, Mp becomes active while Me is inactive. This configuration results in the o/p carrying the voltage VDD. In the evaluation phase, when the clock signal is high, Mp deactivates and Me becomes operational. The state of o/p whether it retains the voltage VDD or links to the ground depends on the input conditions within the nMOS logic block.



(a) (b)

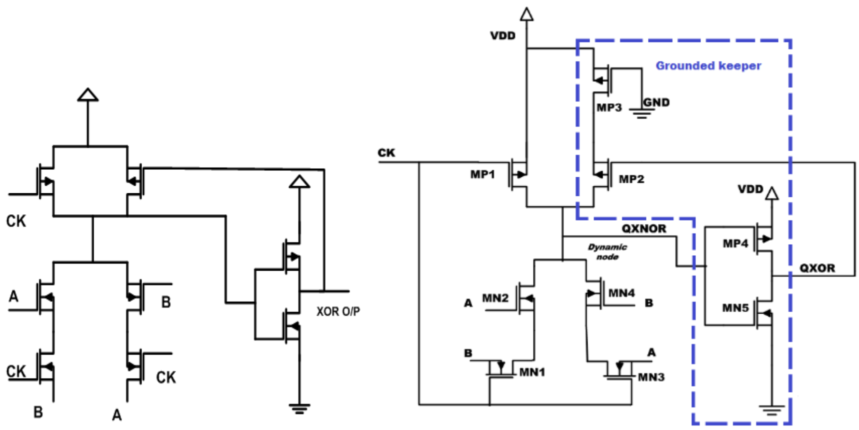
Fig. 3 (a) XNOR using dynamic logic [29] (b) XOR using dynamic logic [29]

In the proposed XOR and XNOR gate design [29], the output node consistently achieves a full voltage swing across all input combinations of A and B. This implementation of dynamic XOR and XNOR gate is shown in fig. 3successfully mitigates the threshold loss problem and offers easy cascading ability within low-power supply circuits.

2.3. Domino XOR/XNOR cell

Chip space utilization is a significant concern in static CMOS design methods. Consequently, dynamic logic styles emerged as an alternative to minimize transistor count, albeit with increased switching power dissipation compared to static designs. Domino logic, which combines dynamic and static logic and provides a viable solution to these issues, is a crucial advancement in the development of electronic circuit technology [7 &16].

In this article [16], a new design for the domino XOR/XNOR cell is introduced and shown in fig. 4(a). This design reconstructs the traditional domino XOR/XNOR cell by combining PTL and CMOS circuits. As a result, it reduces the number of MOSFETs compared to the conventional design, consequently lowering the gate's power consumption and Power-Delay Product (PDP) by 18% and 6% respectively. However, this enhancement leads to a 14% increase in the gate's delay. The design presented in reference [7] integrates dynamic logic and a grounded keeper with an inverted output as shown in fig.4(b). It exhibits a 5.341ps delay, consuming only 0.314µW power, and achieving a power delay product of 1.675aJ. Notably, this design successfully resolves the charge sharing issue commonly associated with dynamic logic styles. Simulated at a nominal VDD of 0.7V using the HSPICE simulator at the 22nm node, this proposed design for the proficient XNOR/XNOR cell demonstrates superior performance.



(a) (b)

Fig. 4 Domino logic XOR/XNOR implementation (a) [16] (b) [7]

Non-conventional design methods and devices have a substantial impact on digital circuit design, especially at lower technology nodes. Within the literature, multiple XOR/XNOR cell designs [8, 16-21, & 30] have been introduced, employing non-conventional approaches rather than the conventional CMOS technology. This discussion encompasses the implementations of XOR/XNOR using these un-conventional technologies.

2.4. FGMOS implementation

The foundation of many digital systems, like arithmetic units and error detection circuits, relies on XOR/XNOR operations. This innovative design integrates FGMOS technology to elevate the performance of these crucial operations. FGMOS devices bring forth enhanced linearity and improved voltage transfer properties, resulting in increased speed and precision when executing XOR/XNOR operations.

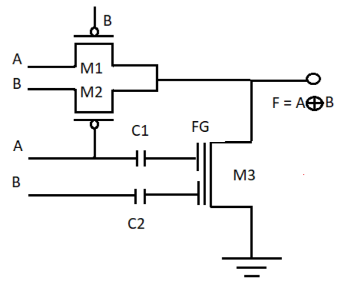


Fig. 5 XOR gate with FGMOS technique [8]

Utilizing FGMOS in the design of XOR gates [8] leads to a decrease in both transistors count and power consumption. The design is comprised of two PMOS transistors utilized in a PTL logic style.

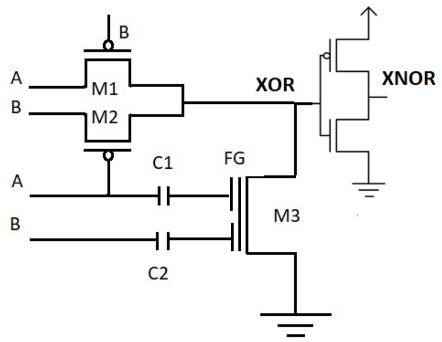


Fig. 6 FGMOS based XOR/XNOR cell

Additionally, one 2-input FGMOS transistor is coupled between the output terminal and ground to ensure a full swing undistorted output. This particular XOR cell design necessitates fewer transistors when compared to the standard CMOS-based implementation. FGMOS based XOR/XNOR cell is depicted in fig.6, which is implemented by adding one static inverter at the output node of XOR cell discussed in [8].

2.5. CNFET implementation

MCML (MOS current-mode Logic) has emerged as a logic style capable of achieving significantly higher speeds while consuming less power than traditional CMOS circuits, especially at high frequencies [17]. CNFET is recognized for its superior device current carrying capacity. The pivotal aspect driving the adoption of CNFET is its device structure and operational principles, which closely resemble those of CMOS devices. Consequently, it allows for the potential reuse of established and existing CMOS infrastructure [31, 32].

In reference [17], the author achieves an XOR/XNOR circuit implementation using CNFETs. The CNFET-based MCML XOR/XNOR circuit demonstrates superior design parameters contrasted to the MOSFET-based MCML XOR/XNOR circuit at nominal VDD. Therefore, among electronic devices in the nanoscale realm, CNFET stands out as a promising candidate. This is primarily attributed to its improved electronic characteristics and notable speed enhancements. The acceleration in speed, particularly due to scaling down to 22-nm and 10-nm technology nodes, has fuelled the advancement of CNFET technology. The author introduced CNFET based simultaneous non-full-swing and full-swing XOR/XNOR gates utilizing PTL technology [20].

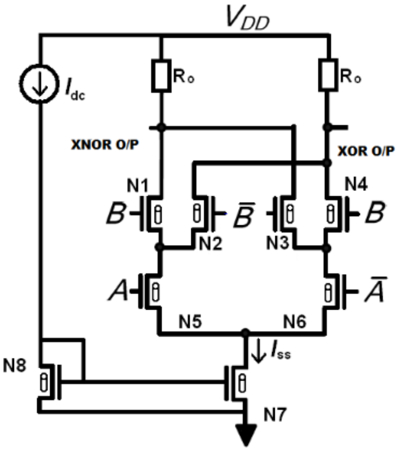
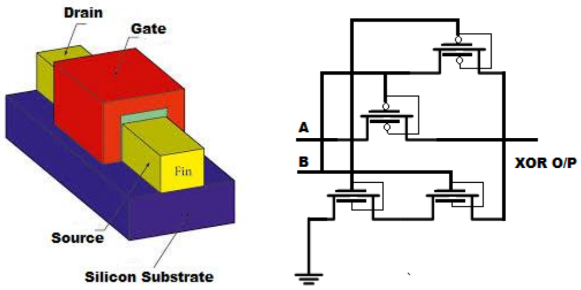


Fig. 7 XOR /XNOR implementation using CNFET [17]

These designs exhibit increased power consumption due to feedback usage and the additional inverter employed for the simultaneous production of XOR/XNOR output. Moreover, the author suggested P1-X and P2-X XOR/XNOR cell designs to execute 4-2 and 5-2 compressors. When compared to the top existing designs, the proposed XOR/XNOR cell demonstrates a reduction in PDP by up to 86.3%. Furthermore, these recommended designs display enhanced reliability in managing temperature, voltage, and process fluctuations [20].CNFET-XOR/XNOR gates were assembled in SR-CPL (Swing Restored CPL) logic within this paper, employing powerless and groundless pass-transistor configurations [33].The authors in research article [34] present diverse XOR/XNOR gate designs employing multiple logic paradigms implemented through CMOS, FinFET, and CNFET technologies. Upon comparison, it is concluded that among these three technologies, CNFET technology delivers the most optimal performance in terms of average delay, power consumption, and PDP [34].

2.6. FinFET implementation

In the nanometer range, short channel MOSFET devices encounter several impacts including punch-through, hot carrier impact, drain-induced hurdle lowering, and limited mobility leading to performance degradation. To address these challenges, FinFET technology emerges as a promising solution to improve the efficiency of low-power devices operating at low voltages. Fig.8 (a) demonstrates the structure of a FinFET, characterized by its three-dimensional configuration, with elevated source and drain areas and gates encompassing the channel region [35]. Compared to alternative technologies, FinFETs offer advantages in power efficiency, propagation delay, fan-in and fan-out capabilities [36].Simulating a FinFET device poses greater challenges. Accurately extracting parasitic elements from FinFETs proves to be considerably more challenging. Creating precise simulation SPICE models for FinFETs is notably more arduous compared to planar technologies [37]. Moreover, the dissipation of heat is less efficient in FinFET design due to the fins' tendency to retain heat [38].



(a) (b)

Fig. 8 (a) FinFET structure (b) FinFET implementation of XOR gate [19]

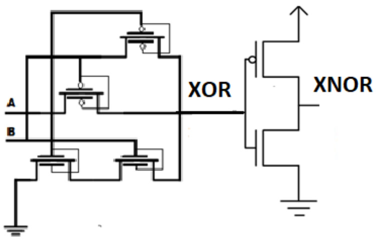


Fig. 9 FinFET based XOR/XNOR cell

The utilization of FinFET technology for implementing the XOR gate is illustrated in Fig. 8 (b) [19]. Assessing the variability of Energy-Delay Product (EDP) is also conducted to exhibit the design's robustness, considering EDP's significance as a crucial circuit metric [19]. Utilizing FinFETs allows for a reduction in transistor count in multi-input logic circuits. An innovative proposal introduces a 4-bit XOR/XNOR cell employing a PTL design style [39]. This design, based on 20 nm FinFET technology, demonstrates favourable outcomes in terms of chip area, signal propagation latency, output swift, and ability to drive current. Furthermore, a 45 nm PTL- XOR/XNOR architecture using FinFET with a 0.7 V supply voltage is recommended, showcasing notably lower power consumption owing to the author's use of a low supply voltage [40].

3. Optimal Selection of XOR/XNOR Cell Design

A detailed discussion of various conventional and non-conventional design methodologies for the designing of XOR/XNOR cell is performed in section 2. This research article provides an in-depth understanding of the importance of each technology. To find the optimal selection of XOR/XNOR cell a comparative analysis has been carried out in this section. The performance of these circuits has been compared on the bases of circuit design parameters. Table 1 shows the simulation results of various XOR/XNOR cell implementations in terms of circuit design parameters. The simulation results for XOR/XNOR cells referenced in [2], [7], [15], [17], and [23] have been obtained from the research article [9]. In contrast, simulations were conducted independently for the XOR/XNOR cell depicted in Fig. 6 and Fig. 9 in the current research. These simulations were conducted on HSPICE tool at 22nm technology node with 0.7V supply. The table 1 presents evidence that CNFET technology outperforms other design methodologies in terms of speed, achieving a remarkably low delay of 2.27ps. It is evident that CNTFET technology, with its ballistic carrier transport, proves suitable for high-speed applications.

Table 1 Summary of XOR/XNOR cell design parameters

Ref.	Technology Used	Delay (ps)	PWR (μW)	PDP (aJ)	EDP (aJ-ps)	Transistor count
[28]	Static CMOS	14.42	2.105	30.3541	437.7061	10
[25]		22.01	2.68	58.9868	1298.299	10
[2]		14.86	2.169	32.23	478.95	10
[23]		32.64	2.65	86.5	2823.2	6
[7]	Domino CMOS	5.341	0.314	1.675	8.946	9
[15]		50.11	0.477	23.9	1197.75	15
[16]		15.94	7.23	115.23	1837.02	8
P3-S[20]	CNFET	35.21	0.059	2.07739	73.1449	8
P4-S[20]		32.47	0.0611	1.983917	64.41778	10
[17]		2.27	44.2	100.5	228.6	10
Design in fig.9	FinFET	14.23	0.0049	0.0697	0.992	6
Design in fig.6	FGMOS	12.73	0.004	0.0509	0.649	5

Additionally, it's noticeable that domino logic operates at a higher speed compared to the static logic style. The comparative analysis showcased that the domino logic approach outperforms static logic due to its reduced transistor count, yet it's affected by a charge sharing issue between nodes, impacting its performance. The data in the table indicates that FGMOS technology consumes the least power (4.001 nW) in terms of the circuit's power consumption. Furthermore, the data clearly shows that unique devices (like CNFET or FinFET) or unconventional design strategies (like FGMOS) produce higher outcomes across all design metrics for lower technology nodes. FGMOS technology, on the other hand, is well suited for low voltage and low power applications since it provides threshold tunability and numerous input possibilities. Therefore, it is crucial to determine which design approach is best for the given application. PDP is indeed an important figure of merit for any digital circuits. Utilizing the PDP results from table 1, a bar chart is shown in fig.10 to visually represent a fair comparison among distinct design methodologies for XOR/XNOR cells. This graphical representation enhances the understanding of the comparative efficiency in terms of power consumption and speed across the various design approaches. The bar chart makes it clear that static CMOS technology has a much higher PDP than alternative design methods such as CNFET, FinFET, and FGMOS in this comparison. These findings are specific to the 22 nm technology node.

In the conventional designs of XOR/XNOR cells, we have adopted the practice of using the minimum transistor size. Specifically, for NMOS transistors, the width-to-length ratio (W/L) is set to 1, while for PMOS transistors, the W/L ratio is considered as 2.5. For CNFET designs, each device is characterized by four tubes, and the chirality of the tube is specified as (19,0). These parameters have been carefully selected to ensure a consistent and standardized approach in our comparative analysis.

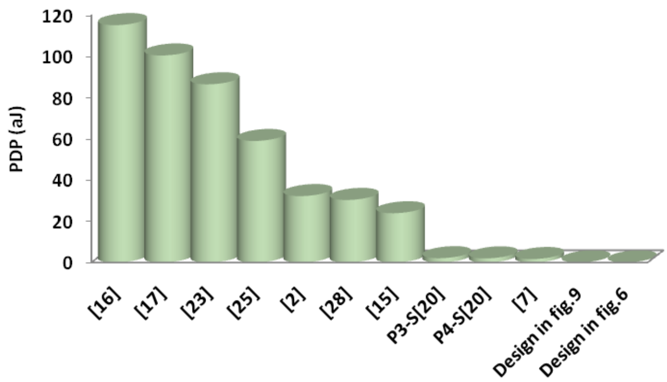


Fig. 10 PDP comparison

Hence, it is recommended that non-conventional design methods offer advantages at lower technological node for low voltage and low power applications.

4. Analysis of Voltage and Temperature Variations for Conventional and Non-Conventional XOR/XNOR Cell Designs

The impact of supply voltage and temperature fluctuations on conventional and unconventional XOR/XNOR cell has been examined in this section. Given the prominence of variability in deep submicron technology, the analysis of PDP variability is conducted using Monte Carlo (MC) simulations, representing a crucial aspect in design metrics. In this study, the design metrics are assessed with a sample size of 2000 to attain an even greater level of accuracy. Moreover, the influence of voltage fluctuations on PDP has been examined for various supply voltages. It's anticipated that in the near future, the potential variance in supply voltage might be around 10% [41]. Consequently, the variability is assessed by adjusting the supply voltage within the range of 0.6V to 1V. The simulation results for the voltage variations are shown in table 2.

Table 2 Simulation results for supply voltage variation

Supply Voltage (V)	PDP (aJ)						
	[15]	[22]	[20]	[21]	[7]	[19]	FGMOS
0.6	22.32	4.8	2.2	1.78	1.55	0.51	0.049
0.7	23.58	5.02	2.52	1.872	1.67	0.67	0.0509
0.8	23.9	7.02	2.83	1.988	1.786	0.78	0.061
0.9	26.04	13.34	2.95	2.106	1.98	0.98	0.0731
1	29.13	27.04	3.123	2.232	2.1	1.005	0.0798

The bar graph displayed in Fig. 11 distinctly illustrates that the FGMOS based XOR cell exhibit minimum variation against this voltage range.

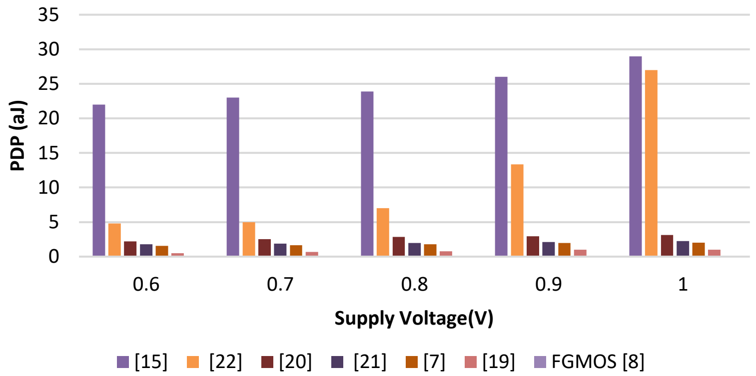


Fig. 11 Voltage resilience analysis

Evaluating the resilience of the proposed design, assessments for both temperature and voltage variability have been conducted. The impact of temperature-related variations on all design metric (PDP) has been thoroughly investigated across a range from -20°C to 100°C. The simulation results demonstrate minimal variations for the FGMOS based XOR/XNOR cell design across this extensive temperature spectrum, the same is shown in fig.12.

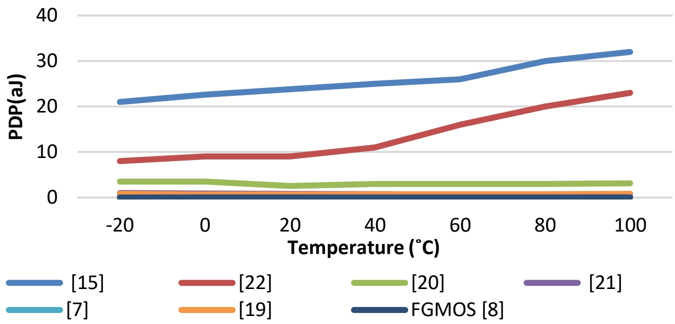


Fig. 12 Temperature resilience analysis

5. CONCLUSION & FUTURE SCOPE

In this research work, XOR-XNOR cells which are essential in a variety of excellent performance arithmetic logical algorithms in LPLV VLSI architectures are thoroughly examined using both traditional and non-conventional design methodologies. While FinFET, CNFET, and FGMOS are regarded as non-traditional design techniques, static and dynamic CMOS technologies are considered conventional design approaches. The study compares different XOR/XNOR cells reported in the literature in terms of circuit design characteristics and discusses the difficulties posed by these methods. Findings show that while FGMOS technology excels in power efficiency, utilizing CNTFET technology at lower technological nodes considerably enhances circuit speed. The HSPICE tool at the 22nm technology node is used in the paper to assess the voltage and temperature resilience of these XOR/XNOR cells using the Predictive Technology Model (PTM) [42]. It is observed that the XOR/XNOR cell based on FGMOS displays the highest robustness to voltage and temperature fluctuations. The adoption of non-conventional technologies is hindered by the absence of appropriate simulation models and the intricacy of fabrication processes. Therefore, there is a pressing need to focus on developing additional simulation tools and simplifying the complexity associated with these innovative technologies.

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