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Original scientific paper

SUCCESSIVE IRRADIATION AND BIAS TEMPERATURE STRESS INDUCED EFFECTS ON COMMERCIAL P-CHANNEL POWER VDMOS TRANSISTORS*

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Abstract. *This study examines the effects of negative bias temperature (NBT) stress on irradiated commercial p-channel power VDMOS transistors, with a focus on contribution to threshold voltage shift of changes in gate oxide charge and interface traps. The research addresses the critical reliability concerns for these transistors, as shifts in the threshold voltage can notably influence device performance, particularly under conditions of elevated temperature and negative gate oxide fields. Considering that VDMOS transistors are power devices, high temperatures occur during their operation, which can cause NBT effects, and this definitely affects normal operation. Furthermore, the study investigates the implications of irradiation on the electrical parameters of VDMOS power transistors, highlighting the need for a thorough understanding of these effects. The experimental methodology includes both irradiation and subsequent NBT stress application. This paper provides a detailed analysis of both static and pulsed NBT stressing, with an emphasis on novel stress signals related to practical applications. The data presented in the paper were obtained by exposing components to NBT stresses with different polarizations on the gate, which were previously exposed to radiation to different doses, with and without polarization. Also, the results with different frequencies applied during NBT stress are presented. Results from the study elucidate the roles of gate oxide charge and interface traps in contributing to threshold voltage shifts, thereby offering critical insights into the reliability of p-channel power VDMOS transistors in various operational stress scenarios. Self-heating during both the operational and cooling phases of fresh and previously irradiated components were measured using IR camera These findings are*

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instrumental for the design and operation of electronic systems that utilize these transistors, ensuring improved reliability and performance.

Key words: *reliability study, gate oxide charge, interface trap, threshold voltage, irradiation, self-heating*

1. Introduction

The Vertical Double Diffused Metal-Oxide Semiconductor (VDMOS) power transistor exhibits distinct characteristics that have established its utility across diverse commercial and specialized applications. Notably, VDMOS transistors possess a high drain-to-source breakdown voltage and can accommodate substantial drain currents. These attributes render them indispensable in the regulation of power within household electrical appliances, industrial machinery, and military electronics. Additionally, they play a critical role in the functioning of switching power supplies and audio amplifiers and are integrated into complex systems serving both primary and ancillary functions in the automotive sector. Given their deployment in various applications, VDMOS power transistors are often subjected to rigorous operational conditions and stresses. This has engendered a growing interest in the assessment of their performance and behavior in specific contexts and environmental scenarios, underscoring the imperative for their reliable operation. However, the reliability and longevity of these devices are closely linked to variations in threshold voltage (V_T). The threshold voltage is a pivotal parameter in VDMOS power transistors, significantly influencing their operational mode. Particularly in p-channel MOSFETs operating at elevated temperatures, between 100 °C and 250 °C, and subjected to negative gate oxide fields, from 2 MV/cm to 6 MV/cm, instability issues associated with Negative Bias Temperature Instabilities (NBTI) [2] may arise.

The phenomenon of threshold voltage shift is notably observed in certain applications where power transistors are exposed to severe operational conditions and various forms of stress. Specifically, radiation environments can induce significant degradation in the electrical parameters of VDMOS power transistors [3]. During the exposure to irradiation, notable changes such as reductions in transconductance and breakdown voltage, an increase in leakage current, and crucially, alterations in threshold voltage can be observed [4, 5]. Deviations in any of the designed parameters of these devices beyond their specified ranges may lead to failure. Consequently, investigating the processes underlying NBTI effects, as well as radiation-induced effects, is critically important [6]. Besides the high susceptibility of PMOS transistors to individual stress factors, there are applications in which they may encounter simultaneous NBT stress and irradiation. Given the constraints in applying NBT stress and radiation concurrently, these stress factors were applied sequentially in the conducted experiments.

Additionally, given the widespread application of p-channel VDMOSs in high-frequency switching circuits, attributed to their superior switching performance [7-10], it becomes crucial to investigate the behavior of these devices under pulsed stress conditions, as such conditions are prevalent in most practical circuit applications. This paper highlights the practical deployment of p-channel power VDMOSs [11], with a primary focus on elucidating the underlying physics and processes during static and pulsed NBT stress. Specifically, it addresses the effects of novel stressing signals that these power VDMOSs encounter in real-world applications.

These effects are attributed to electrochemical processes that generate and/or activate defects within the gate oxide and at the interface between the gate oxide and silicon [12-

14]. Both the gate oxide charge and interface traps contribute to the increase in the threshold voltage (in absolute value). This paper seeks to further elucidate the effects observed in p-channel power VDMOS transistors subjected to the irradiation and NBT stress by specifically analyzing the contributions of the gate oxide charge (ΔV_{ot}) and interface traps (ΔV_{it}) to the resultant threshold voltage shifts (ΔV_T). This analysis aims to provide valuable insights into addressing reliability concerns associated with devices integrated into the electronic equipment [15-17].

2. Literature Review

Despite extensive research over the years into the reactions and processes occurring in VDMOS power transistors under NBT stress and irradiation, this topic remains highly relevant. Many authors analyze the processes from various perspectives. For example, in the paper [5] MOSFETs were exposed to gamma radiation at varying doses to investigate the mechanisms of the radiation-induced interface trap generation and oxide-trapped charge accumulation. For the first time, the influence of the channel orientation on radiation effects was explored. The findings revealed an initial positive shift in the threshold voltage at low irradiation doses, followed by a negative shift as the dose increased. At higher doses, the rapid generation of radiation-induced interface traps prevailed over the accumulation of oxide-trapped charges, resulting in a positive shift in threshold voltage. Besides the radiation, NBT is additionally elucidated in [18]. In that paper, the authors investigate the impact of the hydrogen molecule release on NBTI through the low-temperature pre-treatment (LTPT) in p-channel power VDMOS transistors. They found that the threshold voltage (TH) behavior under NBTS shows two phases: an initial rapid increase due to interface traps and oxide charges, followed by the stabilization. LTPT intensifies the TH increase during NBTS by generating more interface traps, indicating that while LTPT enhances overall device performance, it does not mitigate NBTI. Additionally, LTPT accelerates the hydrogen molecule formation, promoting the oxide charge conversion to interface traps and accelerating the Si-H bond breakdown, suggesting that reducing hydrogen-related impurities can help mitigate NBTI.

It can be observed that increasing efforts are being directed towards developing models that encompass various parameters and predict their behavior. In that style, in the paper [19] authors examined the degradation of the on-state resistance in power MOSFETs under Bias Temperature Instability. By dividing the resistance into NBTI-affected and unaffected parts, the authors developed a first-order linear model to predict the resistance behavior under high gate voltage and temperature. Furthermore, the paper [20] proposes a comprehensive model for describing the threshold voltage instability during and after NBT stress in MOS structures. It integrates three types of traps: interface traps, border traps, and bulk traps, yielding a detailed yet manageable framework. To validate the model, separate measurements of trap contributions to the threshold voltage shift are suggested, allowing comparisons with model predictions. During stress, border traps have minimal impact, comprising only around 2% of the threshold voltage shift, while the recovery is primarily governed by border traps alongside interface traps. The model requires only two free parameters for the recovery, demonstrating its efficiency and versatility across various experimental conditions without parameter adjustments. Its strengths include separate extraction of trap contributions, validation across diverse conditions, and

facilitation of accurate reliability assessments for time-to-failure predictions. Additionally, there are studies focusing on radiation modeling [21], as well as works focusing on the analysis and modeling of PBT stress [22].

In recent years, there has been a significant attention in studies focusing on NBTI [23], Hot Carrier Injection (HCI) [24], and Time-Dependent Dielectric Breakdown (TDDB) [25]. The advent of new measurement techniques, which depict effects that were previously undetectable, has led to a substantial interest in investigating NBTI, particularly the electrochemical mechanisms underlying the observed changes. This expanding interest has catalyzed a series of investigations by various research groups. Table 1 summarizes some of the recent studies on these aspects.

Table 1 Recent investigations obtained by various research groups

Paper's first author and year	Different aspects of research													
	Irradiation	NBTI stress	PBTI stress	BTI and other stresses	Determ. of traps	Modeling and Simulation	TCAD simul.	Transfer characteristics	Recovery	Activation energy	Energy bands	Electro. reactions	Magnetism	Lifetime
Grasser *et al.* in 2011 [2]				X	X	X			X		X			
Zhang *et al.* in 2023 [5]	X				X			X			X	X		
Qin *et al*. in 2019 [6]	X				X			X			X	X		
Bhattacharjee *et al.* in 2022 [8]		X			X						X			
Zeng *et al.* in 2011 [13]	X				X				X					
Sun *et al.* in 2011 [14]	X				X	X			X					
Tripathy *et al*. in 2022 [15]						X	X	X						
Li *et al.* in 2023 [16]	X				X			X			X			X
Lazzaz *et al.* in 2022 [17]						X	X	X						
Liu *et al.* in 2024 [18]		X		X	X			X		X				
Wang *et al.* in 2023 [19]		X				X					X			X
Irrera *et al.* in 2024 [20]		X			X	X		X	X					
Liu *et al.* in 2023 [21]	X				X	X	X	X				X		
Ye *et al.* in 2018 [22]			X		X	X		X						
Yang *et al*. in 2022 [26]		X				X	X	X						X
Xue *et al*. in 2024 [27]			X			X	X	X			X			
Zhao *et al.* in 2024 [28]		X	X			X	X	X		X	X			
Rinaudo *et al.* in 2024 [29]			X							X	X			
Guo *et al.* in 2022 [30]		X				X								
Biswas *et al.* in 2024 [31]		X	X	X	X						X			
Steinmann *et al.* in 2024 [32]		X	X		X		X				X			
Thakor *et al.* in 2024 [33]				X	X	X	X		X			X		X
Bonaldo *et al.* in 2024 [34]	X				X	X		X	X		X			X
Wang *et al.* in 2024 [35]		X			X						X			X
Contamin *et al.* in 2024 [36]		X	X			X			X		X			
Ghosh *et al.* in 2024 [37]				X					X					
Singh *et al.* in 2023 [38]									X					X
Zheng *et al.* in 2023 [39]		X				X		X						
Li *et al.* in 2024 [40]		X			X		X	X						X
Liu *et al.* in 2024 [41]		X			X		X	X						X
Tahi *et al.* in 2021 [42]								X					X	
Tahi *et al.* in 2021 [43]								X					X	

2. Experimental Procedure

Over the years, a significant number of experiments have been conducted by this research group, addressing both radiation effects and negative bias temperature stresses. These efforts have closely followed global scientific trends, the findings of other researchers, and the requirements for supplementing our own experiments. Consequently, a wide range of stress combinations, reflecting those encountered in real-world applications, have been realized.

Throughout this paper, components under commercial code IRF9520 [9] are analyzed. These components are power VDMOS transistors, with the silicon gate and p type of the channel. Due to the very thick oxide of the gate, which is around 100 nm, and the presence of 1650 hexagonal cells, these devices can hold high values of currents and voltages. The individual components were encapsulated within the plastic TO220 packaging, providing the space for mounting the heatsink.

Generally, there are two main parts of the experiment, device irradiation and device negative bias temperature stress. The process of irradiation took place at the Institute for Nuclear Sciences, which is located in Vinča, Serbia. The metrological laboratory, which is part of the Department of Radiation and Environmental Protection, carried out the irradiation. The devices were exposed to Co-60 gamma radiation at a dose rate of 0.5 Gy(SiO_2)/min, with cumulative doses reaching 30 Gy, 60 Gy, 75 Gy, 90 Gy, and 120 Gy with different polarizations during the process. In Fig. 1 it can be seen the schematic representation of used equipment.

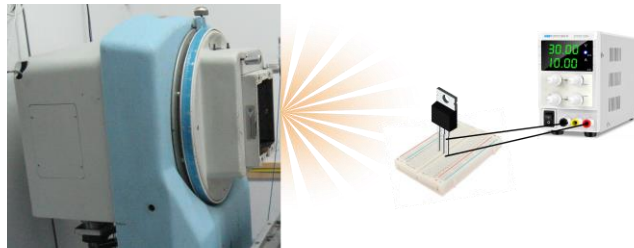


Fig. 1 Illustration of the experimental setup for the irradiation study

Irradiation was performed at room temperature under conditions both with and without gate voltage applied, while the source and drain terminals were maintained at ground potential. The application of low-dose rate irradiation to electronic equipment presents challenges. The current problem concerns the operational efficacy of the components, as the user is unaware of the processes by which the parameters of these components are modified. The subsequent critical experimental phase involved the NBT stress, conducted at the Laboratory for Microelectronics and Electronic Components within the Faculty of Electronic Engineering. For this part of the experiment, two sets of equipment are necessary, both schematically presented in Fig. 2 and Fig. 3.

Fig. 2 clearly shows the presence of a signal generator that allows the component to be exposed to accurately defined signals that are specific to certain applications. The figure also presents an oscilloscope used to verify signal accuracy, along with a heating chamber facilitating experiments at elevated temperatures. In NBT experiments, the components are usually subjected to a high bias, which requires the use of a power source.

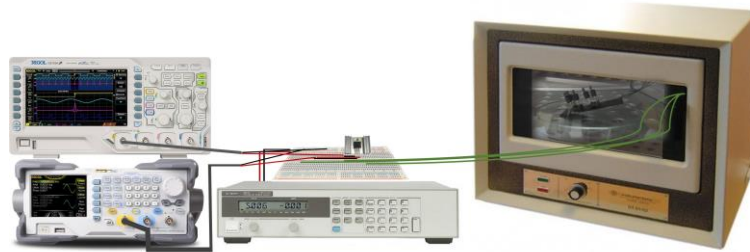


Fig. 2 Schematic representation of the stress setup

Fig. 3 Schematic representation of the *I-V* measurement setup

The second part of this setup (Fig. 3) includes devices for measuring *I-V* characteristics. For the source measurement unit (SMU), a Keysight B2901A was utilized, controlled via computer and corresponding software. To conduct measurements, samples undergo stress interruption, their *I-V* characteristics are measured, and then they are returned to stress. After obtaining the *I-V* characteristics, the midgap method was used to derive most of the results discussed in this paper. The data analysis and results were generated using a custom-written script in Octave software. From these *I-V* characteristics, the threshold voltage change is determined, which is crucial for further VDMOS application.

Details of the experiments are schematically illustrated in the following diagrams, Fig. 4 and Fig. 5. At the start, a large set of samples was irradiated to different doses at room temperature. These dose values were 30 Gy, 60 Gy, 75 Gy, 90 Gy, and 120 Gy, with samples being irradiated under different polarizations of -10 V, 0 V, and +10 V. Following this phase of the experiment, a spontaneous recovery at room temperature without gate bias was conducted, Fig. 4 and Fig. 5. Subsequently, the second, highly significant part of the experiment, NBT stress, was performed. An important aspect is that fresh components were also subjected to NBT stress within the scope of the experiments. Two types of NBT stress were applied: static and pulsed stress, Fig. 4 and Fig. 5.

During static NBT stress, the components were subjected to a temperature of 175 °C with an applied gate voltage of -45 V for 168 hours. As can be observed, components with all absorbed doses were subsequently subjected to the static NBT stress. On the other hand, not all irradiated components were subjected to the pulsed NBT stress. These groups of components will be the focus of investigation in some future experimental procedures. The pulsed NBT stress process consisted of two phases.

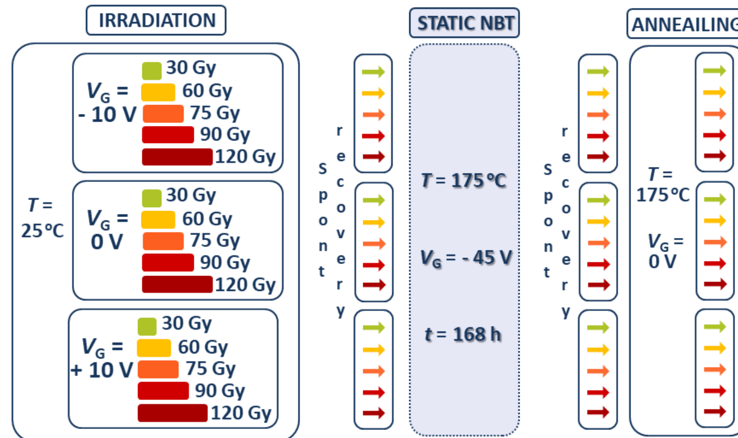


Fig. 4 Schematic representation of the experimental conditions during irradiation and subsequent static NBT stress

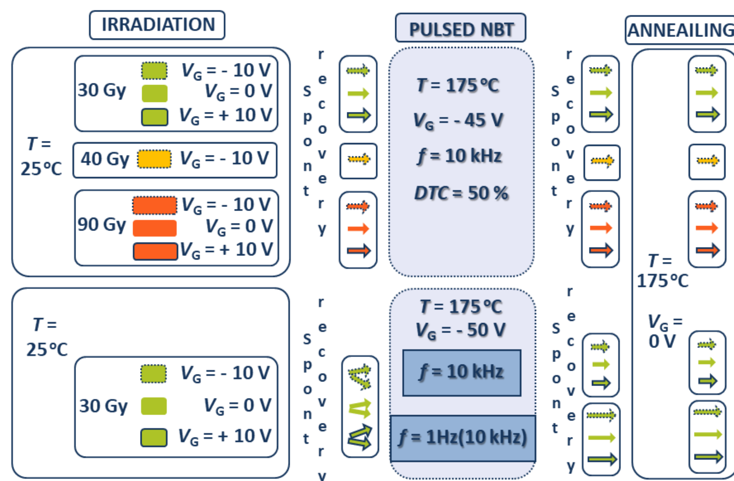


Fig. 5 Schematic representation of the experimental conditions during irradiation and subsequent pulsed NBT stress

In the first part of the pulsed NBT stress, with parameters $f = 10$ kHz and DTC = 50 %, the gate voltage of – 45 V was applied to the devices irradiated up to 30 Gy, 40 Gy and 90 Gy. In the second part of the experiment, the gate voltage of – 50 V was applied only to the irradiated devices up to 30 Gy. These components were subjected to two different types of signals: 1) $f = 10$ kHz and DTC = 50 % (controlling the motor with the PWM signal); 2) $f = 1$ Hz (10 kHz) i.e. in the first half of the period consists of the PWM signal ($f = 10$ kHz, DTC = 50 %), and in the second half of the period, the motor was turned off (in signal of the frequency of 1 Hz, it is embedded part of 10 kHz) [11].

To better elucidate the experimental results obtained from previous experiments, a subset of samples that had not been previously irradiated was subjected to the pulsed

NBT stress. The experimental conditions are schematically depicted in Fig. 6. It can be seen that the fresh samples were stressed with signals of $f = 10$ kHz and $V_G = -45$ V, and $f = 1$ Hz, $f = 10$ kHz, $f = 1$ Hz (10 kHz), and $V_G = -50$ V, while DTC of all signals was 50 % (continuously turning the motor on and off in 0.5 s intervals). All samples were submitted to post-stress annealing. Subsequently, not all results are presented, as such comprehensive analysis would exceed the scope of this study; however, characteristic combinations are provided.

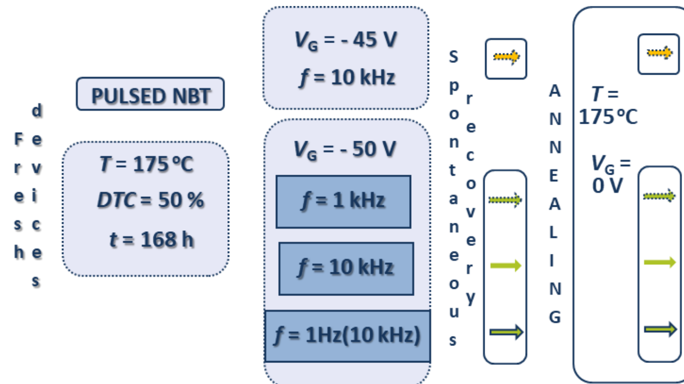


Fig. 6 Schematic representation of the experimental conditions during NBT stress of fresh components

The following tables, Table 2 and 3, list specific samples, their names, and the stress conditions to which they were subjected.

It is noteworthy that the difference in sample names arises because the samples were procured at different times. To avoid any confusion regarding the origin of each sample, distinct labels are used. In conducting the experiments, samples were consistently selected based on matching *I-V* characteristics, ensuring identical initial conditions.

Table 2 Components used for the irradiation induced NBTI (first part) experiment

<table>
<tr><th colspan="2">Irradiation parameters</th><th>90 Gy</th><th colspan="2">30 Gy</th><th>120 Gy</th></tr>
<tr><td rowspan="2">Polarization</td><td>0 V</td><td>SD46, S4</td><td>S15</td><td>S12</td><td>S1</td></tr>
<tr><td>-10 V</td><td>SD60, S8</td><td>SD64, SD66, S19</td><td>S10</td><td>S9</td></tr>
<tr><td colspan="2" rowspan="2">NBT stress parameters</td><td colspan="2">Pulsed: f = 10 kHz DTC = 50 %</td><td colspan="2">Static</td></tr>
<tr><td colspan="4">$T = 175$ °C $V_G = -45$ V</td></tr>
</table>

Table 3 Applied signal properties and parameter values during NBT stress

<table>
<tr><th>f</th><th colspan="3">T = 175 °C V_G = -45 V DTC = 50 %</th></tr>
<tr><td>10 kHz</td><td colspan="3">S16, S42, S43, S45, S46, S58, S59, S60</td></tr>
<tr><td>1 kHz</td><td>S47, S48, S49</td><td>S50, S51</td><td rowspan="2">Previously static NBT: T = 175 C V_G = -45 V</td></tr>
<tr><td>1 kHz (f_1=10 kHz)</td><td>S11, S14, S21, S61, S52, S53</td><td>S54, S55, S65</td></tr>
</table>

3. Results and Discussion

Fig. 7 (a) illustrates the changes in threshold voltage for components irradiated up to 30 Gy, 90 Gy, and 120 Gy. For all absorbed doses, during irradiation, voltages of +10 V and -10 V were applied to the components, while a subset of components was irradiated without any applied bias. A noticeable increase in the absolute value of the threshold voltage is observed across all cases. It is evident that the threshold voltage shift is more pronounced in components irradiated with the applied bias. Additionally, this increase is slightly more significant in those components that were irradiated under the positive bias.

Additionally, Fig. 7(b) shows the threshold voltage variations during the static NBT stress. Throughout this process, all components were subjected to a gate bias of -45 V, while the temperature was elevated to 175°C. A significant decrease in the absolute value of the threshold voltage is observed in components previously irradiated up to doses of 90 Gy and 120 Gy under polarization. This decrease is more evident for devices formerly irradiated up to higher dose (120 Gy). For other components, which were irradiated without polarization as well as those irradiated up to 30 Gy with polarization, an increase is observed. This increase is most pronounced in components irradiated up to 30 Gy without polarization. It can be seen that changes of the threshold voltage are significant in the initial phase of static NBT stress, while in the later phase, the changes are significantly reduced. The explanation for such threshold voltage behavior would be that in devices irradiated without polarization, fewer defects are formed. So, the subsequent stress, which was applied, additionally created more defects, and this is the reason why there is an increase in the absolute value of the threshold voltage shift. For components irradiated under polarization, but only up to 30 Gy, they also have an increase in threshold voltage shift during NBT, due to the smaller number of defects. In fact, they have a similar threshold voltage shift behavior during static NBT stress like components irradiated without any polarization.

The subthreshold midgap technique was utilized for the quantitative determination of the specific contributions of oxide trapped charge and interface traps to the change in threshold voltage. These contributions, ΔV_{ot} and ΔV_{it} are shown in Fig. 8 and Fig. 9, respectively. The first part of figures (Fig. 8a and Fig. 9a) shows changes of ΔV_{ot} and ΔV_{it} during the irradiation, while the second part of figures (Fig. 8b and Fig. 9b) shows these changes during the static NBT stress. The applied NBT stress was performed at T = 175 °C and V_G = - 45 V. In all stressed devices, the contributions of the gate oxide charge to the threshold voltage shift were observed to be larger than that of the interface traps [12].

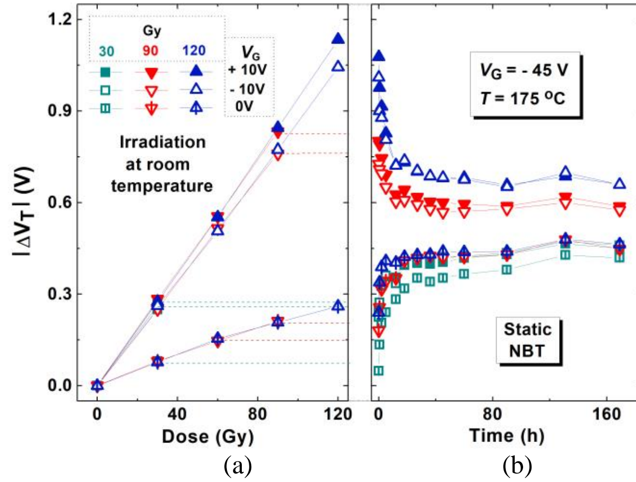
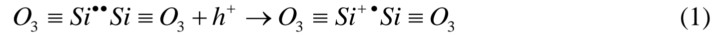


Fig. 7 Threshold voltage shift during: (a) irradiation (with and without gate bias) and (b) static NBT stress

The underlying changes in the density of positive charge in the gate oxide and interface states are attributable to electrochemical reactions occurring during NBT stressing [21, 33]. Initially, positive charge accumulation in the oxide is observed due to the trapping of holes at defects within the oxide, such as oxygen vacancies, Equation 1.



$$O_3 \equiv Si^{\bullet\bullet}Si \equiv O_3 + h^+ \rightarrow O_3 \equiv Si^{+\bullet}Si \equiv O_3 \quad (1)$$

Also, due to the strong electric field, the dissociation of the weakest Si-H bonds occurs at the interface. It is represented by the electrochemical Equation 2.

$$Si_3 \equiv Si - H \leftrightarrow Si_3 \equiv Si^{\bullet} + H^{\bullet} \quad (2)$$

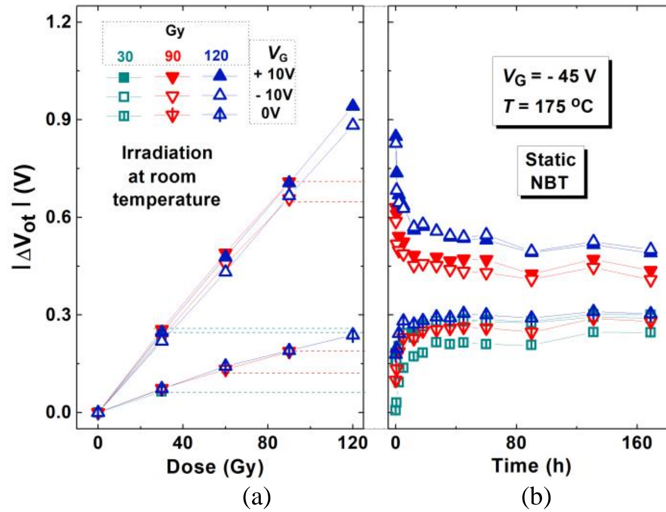


Fig. 8 Threshold voltage shift contributions of gate oxide charge during: (a) irradiation (without and with gate bias) and (b) static NBT stress

These electrochemical reactions are part of a chain of electrochemical processes occurring in the oxide of components and at the interface. The reactions involving hydrogen particles significantly influence the electrochemical processes. Highly reactive hydrogen atoms interact, neutral H_2 molecules diffuse, and positive H^+ ions drift, interacting with defects and weakened bonds. Consequently, practically all electrochemical reactions leading to the formation of charge in the oxide and interface traps are defined by the total amount of hydrogen particles present at and near the silicon dioxide-silicon (SiO_2-Si) interface. Additionally, the overall number of defects in the oxide and at the interface determines the processes of forming trapped positive charge in the gate oxide and interface traps. This results in changes of the threshold voltage, which is one of the most critical parameters of commercial VDMOS power transistors.

The threshold voltage shift contributions of gate oxide charge and interface traps during irradiation and pulsed NBT stress are shown in Fig. 10. In unstressed devices, pulsed voltage stressing typically results in smaller shifts compared to static stressing under identical temperature and gate voltage conditions, attributable to the partial recovery during the pulsed stressing. The pulsed stressing comprises alternating "on-time" and "off-time" phases. During the on-time phase, the applied voltage generates defects within the oxide and at the interface. In the subsequent off-time phase, a portion of these defects undergoes recovery, while the remainder leads to a permanent degradation. It should be noted that, opposite to the static NBT, during the pulsed NBT, notable decrease of ΔV_{ot} was observed only for devices irradiated up to 90 Gy with the negative gate polarization. This decrease in ΔV_{ot} was observed due to pronounced recovery processes. Also, there were no significant changes of both ΔV_{ot} and ΔV_{it} indicated in devices previously irradiated to a lower dose (30 Gy) and those without the polarization at both 30 Gy and 90 Gy. This indicates that in irradiated devices subjected to pulsed NBT stress (at the same temperature and gate voltage), recovery processes are more pronounced.

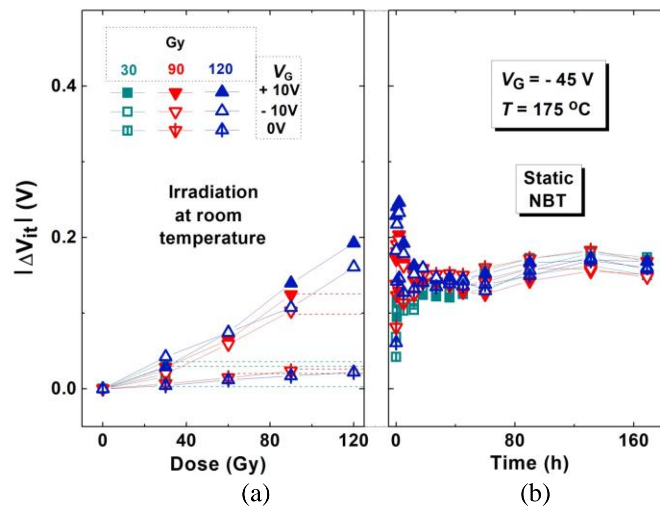
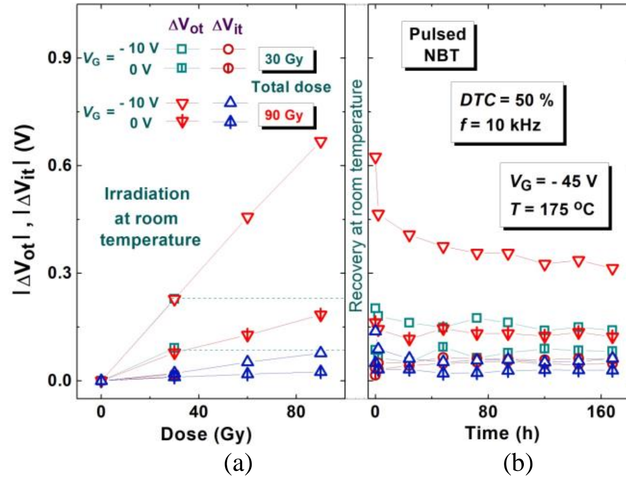


Fig. 9 Threshold voltage shift contributions of interface traps during: (a) irradiation (without and with gate bias) and (b) static NBT stress



(a) (b)

Fig. 10 Contributions of gate oxide charge and interface traps to the threshold voltage shift observed through applied: (a) irradiation performed without and with gate polarization; and (b) pulsed NBT stress

These variations in ΔV_{ot} and ΔV_{it} contribute to alterations in the threshold voltage shift, as depicted in Fig. 11, which illustrates the threshold voltage changes during the static and pulsed NBT stress with -45 V and -50 V polarizations.

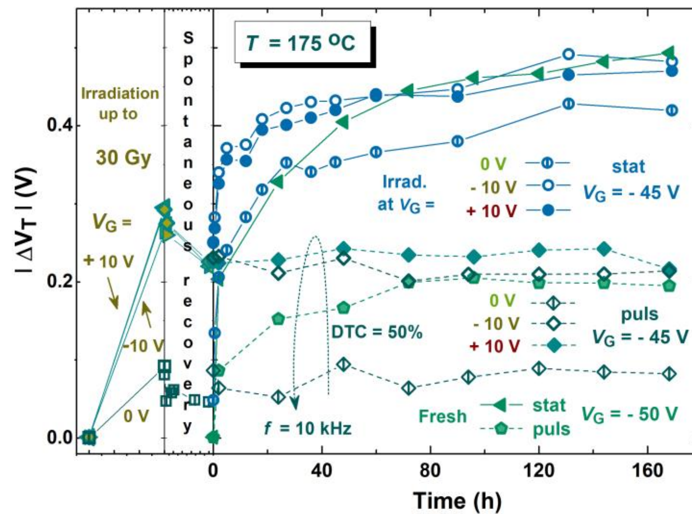


Fig. 11 Changes of threshold voltage observed through applied static and pulsed NBT stress performed with - 45 V and with - 50 V, for fresh and formerly irradiated components

The magnitude of threshold voltage change is compared between unstressed components and those previously irradiated up to 30 Gy, with (+10 V and -10 V) and without the polarization. Notably, the static stress induces more significant threshold voltage shifts for

both polarizations and in all devices. Fig. 11 also highlights that the irradiation with a positive polarization results in a larger ΔV_T compared to a negative polarization. This disparity persists even after the spontaneous recovery. During the NBT stress, a reduction in the threshold voltage change is observed, particularly pronounced in components previously irradiated under the negative polarization. This distinction is evident from the changes observed in components subjected to NBT stress at -45 V.

In order to better examine the changes which, occur in these devices, further analyses were obtained. In Fig. 12 changes of threshold voltage shift induced by the pulsed NBT stress in fresh and previously irradiated devices are presented.

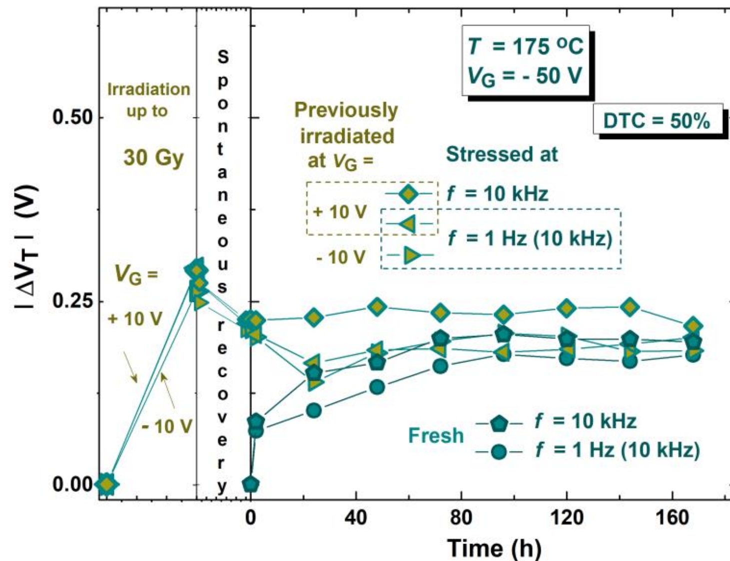


Fig. 12 Shift of the threshold voltage induced by pulsed NBT stress applied to fresh and to previously irradiated devices

It is evident that the changes occurring when components are stressed with the pulsed NBT, where they were previously irradiated with a polarization of ±10 V, are less pronounced in components stressed at 10 kHz compared to those stressed at a combination of 1 Hz and 10 kHz. Fig. 13 and Fig. 14 illustrate the corresponding contributions to the threshold voltage shift from gate oxide charge and interface traps induced by pulsed NBT stress (under conditions: T = 175°C and V_G = -50 V) in both fresh and previously irradiated devices.

Also, it can be seen that the fresh devices had the most prominent response to NBT stress whether static or pulsed. This is evident for the threshold voltage shift and for the contribution of the oxide trapped charge. Although these changes (for fresh devices) are larger, the values of ΔV_{ot} remain lower than the values for previously irradiated devices. As for devices exposed to different stress signals, it was established that in devices subjected to mixed stress signals, ΔV_{ot} is somewhat reduced. This can indicate that some recovery processes are more pronounced. As for the values of ΔV_{it}, it can be noticed that they are lower in devices exposed to mixed stressing signals.

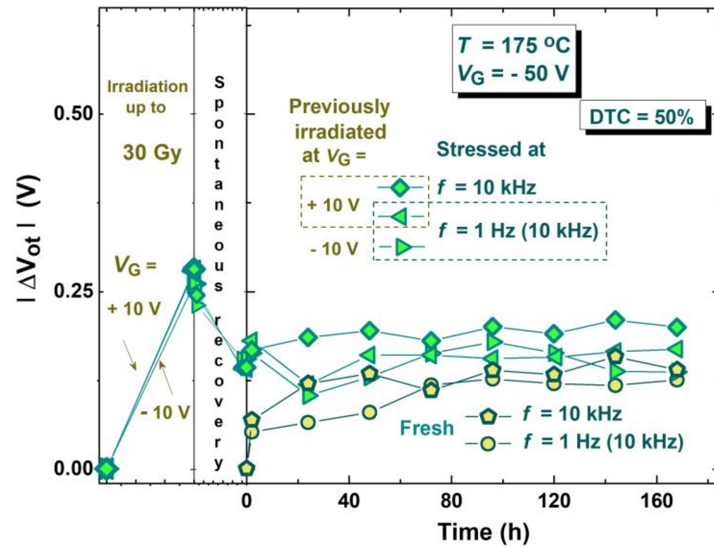


Fig. 13 Contribution of gate oxide charge to shift of the threshold voltage induced by pulsed NBT stress applied to fresh and to pre-irradiated devices

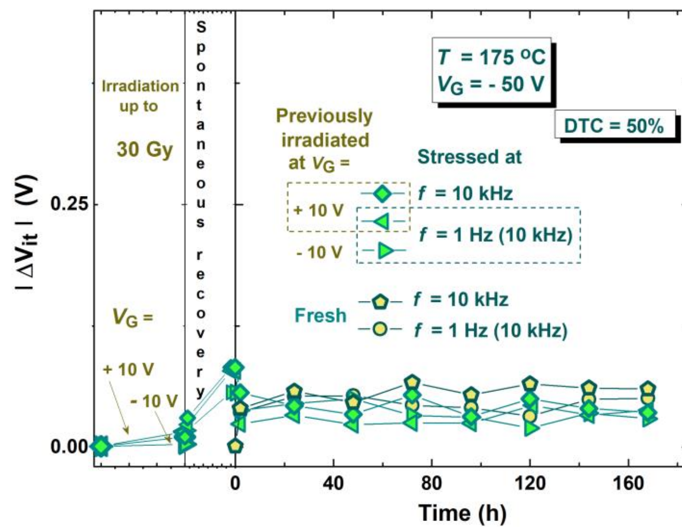


Fig. 14 Contribution of interface traps to shift of the threshold voltage induced by pulsed NBT stress applied to fresh and to pre-irradiated devices

4. SELF-HEATING IN NORMAL OPERATING CONDITIONS

As mentioned, VDMOS devices are extensively utilized in applications such as switching power supplies, automotive electronics, and the aerospace sector [44]. These devices typically operate at switching frequencies within the MHz range, making them suitable for a variety of

circuit applications. The characteristics of the control signal, including parameters such as the duty cycle, rise time, and fall time, manage the transistor's on-time and off-time intervals. When the control signal voltage exceeds the threshold voltage, V_T, the VDMOSFET operates as a closed switch; otherwise, it remains in an open switch state. However, the threshold voltage of the VDMOSFET is subject to a variation due to self-heating effects during the operation [45, 46]. In light of these considerations, the aim of this experimental segment was to evaluate the impact of the previous irradiation on the actual operating conditions of the devices.

The experimental setup used for conducting this part of the experiment was shown in Fig. 15. The examined samples were fresh and previously irradiated, up to 60 Gy with the gate polarization of - 10 V. All component groups were subjected to pulsed signals with parameters that matched the signals found in switching power supplies during the simulation of actual operating conditions. The signal applied to the tested sample was generated using an Agilent 33921A signal generator (1), configured to parameters of 1 Hz frequency, 100 ms rise and fall times, and a 50 % duty cycle. Additionally, a Rigol DL3021 active load (2) was integrated into the drain circuit. Alongside these instruments, a power supply (3) and a Rigol DS1202 oscilloscope (4) were employed to ensure that the component under the test received the correct signal. The temperature changes during the operation and cooling of both fresh and previously irradiated components were measured using a Flir E8 infrared camera (5) and corresponding software (6).

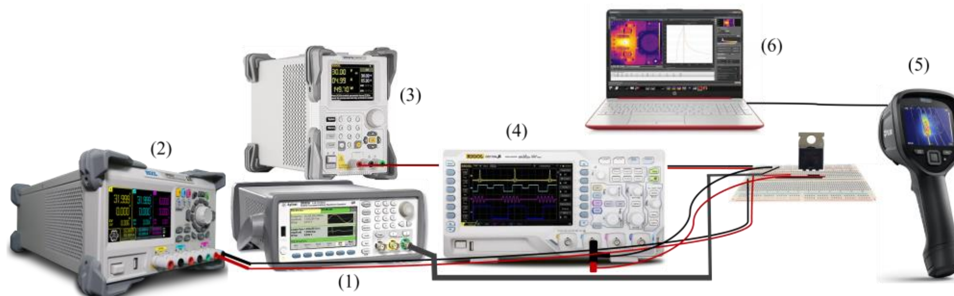


Fig. 15 Schematic representation of equipment used in this part of the experiment

Fig. 16 presents the absolute temperature variations over time under real operating conditions. This figure illustrates the results for p-channel power VDMOS transistors, comparing those with an irradiation history to fresh, unstressed samples.

In addition to analyzing the heating in greater detail, the subsequent cooling was also measured. These components exhibit the most considerable temperature changes because they were subjected to a current of 1.5 A, requiring the longest cooldown period among all devices tested, which is why these specific results are highlighted here. The graph in Fig. 16 reveals a temperature profile that does not exhibit consistent changes over time. The increase in the chip's temperature is primarily attributed to the effects arising from the power dissipation. Each pulse transition introduces additional stress to the device. Temperature rises during the duration of each pulse edge and decreases toward the thermal equilibrium during the off state. The temperature incrementally rises with an increased number of pulses. Furthermore, samples that had previously undergone stress

exhibited changes in the threshold voltage, with an increase in the absolute threshold voltage value. This elevation prolongs the duration of channel opening at the same gate voltage, resulting in current flowing through a higher resistance in stressed devices for extended periods, thus leading to the increased power dissipation.

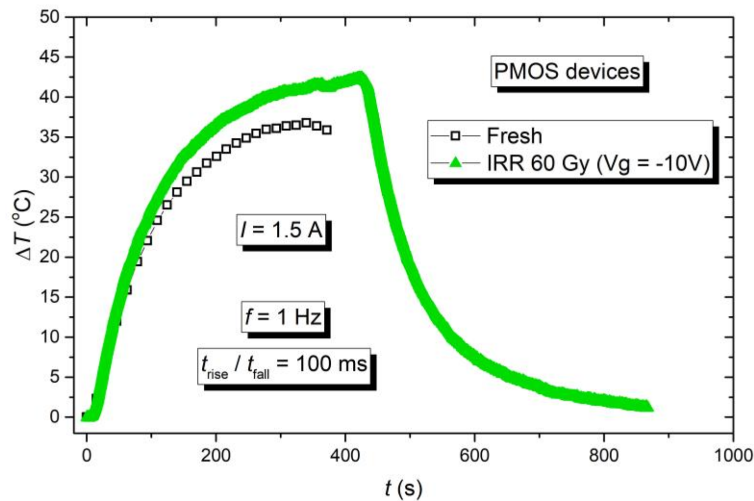


Fig. 16 Changes of absolute temperature value in PMOS devices with fresh and previously irradiated devices

5. CONCLUSION

The study required to elucidate the effects of the negative bias temperature (NBT) stress on irradiated commercial p-channel power VDMOS transistors by investigating contributions of changes in the gate oxide charge, ΔV_{ot}, and interface trapped charge, ΔV_{it}, and their impact on threshold voltage variations. Investigating the source of the change in the threshold voltage is crucial for ensuring the reliable operation of the components. For this reason, the mechanisms that are responsible for the formation of charges in the gate oxide charge and interface traps, and which thereby lead to a change in V_T, were additionally considered. The findings reveal that in devices previously irradiated with a lower dose of 30 Gy without polarization, static NBT stress resulted in increased values for both ΔV_{ot} and ΔV_{it}. Particularly significant alterations in gate oxide charge and interface traps were detected in non-irradiated (fresh) devices during the pulsed NBT stress. Nevertheless, irradiated devices (30 Gy) exhibited higher ΔV_{ot} values, correlating with more pronounced shifts in threshold voltage. For devices subjected to varied stressing signals, it was observed that those exposed to mixed signals experienced a slight decrease in ΔV_{ot}, suggesting the occurrence of certain recovery mechanisms. Moreover, the ΔV_{it} values were reduced in devices under mixed stressing conditions. These findings are consistent with previous research and provide additional insight into the electrochemical mechanisms occurring in the gate oxide. However, due to the need to better understand the mechanisms that cause these parameters to change, additional

comprehensive research will be conducted. Also, a part of the research was dedicated to self-heating of the devices. Research indicated that devices previously subjected to stress are more prone to the self-heating compared to fresh samples. Earlier processing of devices has led to the parameter degradation, evidenced by changes in threshold voltage. Variations in the threshold voltage impact the channel formation, causing delays in channel opening. This delay permits the current to flow through an increased resistance, resulting in the higher power dissipation and subsequent self-heating.

In the future, the components will be examined concurrently for their response to NBT as well as additional stresses like magnetic fields and radiation. Additionally, there are plans to conduct examinations in real-time operations. Afterwards, the aim is to conduct a thorough analysis and comparison of how these factors impact the self-heating process.

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