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**Original scientific paper**

# A NOVEL REVERSIBLE MULTILAYER FULL ADDER CIRCUIT DESIGN IN QCA TECHNOLOGY

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**Abstract:** *The QCA technology is a promising kind of nanotechnology that can replace the conventional CMOS technology due to high-speed, high-dense, and low power consumption properties. The QCA technology is based on the Coulomb repulsion and quantum cell instead of using a transistor. The QCA cell is a square structure with 4 dots placed at the square corners and 2 free electrons. The reversible circuits design is a technique that can reduce the power consumption in digital circuits design. In this technique, there is a one-to-one mapping between its input and output vectors. In addition, the input vector can always be formed from the output vector, and conversely, the output vector can also be formed from the input vector. As a result, using reversible technique in QCA digital circuit is an important issue. On the other hand, the full adder plays a vital role in digital circuits design. This paper presents and evaluates a high-performance QCA Reversible Full Adder (RFA) circuit. The developed RFA circuit is implemented in three layers using reversible gates. The functionality of the suggested RFA circuit is evaluated using QCADesigner tool. The results show that the complexity, required area, delay, and average-energy in the developed RFA circuit are 40 cells, 0.016 µm2, 0.75 clock cycles, and 1.74 meV, respectively. The comparison results demonstrate that the developed RFA circuit outperforms other RFA circuits with regard to area and costs.*

**Key words:** *QCA, Multilayer, Reversible, full adder, QCADesigner*

## 1. INTRODUCTION

Based on Moore's law, the transistors count on a chip should be double every 18 months till 2 years, but it faces some problems [1]. The CMOS technology has faced many problems including the short channel effect [2], the lithographic equipment costs [1], leakage off mode [2], high noise absorption, high power consumption, and operating frequency limitations. These problems increase in the nano dimensions. So, the researchers try to use other technologies such as Silicon On Insulator (SOI), Carbon Nano-Tube Field Effect Transistor

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(CNTFET), Single Electron Transistors (SET) [3], spintronic, molecular fragments and Quantum-dot Cellular Automaton (QCA) technology. The QCA technology is a new technology that can be considered as a suitable alternative to the CMOS technology due to significant advances in the design of` electronic circuits [4], having good energy efficiency, high density and very fast computing performance. The QCA cell is a basic element in the QCA technology, which is a square-shaped structure at nanoscale. Each cell has four quantum dots inside a square with two electrons in these dots [5].

Nowadays, the low power circuits design is an important issue in the digital circuits design. Landauer [6] show that the energy wasted for each bit of information is lost in the irreversible circuits, which is computed as follows [7, 8].

$$kTln2 \text{ (joules)} \tag{1}$$

where T and k denote the temperature and Boltzmann's constant, respectively. He also [6] showed that, if we want not to lose energy, we must prevent the loss of information. Bennett's research [9] helped to solve this problem. One approach to design the low power circuits is reversible circuits design [8].

On the other hand, full adder is one of the main blocks in the computer arithmetic. The logical expressions of the outputs of the full adder circuits are as follows [10].

$$Sum = A \oplus B \oplus C \tag{2}$$

$$Cout = (A \oplus B).C \oplus AB$$

Where Sum and Cout denote the summation and carry output, respectively. In addition A, B, and C denote the inputs.

In this paper, a new Reversible Full Adder (RFA) circuit is suggested. The suggested RFA is designed based on a new structure in three layers. The proposed multilayer RFA circuit is implemented using the QCA designer tool version 2.0.3. In addition, the QCA designer-E is employed for the energy estimation. The implementation results show that the suggested RFA circuit has 0.016 $\mu m^2$ area, and 0.75 clock cycles delay. The comparison demonstrates that the proposed RFA circuit provides advantages in comparison with other RFA circuits.

The structure of this study is as follows. The background of the QCA technology including the concepts of the QCA technology and reversibility, reversible logic gate behavior, and related works of the RFA circuits are summarized in section 2. The developed circuits are proposed in section 3. The simulation results and comparison are presented in section 4. Finally, conclusion of this paper is presented in section 5.

## 2. BACKGROUNDS

### 2.1. QCA technology

The QCA technology is a type of technology that is proposed to build electric circuits in nano dimensions. The standard semiconductive materials are used to form the nanostructures that make up the quantum dots. The quantum wells are used to simulate these structures. Even at distances several hundred times greater than the lattice constant of the material system, they display energy effects. It is also possible to visualize a dot. When an electron is caught inside a dot, it takes more energy for it to come out. This

technology provides advantages including high frequency, very low latency, high density, extremely low power usage and small footprint. Low energy dissipation occurs during the propagation and state change. Consequently, the QCA uses a remarkably small amount of power when compared to CMOS technology [2]. This technology is based on the QCA cell. Each QCA cell has a square environment and inside it includes four dots that are placed in the square corners. In addition, there are 2 free electrons that can move between dots. So, there are 2 stable states in this structure that can be utilized to indicate the binary states. As a result, it is possible to implement digital circuits in the QCA technology. There are two QCA basic gates, majority gate and inverter gate [11-14]. Figure 1 illustrates the QCA cell structure and its stable stats.

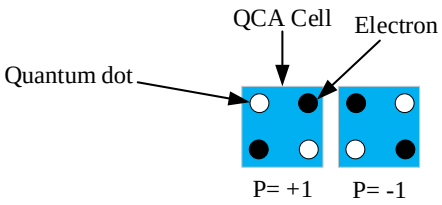



**Fig. 1** The QCA cell structure and its stable stats

### 2.2. QCA wires

The QCA wires are created from a combing structure consisting of several QCA cells arranged one behind each other due to the coulombic repulsion of the electrons of the adjacent cells, the QCA cells assume the same polarity as each other [15]. Figure 2 illustrates the QCA wires.

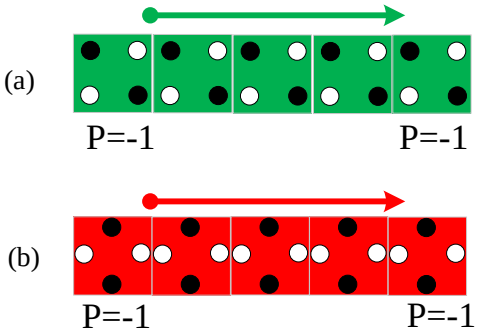



**Fig. 2** Wires in the QCA technology a) normal, b) with 450 rotations

The multilayer crossovers can effect on the circuit area in the QCA technology. It is because the wires can place in different layers. So, the wires do not collide with each other unlike the single-layer arrangement. Thus, there is more physical separation between the wires and the cells that make them up. Errors can therefore be prevented more readily than with a single layer. The multilayer QCA circuits have a more stable response as a result. To implement the multilayer crossover, at least three layers are needed. The multilayer crossover in QCA technology is illustrated in Figure 3.

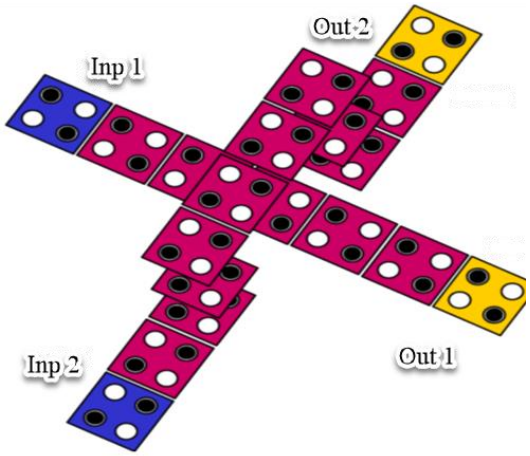



**Fig. 3** QCA multilayer crossing wire

### 2.3. QCA CLOCK

The structural features of the QCA cell cause the clock to form of electronic agents to control the movement of the electrons. It is inside the cells and the existence of the clock causes creation the synchronization takes place in different parts of the circuit. Each clock in the QCA technology has four phases, switch, hold, transition, and release [16, 17]. Figure 4 displays the QCA clock mechanism.

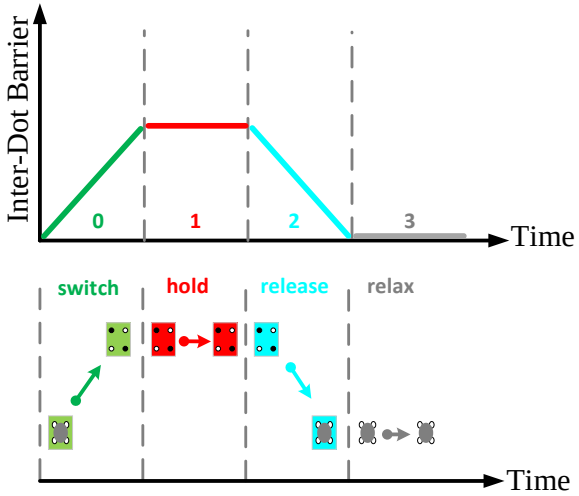



**Fig. 4** QCA clocking with four phases

In the switch phase, the cell polarization is under the influence of neighboring cells. In the hold phase, the cells are in a state of polarization electrons at the greatest distance from each

other. In this phase, cells are able to detect the polarity of adjacent cells. Electrons are progressively released throughout the release phase, and the blocking force is reduced. It is polarity-free during the relaxation phase, allowing electrons to flow freely throughout the cell [16].

### 2.4. Reversibility

A gate is called reversible if there is a one-to-one mapping between its input and output vectors. In addition, the input vector can always be formed from the output vector, and conversely, the output vector can also be formed from the input vector. In general, outputs are permutations of inputs so that all types of input modes are also present on the output modes. In reversible logic, we can never find two states among the outputs of the truth table, which has the same inputs. It is also obvious that we cannot find a case where for one input; produce two identical outputs. We do not have feedback and fan-out in these gates [18-22]**.**

### 2.5. Reversible gates

Main reversible gates are reversible NOT gate, Controlled-V and Controlled-V+ gates**,** Feynman gate, and HN gate [13, 16] that are described in this paper.

#### *2.5.1. NOT gate*

The reversible NOT gate contain one input and one output [13, 23]. Figure 5 displays this reversible gate.

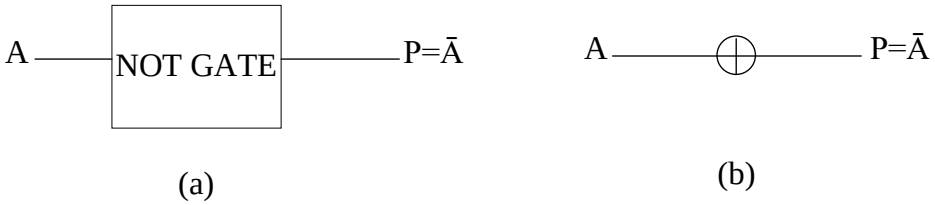



**Fig. 5** Reversible NOT gate a) logic diagram, b) quantum circuit

In this gate, the output is denoted by P, which is computed as follows.

$$P = \bar{A} \tag{3}$$

Where A and P denote input and output, respectively.

#### *2.5.2. Feynman gate*

The Feynman gate has 2 inputs and 2 outputs. It is an important reversible gate, which also called Controlled NOT (CNOT) gate [13, 24]. Figure 6 displays the Feynman gate.

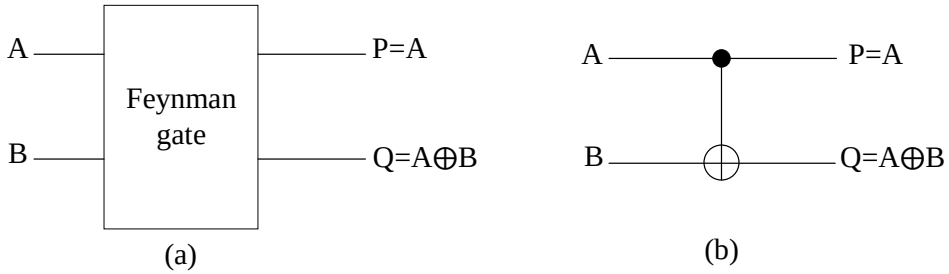



**Fig. 6** Feynman gate a) logic diagram, b) quantum circuit

The outputs of this gate are as follows.

$$Q = A \oplus B$$
$$P = A \tag{4}$$

Where Q and P denote the outputs, and B and A denote the inputs.

*2.5.3. Controlled-V and Controlled-V+*

The controlled-V and controlled-V+ gates are displayed in Figure 7.

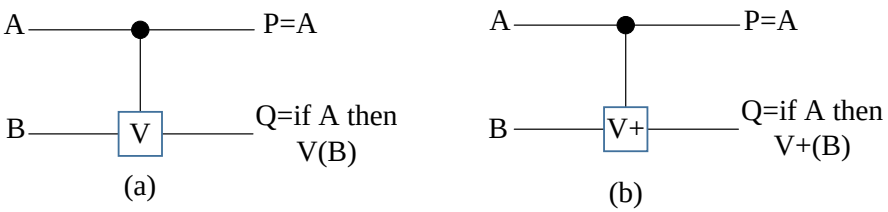



**Fig. 7** Controlled gates a) V gate, b) V+ gate

It should be noted that when two V gates are placed one after the other, the V quantum gate will function as a NOT gate. Furthermore, covered by this theorem is the fact that two V+ gates placed back-to-back result in a NOT gate. The same input is obtained by combining input V gate and input V+ gate[13, 25]. The functionally of these gates are as follows [26].

$$V \times V = NOT$$
$$V^{+} \times V^{+} = NOT \tag{5}$$
$$V \times V^{+} = V^{+} \times V = I$$

These reversible gates have two inputs and two outputs. The quantum cost of the Controlled-V, and Controlled-V+ quantum gates are QC=1.

*2.5.4. HN gate*

The HN gate has 4 inputs and 4 outputs [13, 16]. Figure 8 illustrates the HN gate.

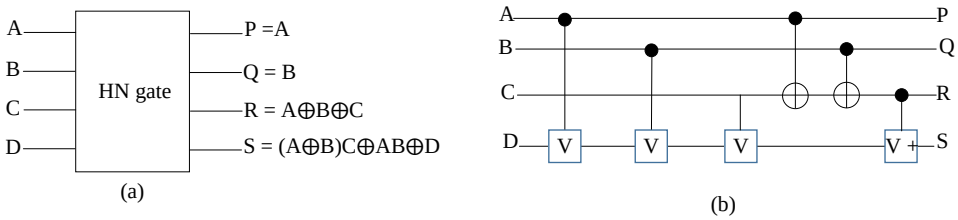



**Fig. 8** HN gate a) logic diagram b) quantum circuit

The outputs of this gate are displayed as follow [13, 16].

$$Q=B$$

$$P=A$$

$$S=(A\oplus B)\ C\oplus AB\oplus D \tag{6}$$

$$R=A\oplus B\oplus C$$

Where P, Q, R and S indicate outputs, and D, C, B, and A indicate inputs. This gate contains 3 Controlled-V gates, 2 Feynman gates, and a Controlled -V+ gate.

These reversible gates can be used to digital circuits design such as FA circuit, which is considered in this paper.

### 2.6. Related RFA works

Taherkhani et al.[27] have offered a coplanar RFA circuit that is illustrated in Figure 9.

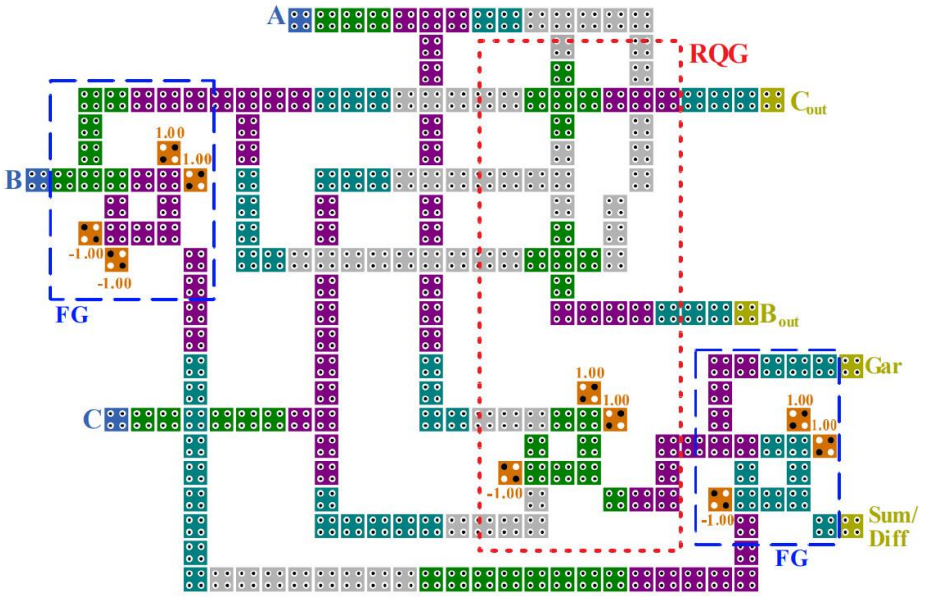



**Fig. 9** Layout of the RFA circuit in [27]

The layout of this RFA is implemented using 2 FG, and a new reversible gate that is named RQG. This circuit can be also used for subtractor. There are four inputs denoted by A, B, 0, and C, and four outputs denoted by Cout, Bout, Gar, Sum/Diff in this circuits, which are computed as follows.

$$\text{Sum} = \text{Diff} = A \oplus B \oplus C$$
$$B_{out} = MAJ(\bar{A}, B, C) = A'.B + B.C + A'.C \quad (7)$$
$$C_{out} = MAJ(A, B, C) = A.B + B.C + A.C$$

This RFA circuit requires 228 cells, 0.28 $\mu m^2$ area, and 1.75 clock cycles latency.
Jeon et al. [28] have offered an RFA circuit, which is shown in Figure 10.

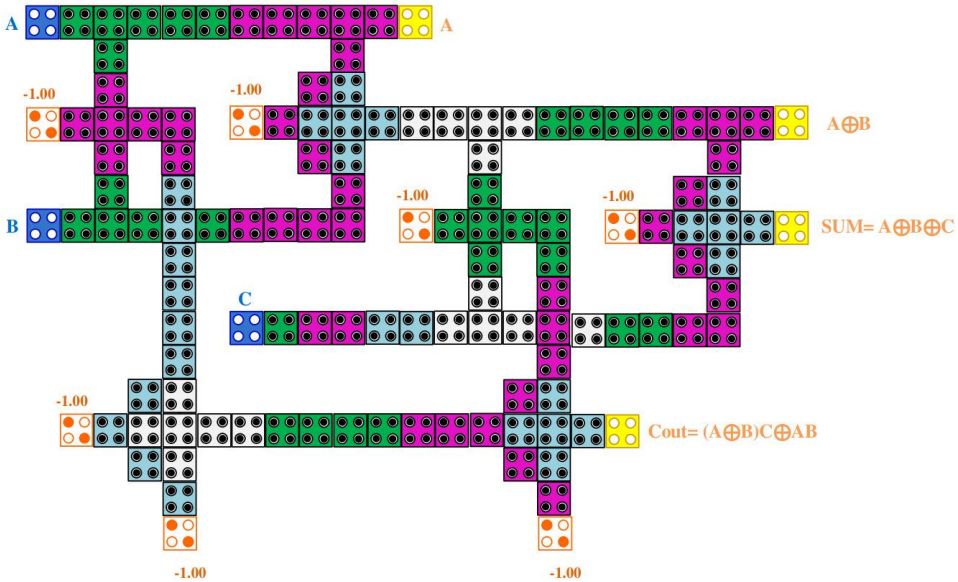



**Fig. 10** Layout of the RFA circuit in [28]

This coplanar RFA contain the Toffoli and Feynman gates. This RFA has 129 cells, 0.13 $\mu m^2$ area, and 1.75 clock cycles delay.

Sultana et al. [29] have offered a coplanar RFA circuit, which is a coplanar RFA circuit. This RFA circuit has 420 cells, 136.080 $\mu m^2$ area.

Heikalabad et al.[30] have offered an RFA circuit that is illustrated in figure 11.

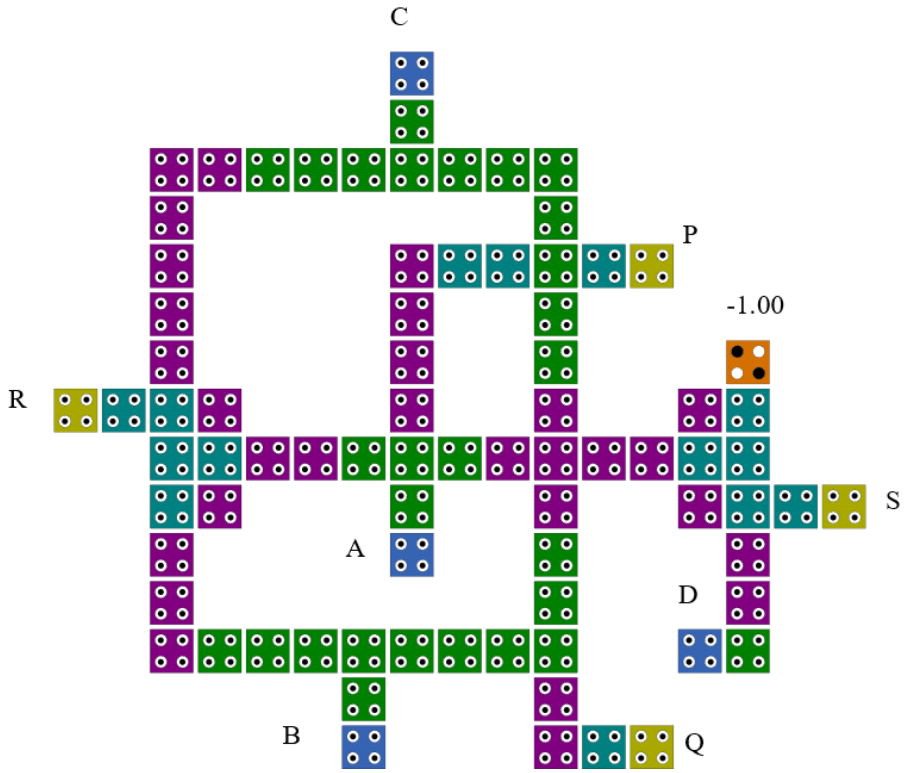



**Fig. 11** Layout of the RFA circuit in [30]

This coplanar RFA circuit has 80 cells, 0.12 μm$^2$ area, and 0.75 clock cycles delay. Aliabadian et al.[31] have offered an RFA, which is shown in Figure 12.

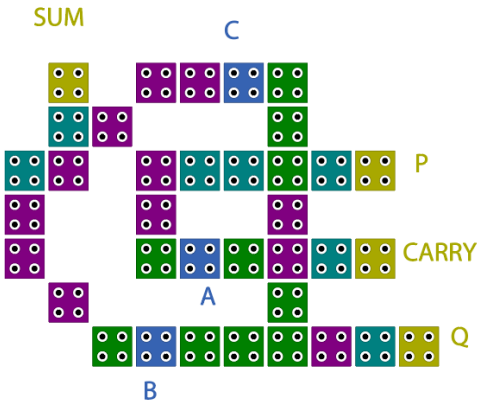



**Fig. 12** Layout of the RFA circuit in [31]

This is a coplanar circuit. It has 36 cells, 0.027 area μm$^2$, 0.75 clock cycles latency.

Although these RFA circuits provide suitable performance, the performance of the RFA circuit can be improved.

## 3. The Suggested RFA Circuit

This section proposed a new three-layer RFA circuit based on the HN gate structure. Figure 13 displays the RFA block diagram.

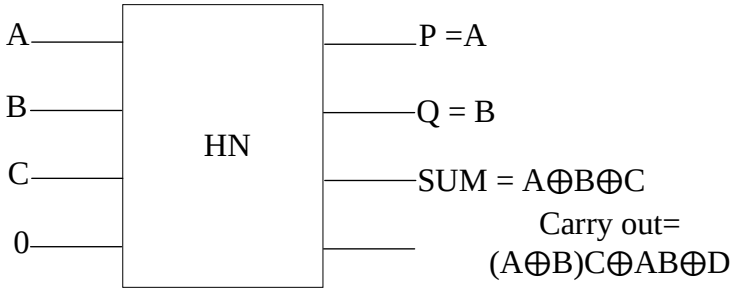



**Fig. 13** Block diagram of the proposed RFA using HN gate

The inputs in this block diagram are denoted by A, B, C, and D=0. The outputs are shown by P, Q, SUM, and Carry out that are calculated as follows.

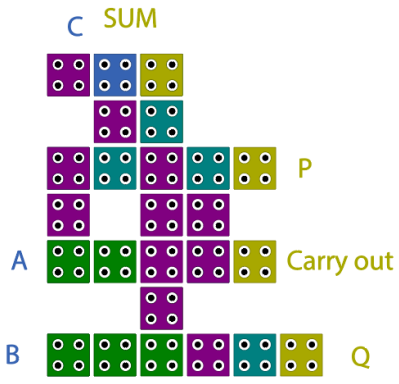
$$Q=B$$

$$P=A \tag{8}$$

$$SUM=A\oplus B\oplus C$$

$$\text{Carry out}=(A\oplus B)\,C\oplus AB$$

Figure 14 displays the developed RFA circuit based on the HN gate as building block.




(a)

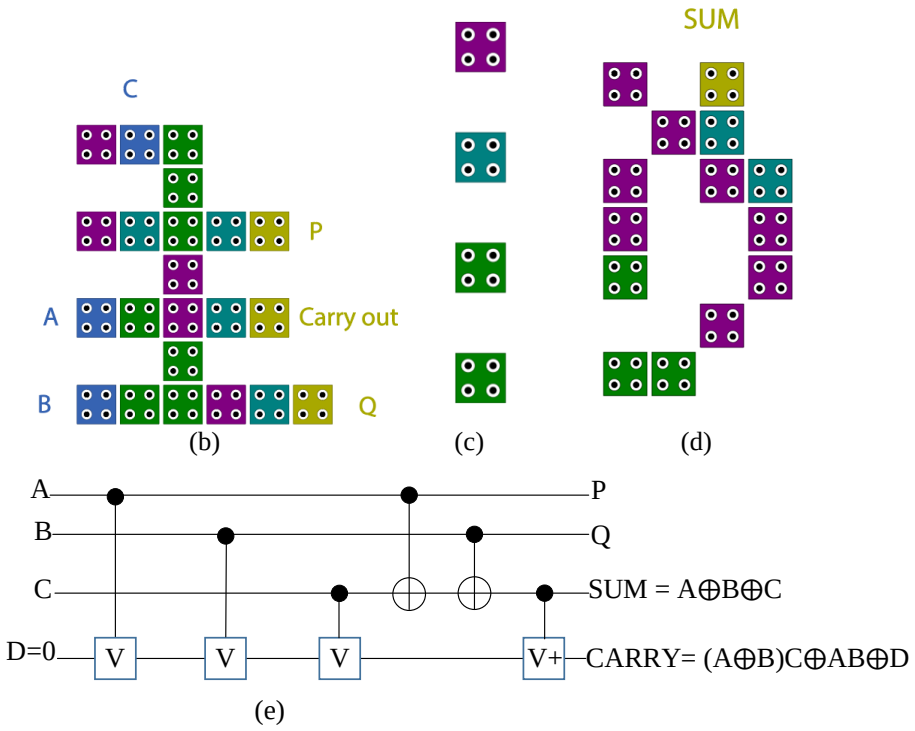



**Fig. 14** Suggested RFA a) 3 layers, b) 1st layer, c) 2nd layer, d) 3rd layer e) quantum circuit

The quantum cost of the suggested RFA circuit is QC=6. There are two garbage outputs P, Q, and a constant input in the proposed RFA circuit.

## 4. Results and Comparison

The functionality of the suggested RFA circuit is verified using the QCADesigner tool version 2.0.3. The utilized parameters for simulation are displayed in Table 1.

**Table 1** The utilized parameters

| Parameter | Value |
|---|---|
| Number of samples | 12,800 |
| Radius of effect | 65.000000 |
| Relative permittivity | 12.900000 |
| Clock shift | 0.000000e+000 |
| Clock amplitude factor | 2.000000 |
| Clock high | 9.800000E-22 |
| Clock low | 3.800000E-22 |
| Layer separation | 11.500000 |
| Convergence tolerance | 0.001000 |
| Maximum iterations per sample | 100 |

Figure 15 displays the results for the suggested RFA circuit.

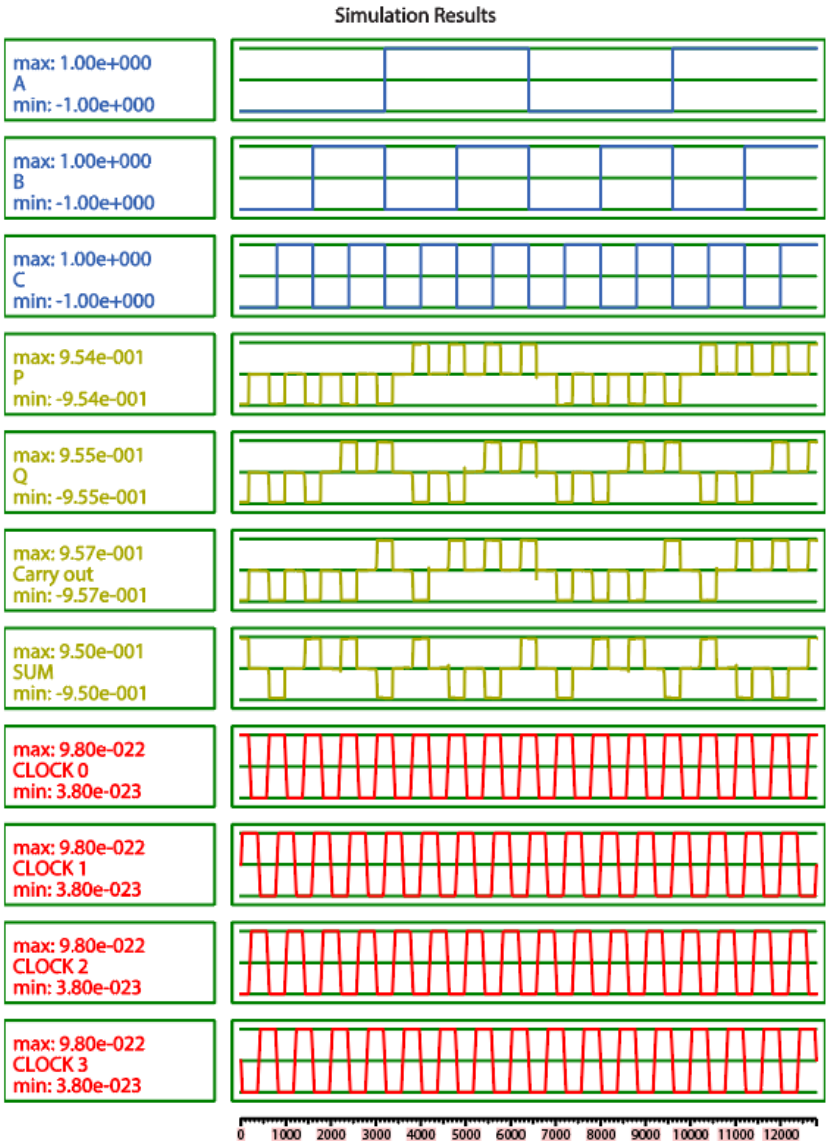



**Fig. 15** Results of the suggested RFA circuit

Based on our results that are shown in figures15, the RFA circuit are correctly worked. The latency of the developed RFA circuit is 0.75 clock cycles. Table 2 summarizes the results of the suggested RFA circuit compared to other RFA circuits.

**Table 2** The QCA RFA circuits comparisons

| Reference | COM (# of cells) | CLA ($\mu m^2$) | TLA ($\mu m^2$) | AUG (%) | LAT (Clock cycles) | CLK (Clock phases) | ADC ($\mu m^2$ ×Clock phases) | ALC ($\mu m^2$ ×Clock cycles$^2$) | cross wiring |
|---|---|---|---|---|---|---|---|---|---|
| [27] | 228 | 0.073872 | 0.28 | 26.38 | 1.75 | 7 | 13.72 | 0.49 | Single layer |
| [32] | 351 | 0.113724 | 0.41 | 27.73 | 1.50 | 6 | 14.76 | 0.615 | Single layer |
| [28] | 129 | 0.041796 | 0.13 | 32.15 | 1.75 | 7 | 6.37 | 0.2275 | Single layer |
| [29] | 420 | 0.13608 | 136.080 | 0.1 | - | - | - | - | Single layer |
| [33] | 268 | 0.086832 | 0.54 | 16.08 | - | - | - | - | Single layer |
| [16] | 80 | 0.02592 | 0.12 | 21.6 | 0.75 | 3 | 1.08 | 0.09 | Single layer |
| [31] | 36 | 0.011664 | 0.027 | 43.2 | 0.75 | 3 | 0.243 | 0.02025 | Single layer |
| [34] | 47 | 0.015228 | 0.020 | 76.14 | 1.5 | 6 | 0.72 | 0.03 | multilayer |
| [35] | 73 | 0.023652 | 0.040 | 59.13 | 0.75 | 3 | 0.36 | 0.03 | multilayer |
| This paper | 40 | 0.01296 | 0.016 | 81 | 0.75 | 3 | 0.144 | 0.012 | multilayer |

It should be noted that TLA, COM, CLA, AUG, LAT and CLK show total area, complexity or cell count, cell area, area usage, used clock cycles and used clock phases, respectively. Moreover, ALC and ADC are computed as follows.

$$ADC = Area \times Delay^2 \tag{9}$$

$$ALC = Area \times Latency \tag{10}$$

Table 3 summarizes the results of the suggested RFA circuit percentage of improvement to other RFA circuits.

**Table 3** The QCA RFA circuits percentage of improvement

| Reference | CLA ($\mu m^2$) | TLA ($\mu m^2$) | ADC ($\mu m^2$ ×Clock phases) | ALC ($\mu m^2$ ×Clock cycles$^2$) |
|---|---|---|---|---|
| [27] | 82.45% | 94.28% | 98.95% | 97.55% |
| [32] | 88.60% | 96.09% | 99.02% | 98.04% |
| [28] | 68.99% | 87.69% | 97.73% | 94.72% |
| [29] | 90.47% | 99.98% | - | - |
| [33] | 85.07% | 97.03% | - | - |
| [16] | 50% | 86.66% | 40.74% | 86.66% |
| [31] | 11.11% | 40.74% | 80% | 40.74% |
| [34] | 14.89% | 20% | 60% | 60% |
| [35] | 45.20% | 60% | 60% | 60% |

These improvements are shown in Figure 16.

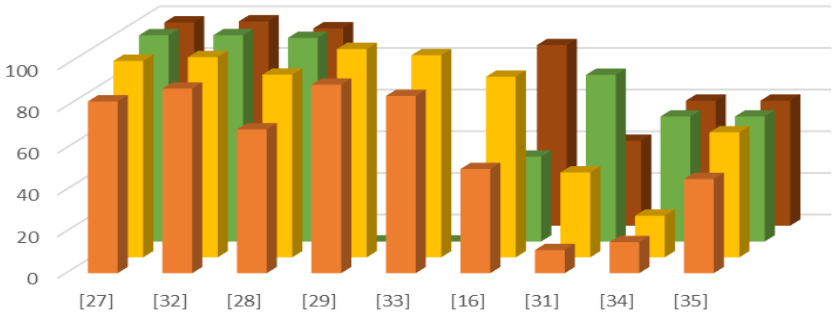



**Fig. 16** Results of the suggested RFA circuit percentage of the improvement compared to other RFA circuits

Based on the results, the suggested RFA provides advantages in comparison with previous RFA circuits in [16, 27-29, 32-35], in terms of COM, CLA, TLA, AUG, ALC, and ADC. The only RFA circuit that has slightly better results regarding CLA and COM compared to our RFA circuit, is the RFA circuit suggested in [31]. Note that our RFA has 40.74%, 46.67%, 40.74%, and 40.74% improvements in comparison with suggested RFA in [31] with regard to ALT, AUG, ALC, and ADC, respectively.

Energy analysis and estimate is a recent development in QCA circuit analysis. So, the energy is estimated for our RFA using QCADesigner-E. Table 4 displays the estimated energy for our RFA using QCADesigner-E at different temperatures.

**Table 4** Calculated energy for the suggested RFA circuit

| Temperature | Avg_Ebath (meV) | Error-Avg_Ebath (meV) | Sum_Ebath (meV) | Error-Sum_Ebath (meV) |
|---|---|---|---|---|
| 1 ◦K | 1.74 | -1.71 | 1.91 | -1.88 |
| 5 ◦K | 1.63 | -1.58 | 1.80 | -1.74 |
| 10 ◦K | 1.92 | -1.85 | 2.11 | -2.04 |
| 15 ◦K | 1.95 | -1.82 | 2.15 | -2.01 |

The estimated energy for our RFA at different temperatures is shown in figures 17 and 18.

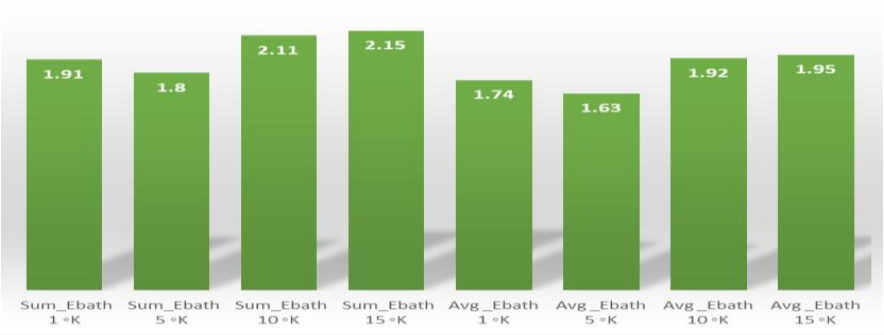



**Fig. 17** Sum and average energy of our RFA circuit for different temperatures


**Fig. 18** Error of sum and average energy of our RFA circuit for different temperatures

We contrast the calculated energy in our suggested RFA circuit with previous RFA circuits. The calculated energy for the RFA circuits at 1° K is compiled in Table 5.

**Table 5** Calculated energy for the RFA circuits

| Reference | Avg_Ebath (meV) | Error-Avg_Ebath (meV) | Sum_Ebath (meV) | Error-Sum_Ebath (meV) |
|---|---|---|---|---|
| [16] | 3.79 | -3.63 | 4.17 | -4.00 |
| [31] | 1.42 | -1.37 | 1.56 | -1.51 |
| This paper | 1.74 | -1.71 | 1.91 | -1.88 |

Based on these results, the suggested RFA outperforms the RFA suggested in [16]. Although the RFA suggested in [31] requires slightly lower energy than our RFA, our RFA has advantages with regard to ALT, ALC, AUG, and ADC in comparison with suggested work in [31].

## 5. Conclusion

The QCA technology is one exciting emerging nanotechnology. Digital circuits can be designed using this technique as an alternative to CMOS technology. Furthermore, the design of digital circuits heavily relies on the adder circuit. This paper suggested a new 3-layer RFA circuit. The design goal of this article was to improve the performance of the RFA circuit. The design strategy is use of cost-effective architecture and path planning design, which can reduce design costs such as area, ADC, and ALC. The QCADesigner tool was utilized to verify the functionality of our RFA circuit. The designed RFA circuit has 40 cells, 0.016 $\mu m^2$ area, and 0.75 clock cycles delay, according to the results. These findings also show that our RFA circuit has benefits over other RFA circuits.

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