FACTA UNIVERSITATIS
Series: **Electronics and Energetics** Vol. 37, Nº 4, December 2024, pp. 581 – 597
https://doi.org/10.2298/FUEE2404581S

Original scientific paper

EVALUATING NBTI AND HCI EFFECTS ON DEVICE RELIABILITY FOR HIGH-PERFORMANCE APPLICATIONS IN ADVANCED CMOS TECHNOLOGIES*

Karan Singh[1], Shruti Kalra[2], Jyoti Mahur[3]

[1]Department of Electronics and Communication,
Noida Institute of Engineering and Technology, Greater Noida, India
[2]Department of Electronics and Communication Engineering,
Jaypee Institute of Information Technology, Noida, India
[3]Department of Computer Science and Engineering, Noida International University,
Greater Noida, India

ORCID iDs: Karan Singh https://orcid.org/0000-0002-1452-7976
Shruti Kalra https://orcid.org/0000-0002-0609-922X
Jyoti Mahur https://orcid.org/0009-0006-0437-3383

Abstract. *The integrated circuit (IC) industry faces significant reliability challenges as MOSFET devices age, particularly at advanced nodes. Key degradation mechanisms include hot-carrier injection (HCI), negative-bias temperature instability (NBTI), and positive-bias temperature instability (PBTI), affecting both PMOS and NMOS transistors. These aging effects alter critical parameters like drain current and threshold voltage, reducing device lifespan. This paper introduces a comprehensive aging framework for MOSFETs, accounting for PBTI, NBTI, and HCI with a focus on partial recovery in AC operations at advanced technology node of 22 nm. A machine learning model enhances feature extraction, while the MOSRA approach accelerates SPICE simulations to optimize yield and reliability.*

Key words: *Threshold Voltage, MOSFET, Aging, HCI, Reliability, Temperature*

1. INTRODUCTION

The rapid advancement of semiconductor technology has fueled exponential growth in the integrated circuit (IC) industry, paving the way for increasingly powerful, compact, and energy- efficient devices. These advancements, however, come with significant challenges, primarily due to the limitations imposed by device aging on reliability, especially at advanced technology nodes like 22 nm and below. Device aging is the gradual degradation of a MOSFETs electrical properties over time, directly impacting its

Received June 29, 2024; revised September 22, 2024 and November 19, 2024; accepted November 20, 2024
Corresponding author: Karan Singh
Department of Electronics and Communication, Noida Institute of Engineering and Technology, Greater Noida, India
E-mail: vermakaransingh@gmail.com

performance and reducing the lifespan of the IC. This issue has become critical as circuit designs push the boundaries of high-performance applications, necessitating comprehensive analysis and modeling of aging mechanisms to ensure long-term reliability [1]. MOSFET aging primarily results from three dominant degradation mechanisms: Hot Carrier Injection (HCI), Negative Bias Temperature Instability (NBTI), and Positive Bias Temperature Instability (PBTI) [2]. These effects alter fundamental parameters, such as threshold voltage (Vth) and drain current, leading to a progressive decline in device performance and reliability. HCI, for instance, occurs when high-energy carriers (electrons or holes) from the channels drain end are injected into the gate insulator, gradually altering its properties. This phenomenon affects both PMOS and NMOS transistors and is especially prevalent at higher voltages and smaller node sizes, where electrical fields are intensified. NBTI and PBTI, in contrast, are primarily concerns in PMOS and NMOS transistors, respectively, and are closely associated with metal gate and high-k dielectric materials common in advanced CMOS technologies. NBTI is particularly challenging in PMOS transistors, as it leads to a threshold voltage increase when subjected to negative bias at elevated temperatures, a condition typical in many IC applications. PBTI, on the other hand, has emerged as a significant reliability issue for NMOS devices in high-k metal gate stacks, causing similar degradation under positive bias [3].

These mechanisms introduce substantial challenges in reliability modeling. The degradation they cause is not uniform but varies with stress conditions, biasing schemes, transistor geometry, and environmental factors like temperature. Furthermore, both NBTI and PBTI exhibit partial recovery when the device is in an AC (alternating current) operation, which complicates the modeling of degradation in dynamic environments. Neglecting this partial recovery effect can lead to overly pessimistic projections of circuit reliability, as the devices regain some performance when not continuously stressed [4-5]. Therefore, a robust reliability framework for high-performance applications must account for these factors to provide accurate predictions. At the advanced 22 nm node, the importance of such a framework is further heightened. Smaller node sizes increase the impact of aging effects due to the heightened sensitivity of miniature transistors to electric field stress and material degradation. Given the high-stakes applications of these circuits in computing, automotive, and communications sectors, where consistent performance and longevity are critical, accurately modeling these degradation mechanisms becomes essential. However, achieving this is complex, requiring sophisticated approaches that combine physical insights with advanced simulation techniques [6-8].

To address these challenges, this paper presents a comprehensive aging framework that integrates NBTI, PBTI, and HCI effects within the context of advanced CMOS technology nodes. By focusing on partial recovery in AC operations, this framework offers a more accurate reflection of real-world conditions, where devices are rarely subjected to constant stress. This approach also recognizes the variability in aging effects based on different operating environments, capturing the nuance needed for accurate reliability modeling in high-performance applications. Incorporating machine learning into this framework introduces an additional layer of precision by automating feature extraction processes for degradation modeling [9]. Given the complexity of device behavior under varying stress conditions, machine learning techniques can help identify patterns in aging behavior and improve the predictive accuracy of the model. By analyzing large datasets of MOSFET characteristics under different biasing, temperature, and geometric conditions, the model can recognize degradation trends and partial recovery behaviors more accurately than

traditional methods. This data-driven approach enhances the models robustness, making it better suited for high-performance applications that demand strict reliability criteria. The integration of machine learning also aligns well with the MOSRA (MOS Reliability Analysis) methodology, which is increasingly used in reliability analysis at advanced nodes. MOSRA facilitates accelerated SPICE simulations, allowing designers to model aging impacts on circuitry more efficiently. SPICE (Simulation Program with Integrated Circuit Emphasis) simulations have long been essential for circuit design, providing insight into device behavior under various conditions [10]. However, traditional SPICE models often struggle to capture the complexities introduced by NBTI, PBTI, and HCI degradation, especially in dynamic environments where partial recovery occurs. MOSRA overcomes these limitations by providing a structured approach to simulate degradation effects, enabling more accurate prediction of device reliability. This combined framework, which leverages the strengths of machine learning and MOSRA, not only enhances yield but also ensures IC reliability in demanding high-performance applications. By accurately simulating the effects of NBTI, PBTI, and HCI, the framework enables designers to optimize their circuits to withstand the aging processes that naturally occur over time. This is critical for applications like cloud computing, artificial intelligence, and telecommunications, where even minor lapses in device performance can lead to significant disruptions. Through this approach, the IC industry can better predict and mitigate the effects of MOSFET aging, ultimately supporting the continued advancement of semiconductor technology. Furthermore, this study contributes to the ongoing discourse on aging mechanisms by providing insights into the limitations of existing models [11]. Traditional aging models often assume static stress conditions, overlooking the dynamic nature of real-world environments. By incorporating the effect of partial recovery, this work not only challenges existing paradigms but also sets the foundation for more flexible and accurate reliability models. In doing so, it paves the way for a new generation of IC designs that are resilient against the inevitable degradation that comes with MOSFET aging [12-13].

2. LITERATURE SURVEY

The Table 1 presents a detailed literature survey on MOSFET aging and reliability models, highlighting critical advancements, methodologies, and limitations in reliability prediction. Starting with foundational work, Arora and Sharma (1991) introduced an empirical substrate current model, which has become a standard for circuit simulation accuracy, although it lacks adaptability to modern, smaller nodes. Following this, Tudor et al. (2012) contributed an aging model specifically suited to 28 nm technology nodes, an advancement that paved the way for more accurate IC simulation, though it struggles with scalability to smaller nodes. A pivotal study by Grasser et al. (2011) shifted the understanding of Bias Temperature Instability (BTI) by integrating BTI and Hot Carrier Injection (HCI) effects. This work enhanced reliability predictions but still requires more extensive experimental validation under diverse temperature conditions. Parihar et al. (2017) further improved BTI modeling with a specialized tool for NBTI degradation analysis, factoring in nitrogen impact and recovery kinetics, though it focuses less on HCI effects. In the same year, Pan and Paul (2017) examined degradation under temperature and voltage cycling, a crucial study for high-performance applications, though limited to low-frequency scenarios. Research by Liang et al. (2018) explored the influence of body effects

Table 1 Literature Survey on MOSFET Aging and Reliability Models

S.No.	Ref. No.	Paper Title	Year	Major Work Done	Drawbacks
1	[14]	MOSFET substrate current model for circuit simulation	1991	Proposed an empirical model for substrate current in MOSFETs, enabling improved circuit simulation accuracy	Limited accuracy for modern sub-10nm nodes; lacks fine parameter tuning for newer technologies
2	[15]	An accurate MOSFET aging model for 28 nm integrated circuit simulation	2012	Developed a MOSFET aging model suitable for IC simulation at 28 nm nodes, accounting for aging effects	Limited scalability to more advanced technology nodes; increasing complexity for smaller geometries
3	[16]	The Paradigm Shift in Understanding the Bias Temperature Instability: From Reaction Diffusion to Switching Oxide Traps	2011	Provided an integrated model for BTI and HCI effects, focusing on switching oxide traps for improved reliability in nanoscale MOSFETs	Lacks extensive experimental validation, particularly across varied temperature conditions
4	[17]	BTI analysis tool Modeling of NBTI DC, AC stress and recovery time kinetics, nitrogen impact, and EOL estimation	2017	Developed a BTI analysis tool for modeling NBTI with recovery time and end-of-life estimation	Limited focus on HCI effects; recovery parameters not optimized for varied device sizes
5	[18]	Reliability Analysis of MOSFETs under Temperature and Voltage Cycling Stress	2017	Analyzed degradation due to temperature and voltage cycling, with an emphasis on high-performance applications	Limited to low-frequency applications; lacks consideration of geometry scaling
6	[19]	Influence of body effect on sample-and-hold circuit design using negative capacitance FET	2018	Explored the body effect in sample-and-hold circuits with negative capacitance FETs, addressing reliability under various conditions	Body effect model complexity increases with reduced device sizes; limited to specific circuit designs
7	[20]	Unified Cumulative Stress Model Integrating HCI and BTI for Nanoscale MOSFETs	2020	Proposed a cumulative stress model integrating HCI and BTI degradation mechanisms for reliability predictions	Conservative model potentially underestimating device lifespan
8	[21]	Machine Learning-Assisted Aging Prediction for MOSFET Reliability	2020	Employed machine learning to predict aging under different stress conditions, enhancing accuracy	High computational requirements and reliance on large datasets; limited applicability to new architectures
9	[22]	Efficient machine learning-assisted failure analysis method for circuit-level defect prediction	2024	Developed an efficient ML-assisted method for predicting circuit-level defects, useful for early aging predictions in MOSFETs	Potential for high computational cost and limited data generalizability across technology nodes
10	[23]	A Comprehensive Overview of Reliability Assessment Strategies and Testing of Power Electronics Converters	2024	Overviewed reliability strategies for power electronics, addressing BTI and HCI impacts on device aging and converter reliability	Broad overview with limited focus on specific MOSFET failure mechanisms in advanced nodes

in negative capacitance FETs, an emerging area of study for enhanced circuit reliability, albeit with increased model complexity. Ramezani et al. (2020) developed a unified cumulative stress model that incorporates both HCI and BTI effects, providing a conservative approach to predict device lifespan, although it may underestimate longevity. Chen et al. (2020) applied machine learning to aging prediction, offering improved accuracy but at a high computational cost. More recent studies by Ghosh (2024) and Hosseinabadi et al. (2024) leverage machine learning and provide comprehensive reliability assessments for MOSFETs and power electronics, respectively. While these studies offer insights into early defect detection and testing strategies, challenges in data generalization and specific failure mechanisms persist, especially for advanced nodes.

3. Device Aging and Recovery Mechanism in MOSFETs

Device aging is a critical issue in modern MOSFET (Metal-Oxide-Semiconductor Field-Effect Transistor) technology, particularly as transistor sizes shrink to advanced technology nodes. As devices operate over time, they experience degradation in key parameters such as threshold voltage (Vth), which leads to reduced circuit performance and reliability. Two prominent mechanisms contributing to this degradation are Negative Bias Temperature Instability (NBTI) and Hot Carrier Injection (HCI) [24-25]. These mechanisms are influenced by various operating conditions, including frequency, duty cycle, and stress conditions, which together affect the longevity and stability of MOSFETs. The figure 1 illustrates the effects of duty cycle and frequency on Vth degradation in MOSFETs, providing insight into how operating conditions accelerate aging. The plot on the left shows Vth degradation changes as a function of duty cycle for different operating frequencies (0.1 Hz, 1 Hz, 10 Hz, and 1 kHz). As observed, there is a noticeable increase in degradation with higher duty cycles across all frequencies. Higher duty cycles mean that the device is subjected to stress for longer periods, exacerbating the degradation. This is particularly evident at low frequencies (e.g., 0.1 Hz), where the degradation is more severe compared to higher frequencies. At these low frequencies, the effects of NBTI are more pronounced as the device undergoes prolonged periods of stress before any recovery can take place. his results in a significant shift in Vth, indicating greater aging. On the other hand, at higher frequencies (e.g., 1 kHz), the degradation is comparatively lower, even at high duty cycles. This is due to the partial recovery effect that occurs during the rapid switching cycles. At high frequencies, the stress-recovery cycles alternate more quickly, allowing the device to recover partially between each stress period. This effect mitigates the accumulation of defects in the oxide layer and slows down the overall degradation rate. However, even with partial recovery, there is still an upward trend in Vth degradation with increased duty cycle, emphasizing the cumulative impact of prolonged stress over time. The right plot in the figure further highlights the relationship between frequency and Vth degradation for two duty cycle values, 50% and 90%. Here, we observe a clear trend where degradation decreases as the frequency increases, consistent with the findings from the left plot. At a duty cycle of 90%, the degradation is higher across all frequencies compared to the 50% duty cycle, reflecting the greater exposure to stress. However, as frequency increases, the degradation rate drops, particularly evident for the 50% duty cycle curve. This confirms that higher frequencies facilitate recovery during each cycle, effectively slowing down

the aging process. For high-duty cycle operations, the recovery effect is less effective, and thus, degradation remains at elevated levels even as frequency increases.

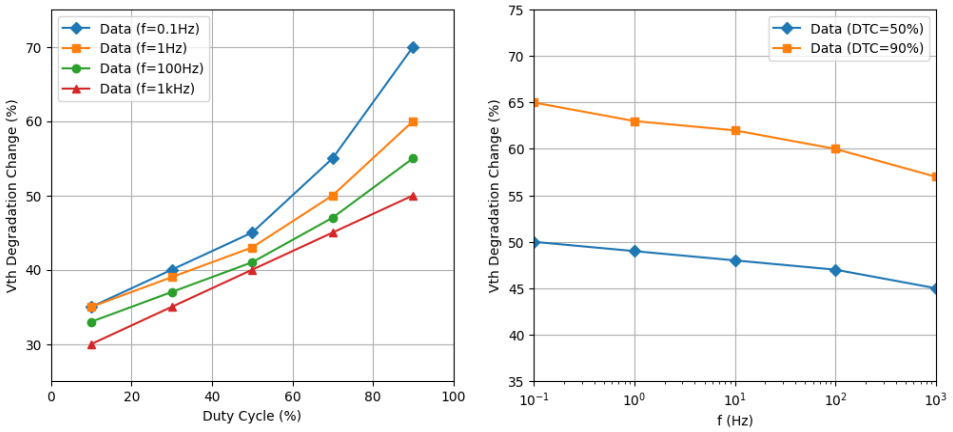

Fig. 1 ΔV_{th} deterioration vs duty cycle and frequency

The recovery mechanism is a crucial aspect of MOSFET degradation, particularly for phenomena such as Bias Temperature Instability (BTI) [26]. When a MOSFET undergoes stress due to a constant or alternating gate bias, it experiences degradation in key electrical parameters such as the threshold voltage (V_{th}) and saturation drain current ($I_{D,SAT}$). However, when the stress is removed or periodically relieved, partial recovery occurs in these parameters, slowing down the overall rate of degradation. This recovery effect is essential for accurately modeling MOSFET aging, as it provides a more realistic depiction of device behavior under actual operating conditions where devices are not continuously stressed. The figure 2 illustrates the recovery effect observed in a MOSFET under periodic stress. The top plot shows the percentage degradation in the saturation drain current, ($\Delta I_{D,SAT}$), over time. The periodic nature of degradation and recovery is evident, with ($\Delta I_{D,SAT}$) increasing during each stress phase and partially recovering during the unstressed intervals.

This pattern of degradation and recovery indicates that the MOSFET experiences a reduction in I_D, sat when subjected to stress, but this reduction does not fully persist when the stress is removed. Instead, a partial recovery occurs, reducing the cumulative degradation impact on the device. The bottom plot in the figure shows the gate-to-source voltage, V_{gs} applied to the MOSFET as a function of time. The alternating voltage pattern highlights that the device is under stress when V_{gs} is negative, while it undergoes recovery when V_{gs} returns to zero or positive values. During each stress period, carriers are trapped in the oxide layer, leading to degradation in $I_{D,SAT}$ and other electrical parameters. However, when the stress is relieved, some of these trapped carriers are released, allowing the device to partially recover. This release of trapped carriers restores a portion of the MOSFET's initial electrical characteristics, illustrating the cyclical nature of degradation and recovery. Mathematically, this recovery phenomenon can be represented by introducing a recovery term in the degradation model. For example, the total degradation in $I_{D,SAT}$ due to BTI can be expressed as [26]:

$$\Delta I_{D,sat}(\mathrm{t}) = \Delta I_{D,sat,stress},(\mathrm{t}) - \Delta I_{D,sat,recovery}(\mathrm{t}) \tag{1}$$

where $\Delta I_{\mathrm{D,\ sat,\ stress}}$ (t) represents the degradation due to stress, and $\Delta I_{\mathrm{D,\ sat,\ recovery}}$ (t) represents the partial recovery during the unstressed intervals. The recovery term is typically modeled as a time-dependent decay function, capturing the gradual release of trapped charges as follows:

$$\Delta I_{D,sat,recovery}(\mathrm{t}) = B * t^{-r} \tag{2}$$

where B and r are fitting parameters that depend on the device material and structure. The negative exponent r reflects the gradual nature of the recovery process, where a significant portion of the trapped charges are released shortly after the stress is removed, with diminishing recovery over longer periods. The recovery effect is highly dependent on the frequency and duty cycle of the applied V_{gs} waveform. Higher frequencies lead to more frequent stress-relief cycles, allowing the device to undergo recovery more often. This frequent recovery helps mitigate the cumulative degradation impact, resulting in a slower overall degradation rate. Conversely, a high duty cycle (i.e., longer periods of stress relative to recovery) reduces the effectiveness of recovery, as the device remains under stress for extended periods, leading to greater cumulative degradation.

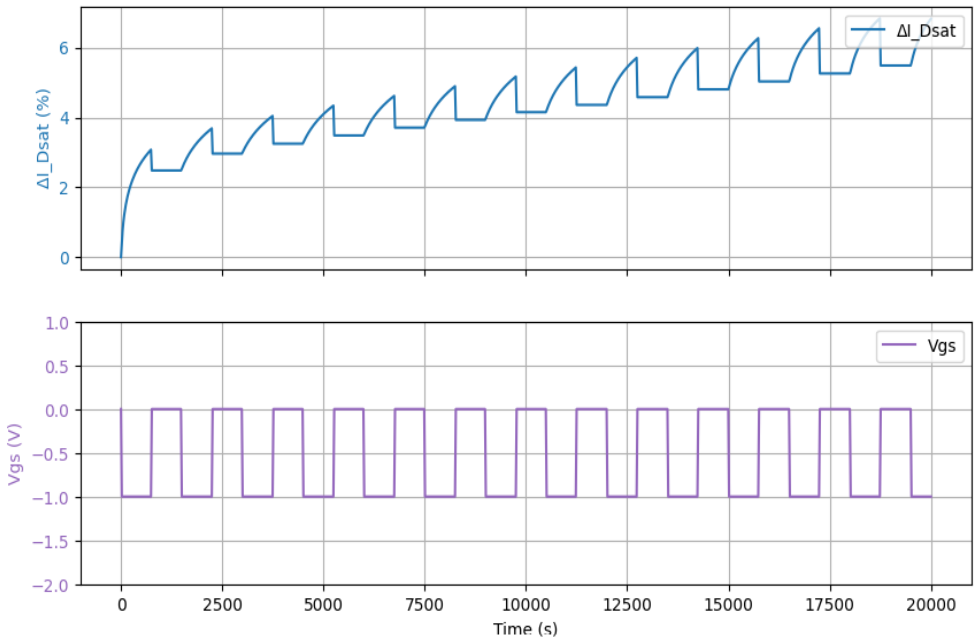

Fig. 2 $I_{\mathrm{D,SAT}}$ deterioration during Stress and Recovery Phase

4. BTI AND HCI MODELS

Bias Temperature Instability (BTI) and Hot Carrier Injection (HCI) are two major degradation mechanisms that significantly impact the reliability and performance of MOSFET devices, especially as technology scales down to nanometer nodes. Understanding the mathematical models for BTI and HCI is crucial for accurately predicting device aging and optimizing design for reliability [27].

4.1. Bias Temperature Instability (BTI) Model

BTI is a phenomenon that primarily affects the threshold voltage (Vth) of MOSFETs, leading to a gradual increase in Vth over time. BTI can be divided into two types: Negative Bias Temperature Instability (NBTI), which affects PMOS transistors under negative gate bias, and Positive Bias Temperature Instability (PBTI), which affects NMOS transistors under positive gate bias. The degradation due to BTI is influenced by factors such as gate bias, temperature, and time. The degradation in threshold voltage due to BTI, denoted as $\Delta V_{th,BTI}$, can be modeled using a power- law time dependence as follows [27]:

$$\Delta V_{th,\mathrm{BTI}}(\mathrm{t}) = A * (V_{gs} - V_{th})^{n} * exp(\frac{-E_a}{kT}) * t^{p} \tag{3}$$

where:
A is a fitting parameter that depends on the material properties and device characteristics.
V_{gs} is the gate-to-source voltage.
V_{th} is the threshold voltage of the MOSFET.
n is a parameter that represents the voltage dependency of the BTI effect.
E_a is the activation energy of the BTI process.
k is the Boltzmann constant.
T is the temperature in Kelvin.
t is the stress time.
p is the time exponent, typically between 0.2 and 0.3 for BTI in advanced technology nodes.

This model indicates that $\Delta V_{th,BTI}$ increases with higher gate voltage, elevated temperature, and longer stress time. The exponential dependence on T reflects the thermally activated nature of the BTI mechanism. In practice, BTI degradation is not entirely permanent. When the stress is removed (e.g., the device is switched off), a portion of the degradation recovers over time. This recovery effect can be modeled by introducing a recovery term, $\Delta V_{th,rec}$, which decays with time as follows [27]:

$$\Delta V_{\mathrm{th},rec}(\mathrm{t}) = B * t^{-r} \tag{4}$$

where B and r are fitting parameters. The total BTI degradation can then be modeled as a combination of stress-induced degradation and recovery:

$$\Delta V_{th,\mathrm{BTI,total}} = \Delta V_{th,\mathrm{BTI}} - \Delta V_{th,rec} \tag{5}$$

4.2. Hot Carrier Injection (HCI) Model

HCI is another degradation mechanism that affects both NMOS and PMOS transistors, though it is more pronounced in NMOS devices. HCI occurs when high-energy carriers (electrons or holes) are injected into the gate oxide from the channel, causing damage to the

oxide interface and leading to shifts in threshold voltage and other device parameters. The threshold voltage degradation due to HCI, denoted as $\Delta V_{th,HCl}$, can be modeled as:

$$\Delta V_{th,HCl}(\mathrm{t}) = C * (V_{ds} - V_{th})^{m} * (I_{d})^{q} exp(\frac{-E_i}{kT}) * t^{r} \quad (6)$$

where:
C is a fitting constant based on device characteristics.
V_{ds} is the drain-to-source voltage.
I_d is the drain current, which depends on the channel current and influences the carrier energy in the channel.
m and q are empirical parameters that describe the dependency on voltage and current.
E_i is the activation energy associated with HCI.
k is the Boltzmann constant.
T is the temperature in Kelvin.
r is the time exponent for HCI, typically ranging from 0.3 to 0.6.

The HCI effect increases with higher drain-to-source voltage, as well as higher drain current, since both contribute to generating high-energy carriers capable of causing damage to the oxide interface. Similar to BTI, HCI degradation also has a time dependence, with a power-law relation. While the degradation due to HCI is often considered less recoverable than BTI, partial recovery can still occur under certain conditions, particularly when the device is operated at lower voltages or temperatures. However, this recovery effect is less significant for HCI and is often neglected in long-term reliability modeling.

4.3. Combined Model for BTI and HCI Degradation

In advanced technology nodes, MOSFETs are subject to both BTI and HCI degradation mechanisms simultaneously. The total threshold voltage degradation, $\Delta V_{th,total}$, can thus be represented as the sum of BTI and HCI degradation components:

$$\Delta V_{th,\mathrm{total}} = \Delta V_{th,\mathrm{BTI,total}} + \Delta V_{th,HCl} \quad (7)$$

where $\Delta V_{th,BTI,\ total}$ includes both the stress-induced degradation and recovery term, and $\Delta V_{th,HCl}$ represents the degradation due to hot carrier injection. To accurately model the degradation in high-performance applications, it is crucial to capture the dynamic nature of these mechanisms, including the impact of operating conditions such as duty cycle, frequency, and temperature. For instance, higher duty cycles and operating frequencies can lead to faster accumulation of damage due to increased exposure to stress cycles, while elevated temperatures accelerate both BTI and HCI degradation due to their thermally activated nature.

5. Proposed Model

5.1. Modified Lifespan Model for MOSFET Aging

The original lifespan model presented in [28] contains three distinct terms that account for the dependencies on drain voltage, substrate current, and drain current. However, in practice, separating these parameters for accurate reliability predictions is challenging. To

address this, we propose an altered model that retains essential bias dependencies while merging two of the original terms. This modified model is represented as:

$$\Delta V_{th,HCl} \sim \left[\mathrm{THCl1} * \left(\frac{I_{ds}}{W_{eff}} \right)^{TDCE} * \left(\frac{I_{sub,i}}{I_{ds}} \right)^{TDII} + THCl2 * V_{ds}^{TDVD} * \left(\frac{I_{ds}}{W_{eff}} \right)^{TDID} \right] * t^{HN} \quad (8)$$

In this model, the LEM terms parameters are represented by TDCE and TDII, while TDVD and TDID define the bias dependencies in the elevated current regime. THCI2 captures the high current domain, while THCI1 corresponds to moderate and low drain current phases (consistent with LEM paradigms). HN denotes the stress time exponent for HCI. This formulation makes the model suitable for nanoscale technologies by covering a range of operating points, as illustrated in figure 3. The figure illustrates the contributions of two terms in the modified lifespan model for MOSFET aging: the first term (dashed blue line) represents the LEM (Long-term Electromigration) component, capturing moderate and low drain current phases, while the second term (green dashed line) reflects the elevated current regimes impact. The combined model (solid red line) integrates both terms, demonstrating a more comprehensive representation of threshold voltage degradation (ΔV_{th}) with increasing gate-to-source voltage (V_{gs}). As V_{gs} increases, the combined model exhibits a higher degradation rate, accurately reflecting the cumulative effect of both moderate and high current stress phases.

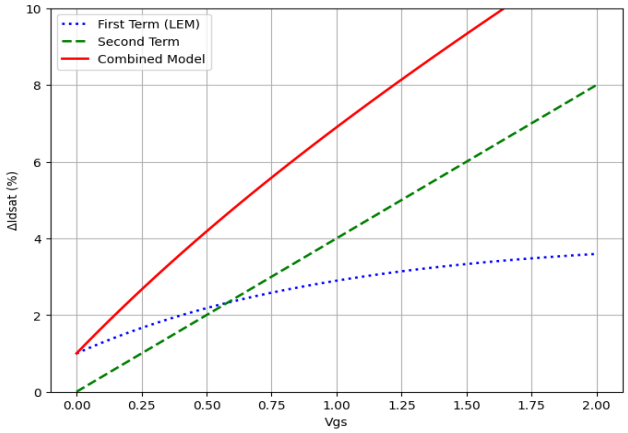

Fig. 3 I_{dsat} HCI deterioration vs V_{gs}

5.2. Enhanced HCI Model for Predicting Substrate Current in MOSFETs

For an accurate representation of Hot Carrier Injection (HCI) effects, a detailed model that incorporates the ionization impact on substrate current is essential. The conventional compact models, such as BSIM4, provide a baseline approximation of impact ionization-induced substrate current but lack precision in certain operational regions, particularly within the saturation zone of the MOSFET. To address this limitation, a predictive MOS Reliability Analysis (MOSRA) HCI model is introduced, as illustrated in figure 4. This model enhances accuracy in the saturation region by better capturing the behavior of substrate current under HCI stress, compared to traditional models. In the figure, the substrate current (I_{sub}) is plotted

against the gate voltage (V_g), with the MOSRA HCI model and BSIM4 model predictions shown alongside experimental data (represented by purple dots). The MOSRA model (solid lines) demonstrates improved alignment with the experimental data across different voltage levels, particularly in the saturation region, where BSIM4 (dashed lines) deviates more significantly. Each colored line in the figure corresponds to substrate current predictions at varying HCI stress levels, illustrating the MOSRA model's enhanced sensitivity to these changes. The red curve indicates the highest stress, while the other curves (green, orange) correspond to progressively lower stress levels. This improved accuracy is achieved by incorporating a more detailed treatment of impact ionization effects. In MOSFETs, impact ionization occurs when high energy carriers in the channel gain sufficient kinetic energy under strong electric fields (as in the saturation region) to generate electron-hole pairs through collisions with the lattice. The holes generated by this ionization process contribute to the substrate current, I_{sub}, which serves as an indicator of the extent of HCI-induced degradation. The MOSRA model's equation for substrate current in the presence of HCI stress can thus be expressed with a greater degree of accuracy, allowing it to predict degradation effects more precisely. By integrating both HCI and ionization effects, the model effectively combines the benefits of compact models like BSIM4 with additional precision tailored to advanced technologies. This integration makes the MOSRA model more applicable for nanoscale devices, where accurate substrate current prediction is critical for ensuring device reliability.

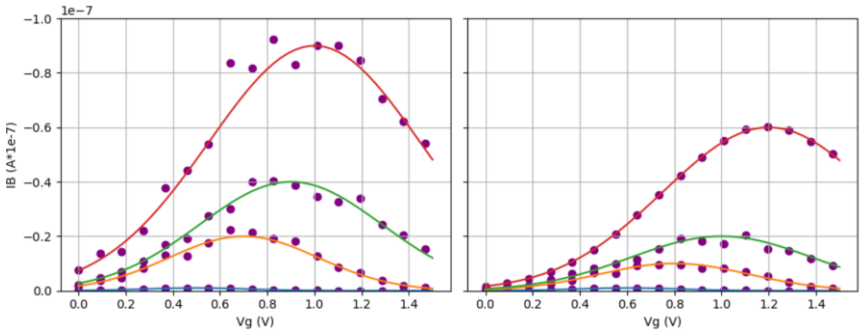

Fig. 4 I_{sub} vs V_g of BSIM4 model without and with the HCI impact ionization

6. Estimation of Deterioration Modeling Parameters

Accurately estimating deterioration parameters for Hot Carrier Injection (HCI) and Bias Temperature Instability (BTI) is essential for reliable aging modeling in MOSFET devices. Typically, HCI and BTI data are collected under accelerated stress conditions with larger bias voltages than conventional circuit operation. This process involves collecting data from multiple identical devices, each tested at different temperatures and bias levels to capture variability in device degradation. Particularly in BTI characterization, this procedure is time-consuming, as it requires "on-the-fly" tests to minimize recovery during measurements. Full sets of degraded I-V curves are rare, and available measurement data often consist only of threshold voltage shifts (ΔV_{th}), saturation current (I_{dsat}), and/or sub-threshold leakage current. Estimating degradation across the entire bias range becomes challenging, especially for sub-threshold leakage and other low current regions. To address variability, it is crucial to analyze "fresh" data obtained before stress is applied. This initial data accounts for natural variations

across devices, allowing a baseline for comparison. However, measurements taken under low-stress bias and short operational periods can be noisy, with potential errors comparable to actual degradation values, particularly for subthreshold currents. This noise can obscure early degradation signals, complicating accurate parameter estimation. The parameter extraction process involves three main stages, beginning with the recovery-related parameters of the BTI model. In the first step, parameters that exclusively affect BTI recovery are identified. Next, with the BTI parameters established, the HCI model parameters are extracted. Finally, using both BTI and HCI parameters, the parameters associated with recovery effects are determined. Each stage requires refinement of the parameter set to achieve accuracy, accomplished through a systematic optimization loop. As illustrated in figure 5, the process begins with an initial set of parameters. The aging simulation is conducted using HSPICE, with the simulation conditions matching the stress bias and time intervals in the experimental data. The simulator extracts key device characteristics, such as threshold voltage (ΔV_{th}), saturation current (I_{dsat}), and mobility, across various stress conditions. An error function then compares simulated values with measured data to evaluate the accuracy of the current parameter set. In each optimization cycle, the parameter set is iteratively adjusted to minimize the error function. This iterative process continues until the error function reaches an acceptable threshold, indicating a close match between simulated and experimental results. The optimization cycle focuses on specific deterioration factors, such as threshold voltage shift and mobility degradation. Initially, parameters related to degradation in the linear region, such as V_{th} and mobility, are tuned. Subsequently, saturation characteristics, including saturation velocity and Drain-Induced Barrier Lowering (DIBL), are adjusted. Finally, geometry scaling parameters are refined to account for device size effects.

The process is computationally intensive, as it requires consideration of multiple stress biases, temperatures, and time intervals. The early stages of parameter tuning often demand significant computational resources due to the range of conditions being evaluated. However, the systematic optimization loop ensures that all relevant factors are accounted for, enabling precise parameter estimation that reflects real-world operating conditions.

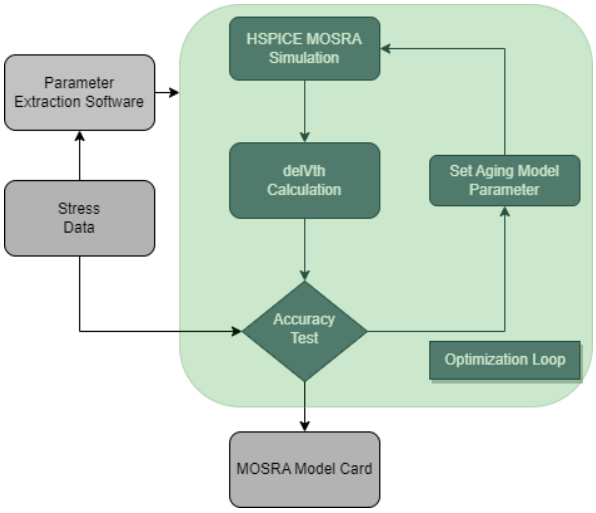

Fig. 5 MOSRA Parameter Optimization

7. AGING MODELS IN THE MOSRA FLOW

The MOSRA (MOS Reliability Analysis) flow has been developed to incorporate aging models for Bias Temperature Instability (BTI) and Hot Carrier Injection (HCI) into HSPICE and HSIM simulators. This flow is built on a unified engine capable of handling both regular non-aging simulations and aging calculations, ensuring efficient data transfer between these two modes. The term end of life (EOL), as depicted in figure 6, refers to the point in the MOSFET's operational lifespan where a critical performance parameter (such as threshold voltage or saturation current) decreases by a predefined percentage (typically 10%) from its initial value.

7.1. MOSRA Flow Overview

The MOSRA flow is divided into two main phases: pre-stress and post-stress. These phases can either be conducted individually or within a single simulation run, depending on the requirements of the analysis. In the pre-stress (or fresh) phase, simulations are run with no prior aging impact, while the post-stress phase includes accumulated aging effects over time.

7.2. Pre-stress Simulation

The pre-stress simulation phase involves running a fresh simulation, where the MOSRA aging models calculate the voltage stress on user-defined MOSFETs within the circuit. This stress analysis is based on each device's electrical specifications, as illustrated in Fig. 6. During transient analysis, various stress values derived from the Synopsys MOSRA model are applied over different stress periods. After a defined operational time, the results are extrapolated to estimate the overall degradation of each targeted device. During this phase, MOSRA uses an API (Application Programming Interface) to allow custom-based models to be incorporated if needed. This flexibility supports precise analysis by letting users adjust the model based on specific device characteristics or novel aging effects not captured by default models. The data obtained here serves as a baseline, helping to understand how devices behave under initial, stress-free conditions and identifying the early degradation trend.

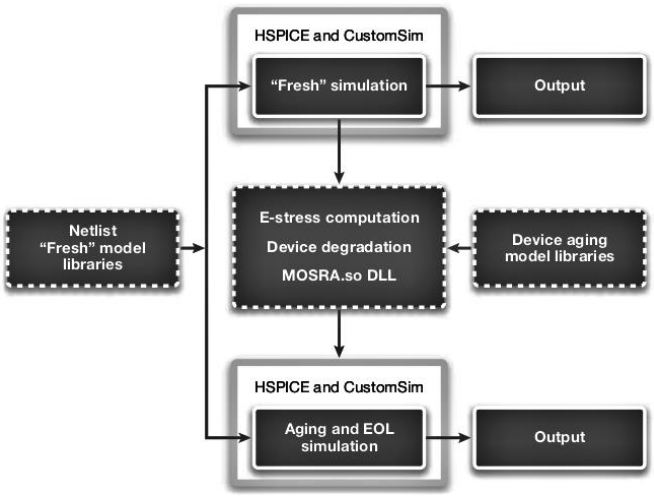

Fig. 6 The MOSRA Flow

7.3. Post-stress Simulation

In the post-stress simulation phase, the accumulated degradation from BTI, HCI, and other aging mechanisms is incorporated to simulate the circuit's behavior under long-term stress. Different types of analysis transient, DC, or AC can be applied during this phase, depending on the circuit's operational requirements. This phase assesses the circuit-level degradation against specified reliability standards, providing insights into how aging impacts the circuits performance over time. An example of this degradation is illustrated in figure 7, which shows frequency decay over time in a ring oscillator circuit. Two scenarios are depicted: one with partial BTI recovery (solid line) and another without it (dashed line). Partial recovery refers to the device's natural tendency to regain some of its performance when stress is relieved temporarily, as often happens with BTI. When partial recovery is ignored, the frequency degradation is overstated, leading to a pessimistic

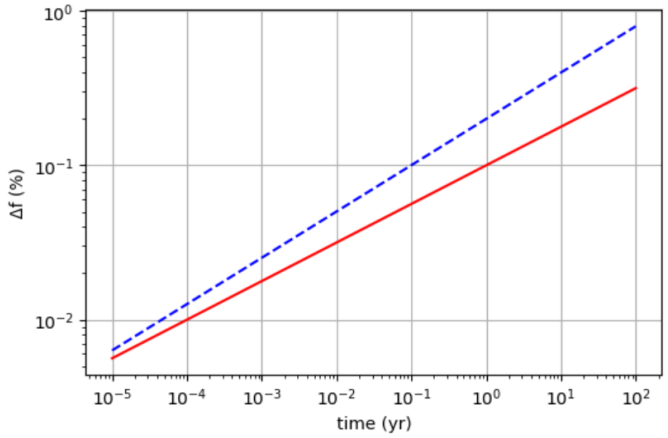

Fig. 7 Ring Oscillator frequency deterioration without (dashed line), and with partial recovery (solid line)

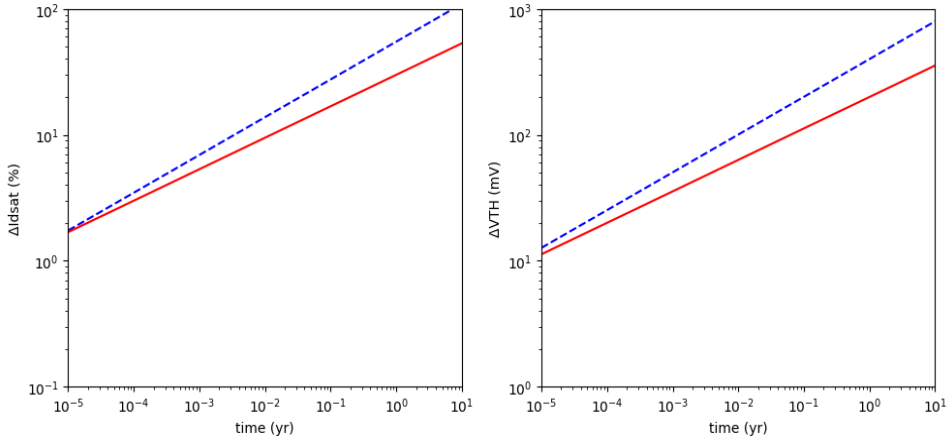

Fig. 8 The effect of accumulated stress on I_{dsat} and on V_{TH}

estimation of the circuit's lifespan. Thus, accounting for recovery effects is essential for realistic modeling, as it prevents unnecessary conservatism in the reliability analysis.

7.4. Optimization and Cumulative Stress

The MOSRA flow incorporates an optimization loop to refine the accuracy of aging models. Parameters are initially set and then iteratively adjusted to minimize the error between simulated results and experimental measurements. For instance, pre-stress simulations may involve adjusting parameters associated with threshold voltage shifts (ΔV_{th}), saturation current (I_{dsat}), and mobility in the linear region. Following this, saturation region characteristics such as saturation velocity and Drain-Induced Barrier Lowering (DIBL) are fine-tuned. Lastly, geometry scaling adjustments are applied to capture the impact of device dimensions on aging behavior. The cumulative effect of stress is another critical consideration in the MOSRA flow. As shown in figure 8, the aging models account for the continuous accumulation of stress over different periods, avoiding the need for empirical adjustments. Each MOSRA analysis inherently includes deterioration data from previous phases, creating a holistic approach to aging. Ignoring this cumulative effect would lead to an overestimation of degradation, as evidenced by the divergence between actual and predicted values over extended simulation periods. figure 6 highlights how disregarding cumulative stress impacts can significantly overstate deterioration, especially as the simulation period extends.

7.5. Benefits of the MOSRA Flow

The MOSRA flows integration of HCI and BTI models enables a comprehensive approach to MOSFET aging analysis in high-performance circuits. By maintaining continuity between pre-stress and post-stress phases, it captures the progressive impact of degradation and offers flexibility to simulate under various stress biases, time intervals, and temperature conditions. Additionally, the ability to include partial recovery effects and cumulative stress over time results in more realistic lifespan predictions for nanoscale devices.

8. CONCLUSION

The integration of Bias Temperature Instability (BTI) and Hot Carrier Injection (HCI) models into advanced simulation flows, like MOSRA, is essential for accurate reliability predictions in high-performance MOSFET applications. These models account for complex aging mechanisms, particularly relevant at nanoscale nodes where device degradation impacts both performance and lifespan. By simulating both degradation and partial recovery effects under varied operating conditions, MOSRA enables more realistic assessments of IC durability. This comprehensive modeling approach, enhanced with machine learning techniques, supports the semiconductor industry's ongoing advancement by providing robust tools for circuit longevity and reliability in dynamic environments.

REFERENCES

[1] H. Zhang, X. Shi, R. Huang, et al., "Semiconductor memory roadmap: advances in semiconductor memory", *IEEE Access*, vol. 8, pp. 137566–137590, 2020.

[2] A. Das, X. Wang, C. Hsieh, et al., "Unified aging model of NBTI and HCI degradation towards lifetime prediction for FinFETs at advanced technology nodes", *IEEE Trans. Electron Devices*, vol. 70, no. 1, pp. 15–22, 2023.

[3] A. Crespo, F. Sanchez, and D. Morente, "Impact of Hot Carrier Injection (HCI) on the reliability of CMOS inverters", *IEEE Trans. Device Mater. Reliab.*, vol. 21, no. 2, pp. 55–64, 2021.

[4] N. Goel and S. Mahapatra, *Fundamentals of Bias Temperature Instability in MOS Transistors: Characterization Methods, Process and Materials Impact, DC and AC Modeling*. Springer, 2022, pp. 209–263.

[5] H. Gupta, Y. Wang, and H. Lin, "Reliability-Conscious MOSFET Compact Modeling with Focus on the Defect-Screening Effect of Hot-Carrier Injection", in *Proceedings of the IEEE Conference Publications*, 2022, pp. 131–138.

[6] A. Das and T. Mogami, "An Accurate and Scalable MOSFET Aging Model for Circuit Simulation", *IEEE Trans. Device Mater. Reliab.*, vol. 22, no. 4, pp. 390–396, 2021.

[7] Fraunhofer IIS/EAS, "White Paper: Circuit Level Aging Simulations", Fraunhofer Institute for Integrated Circuits, 2023. (Available: www.eas.iis.fraunhofer.de).

[8] S. Reddy and J. Liu, "Reliability Challenges in FinFETs", Springer, 2021, pp. 123-139. (Available: www.springerlink.com).

[9] S. Mahapatra, N. Goel, and A. Islam, "Fundamentals of Bias Temperature Instability in MOS Transistors: Characterization Methods, Process and Materials Impact, DC and AC Modeling", in *Fundamentals of Bias Temperature Instability in MOS Transistors*, Springer, 2022, pp. 209–263.

[10] H. Gupta, Y. Wang, and H. Lin, "Reliability-Conscious MOSFET Compact Modeling with Focus on the Defect-Screening Effect of Hot-Carrier Injection", in *Proceedings of the IEEE Conference Publications*, 2022, pp. 131–138.

[11] A. Das and T. Mogami, "An Accurate and Scalable MOSFET Aging Model for Circuit Simulation", *IEEE Trans. Device Mater. Reliab.*, vol. 22, no. 4, pp. 390–396, 2021.

[12] L. Chen and M. Tahoori, "MOSRA: An efficient and versatile MOS aging modeling and reliability analysis solution for 45 nm and below", in *Proceedings of the IEEE Conference Publications*, 2011, pp. 1–5.

[13] A. Torres-Jacome and E. Tlelo-Cuautle, "On the Prediction of the Threshold Voltage Degradation in CMOS Technology Due to Bias-Temperature Instability", *Electronics*, vol. 7, no. 12, pp. 427–435, 2018.

[14] N.D. Arora and M.S. Sharma, "MOSFET substrate current model for circuit simulation", *IEEE Trans. Electron Devices*, vol. 38, no. 6, pp. 1392–1398, 1991.

[15] B. Tudor, J. Wang, Z. Chen, R. Tan, W. Liu, F. Lee, "An accurate MOSFET aging model for 28 nm integrated circuit simulation", *Microelectronics Reliability*, vol. 52, no. 8, pp. 1565–1570, 2012.

[16] T. Grasser, H. Reisinger, B. Kaczer, W. Goes, H. Reisinger, T. Aichinger, P. Hehenberger, P.J. Wagner, F. Schanovsky, J. Franco, M. T. Luque, and M. Nelhiebel, "The Paradigm Shift in Understanding the Bias Temperature Instability: From Reaction-Diffusion to Switching Oxide Traps", *IEEE Trans. Electron Devices*, vol. 58, no. 11, pp. 3652–3666, 2011.

[17] N. Parihar, N. Goel, S. Mukhopadhyay, and S. Mahapatra, "BTI analysis tool: Modeling of NBTI DC, AC stress and recovery time kinetics, nitrogen impact, and EOL estimation", *IEEE Trans. Electron Devices*, vol. 65, no. 2, pp. 392–403, 2017.

[18] C. Pan and S. Paul, "Reliability Analysis of MOSFETs under Temperature and Voltage Cycling Stress", *Microelectronics Reliability*, vol. 76, pp. 29–38, 2017.

[19] Y. Liang, X. Li, S. George, S. Srinivasa, Z. Zhu, S. K Gupta, S. Datta, V. Narayanan, "Influence of body effect on sample-and-hold circuit design using negative capacitance FET", *IEEE Trans. Electron Devices*, vol. 65, no. 9, pp. 3909–3914, 2018.

[20] H. Ramezani, S. Alavi, and M. Niakan, "Unified Cumulative Stress Model Integrating HCI and BTI for Nanoscale MOSFETs", *Solid-State Electronics*, vol. 174, p. 107863, 2020.

[21] Y. Chen, Z. Li, and J. Zhou, "Machine Learning-Assisted Aging Prediction for MOSFET Reliability", *IEEE Trans. Device Mater. Reliab.*, vol. 20, no. 4, pp. 500–508, 2020.

[22] J. Ghosh, "Efficient machine learning-assisted failure analysis method for circuit-level defect prediction", *Machine Learning with Applications*, vol. 16, p. 100537, 2024.

[23] F. Hosseinabadi, S. Chakraborty, S.K. Bhoi, G. Prochart, D. Hrvanovic, O. Hegazy, "A Comprehensive Overview of Reliability Assessment Strategies and Testing of Power Electronics Converters", *IEEE Open J. Power Electron.*, 2024.

[24] A. Campos-Cruz, G. Espinosa-Flores-Verdad, A. Torres-Jacome, and E. Tlelo-Cuautle, "On the prediction of the threshold voltage degradation in CMOS technology due to bias-temperature instabilityv, *Electronics*, vol. 7, no. 12, p. 427, 2018.

[25] B. Tudor, J. Wang, Z. Chen, R. Tan, W. Liu, and F. Lee, "An accurate and scalable MOSFET aging model for circuit simulation", in *Proc. 2011 12th Int. Symp. Quality Electron. Design*, pp. 1–4, 2011.

[26] M.F. Li, S.J. Rhee, and C. Choi, "Dynamic Bias-Temperature Instability in Ultrathin SiO_2 and HfO_2 MOSFETs and Its Impact on Device Lifetime", *Jpn. J. Appl. Phys.*, vol. 43, pp. 7807–7814, 2004.

[27] Synopsys, "MOS Device Aging Analysis with HSPICE and CustomSim", *Synopsys Technical Documentation*, 2023.

[28] W. Wang, S. Yang, S. Bhardwaj, S. Vrudhula, F. Liu, and Y. Cao, "The impact of NBTI effect on combinational circuit: Modeling, simulation, and analysis", *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 18, no. 2, pp. 173–183, 2009.