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**Original scientific paper**

# IMPACT OF INTERFACE OXIDE TYPE ON THE GAMMA RADIATION RESPONSE OF SIC TTL ICS*

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**Abstract.** *In this study, we investigate the impact of Gamma Radiation on 4H Silicon Carbide (SiC) Transistor-Transistor Logic (TTL) integrated circuits (ICs), particularly focusing on inverters processed with distinct types of interface oxides: Thermally Grown, Chemical Vapor Deposition, and Atomic Layer Deposition. This research was conducted using a $^{60}Co$ source at Hiroshima University, applying varied radiation doses (17.9 $rad_{(Si)}$/s, 7.3 $rad_{(Si)}$/s, and 2.47 $rad_{(Si)}$/s) to assess the resilience of the SiC inverters under these conditions. Our findings reveal that thermal oxides (Batch 1: $W_1$ and $W_2$) demonstrate higher radiation resilience compared to ALD and CVD interface oxides (Batch 2: $W_3$ and $W_4$), attributable to their denser structure and fewer defects. The study also identifies that while the inverters exhibit marginal degradation at gamma doses nearing 700 krad (under 6%), the most critical operational state is the passive mode ($V_{CC} = V_{IN} = 0$ V), where the build-up of induced charge in the oxide and interface may lead to early IC degradation of the noise margins. The outcomes from this research provide insights into the processing flow and enhancement of SiC electronics. Our results underscore the potential of SiC-based ICs in environments with high radiation levels, such as space missions, nuclear reactors, and medical applications, due to their enhanced radiation tolerance.*

**Key words**: *Silicon Carbide, BJT, ICs, Inverter, Co-60, TTL, Logic Device, Processing, gamma radiation, ELDRS*

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## 1. INTRODUCTION

In this study, we delve into the radiation response of bipolar 4H Silicon Carbide (SiC) based electronic low power logic devices, with a focus on the behavior of basic logic circuits. Our project builds upon prior research in the field [1-3], extending the knowledge base particularly on the performance of SiC bipolar circuits under radiation. The core of this study is an exploration of the behavior of SiC inverters under conditions of low exposure rate, a critical aspect due to the Enhanced Low Dose Rate Sensitivity (ELDRS) effect. The inverter, a fundamental logic component in digital electronics, serves as the cornerstone for understanding the resilience of electronics in radiation environment. Our study explores not only the operational aspects of the inverters under the Gamma Radiation, but assesses the influence of ELDRS effect in their performances as well. Transistor-Transistor Logic (TTL) is more robust in harsh environments where signals are prone to noise spikes and glitches, supply degradation etc which is a common occurrence in Medical Linear Accelerators (MedLINACs) [4-6] and Nuclear reactors [7-8].

Among wide-bandgap semiconductors, Silicon Carbide (SiC) stands out as a material of remarkable capabilities, overshadowing traditional Silicon (Si) and emerging contenders like Gallium Nitride (GaN) in electronic applications. The hallmark of SiC lies in its robustness, particularly its ability to function reliably under extreme conditions. This includes operating at temperatures that surpass 500°C [9,10] and enduring high electric field, which are significantly beyond the thresholds tolerated by both Si and GaN. In the field of logic ICs, this means achieving not only better performance but also greater flexibility in challenging environments.

The properties of SiC contribute to diminishing the dimensions and mass of the resulting electronic components. However, it is essential to recognize the broader context in which these advantages of SiC are situated. The widespread integration of SiC in the semiconductor industry is not without its challenges, primarily due to considerations such as the current cost and market availability. These factors play a pivotal role in determining the feasibility and rate at which SiC can be adopted on a global scale.

In semiconductor technology, Total Ionizing Dose (TID) effects from Gamma Rays are increasingly relevant. While currently more pertinent to space missions, especially in deep space, TID's impact is crucial in fields like medical application [11,12] and nuclear science [13,14]. In medical applications, particularly diagnostic and radiotherapy equipment, semiconductor resilience to TID is vital for maintaining precision and reliability.

TID's role in the semiconductor industry may seem limited, but its significance in medical settings, especially under high radiation doses, is profound. Semiconductors that endure high radiation without losing functionality enhance medical diagnostics and treatments, leading to safer, more effective healthcare.

The nuclear sector's reliance on semiconductor technology also warrants attention. High radiation levels in this field make understanding the behavior of basic logic devices like inverters critical for safety and lifetime of electronic components in nuclear reactor and radioactive material handling.

A notable knowledge gap exists in the behavior of SiC TTL low-power logic devices under Gamma Radiation. Addressing this, our research provides insights into the performance and durability of SiC TTL electronics in high-radiation environments, contributing to practical solutions and enhancing understanding in this critical area.

## 2. MATERIALS AND METHODS

The TTL inverter under investigation is designed using resistors, four NPN transistors, and a diode. A comprehensive exposition of the basic Bipolar Junction Transistor (BJT) topology, alongside its behavior under radiation exposure and the critical operational parameters, has been detailed in reference [2].

The structural design of the inverter circuit can be categorized into three distinct stages, as illustrated in Figure 1. The initial segment, referred to as the 'Input Stage,' incorporates a single-emitter transistor. This study opts for a simplified circuit configuration, utilizing a single-emitter in lieu of a multi-emitter transistor typical of a multiple-input NAND gate, to facilitate experimental precision and clarity. After the Input Stage, the signal enters the 'Phase Splitter' stage. Here, a transistor acts as a switch, splitting the signal phase into binary outputs: 0 and 1. The final segment, designated as the 'Output Stage,' features a duo of transistors arranged in a totem-pole configuration, operating exclusively to alternate between the logic high (1 = 10 V) and low states (0 = 0 V). In scenarios where the input is set with $V_{CC}$ at 15 V and $V_{IN}$ at 0 V, transistor $Q_1$ is in the 'ON' state, consequently switching $Q_2$ to the 'OFF' state. This configuration leads to a phase split, yielding a logic 1 at the collector of $Q_1$ and a logic 0 at its emitter. Subsequently, $Q_3$ is activated ('ON') while $Q_4$ is deactivated ('OFF'), resulting in an output of logic 1. It is noteworthy that the output voltage stabilizes at 10 V, a phenomenon attributable to the voltage drops across the PN junctions of $Q_3$ and $D_1$. This characteristic voltage reduction is also observed in silicon TTL circuits, where output voltage does not equate to the supply voltage due to similar junction drops.

Conversely, with $V_{CC}$ maintained at 15 V and $V_{IN}$ adjusted to 15 V, the emitter-base junction of $Q_1$ becomes reverse-biased, rendering it in a reverse active mode. This transition causes $Q_2$, the phase splitter transistor, to invert the collector to a logic 0 and the emitter to a logic 1. Following this, $Q_3$ transitions to the 'OFF' state and $Q_4$ to the 'ON' state, resulting in the output adopting a logic 0 state, essentially registering close to 0 V.

The choice of 4H SiC as the foundational material for this study stems from its exceptional resilience to extreme operating conditions [8]. SiC's wide bandgap and high thermal conductivity enable it to withstand elevated temperatures that would severely compromise the performance of conventional silicon-based devices [10]. This inherent robustness makes SiC an ideal candidate for applications in harsh environments, such as those encountered in aerospace, automotive, and industrial settings, where high temperatures and aggressive chemical conditions are commonplace [15]. Furthermore, the utilization of bipolar technology in SiC devices leverages the inherent radiation tolerance observed in silicon bipolar transistors [18], offering the potential for enhanced reliability in radiation-rich environments. This combination of material and device-level advantages positions 4H SiC bipolar technology as a promising platform for the development of next-generation electronics capable of operating reliably under extreme conditions.

In the course of this project [2,3], a series of wafers underwent fabrication, each distinguished by different oxide types at the SiC-$SiO_2$ interfaces. While there were slight variations in the base layer compositions across these wafers, such discrepancies did not manifest in any significant effects under radiation exposure. We arrived at this conclusion due to the absence of any significant difference in the nature of degradation (dose or exposure rate) for samples from wafers of various layer's composition.

The fabrication process entailed epitaxial growth on 100 mm 4H-SiC wafers, leading to the formation of multi-layered structures with 6 and 7 layers atop the 4H-SiC substrates. Oxidation process played a crucial role in laying the groundwork for subsequent experiments.

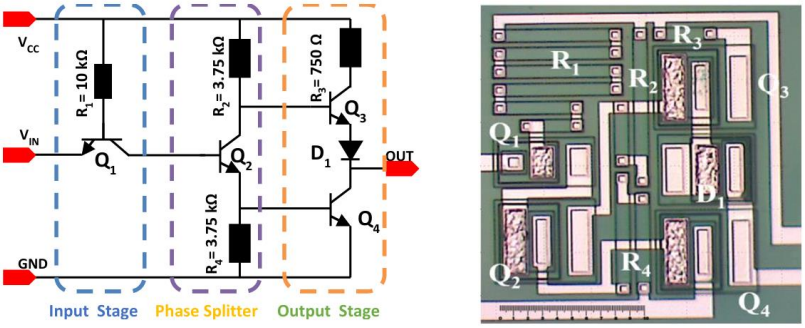


**Fig. 1** BJT SiC Inverter representation
Left picture - A schematic representation of the Integrated inverter TTL IC,
Right picture - A photograph of the fabricated inverter (scale bar is 100 μm)

In our study, we used three different methods to create interface oxides on SiC wafers. Table 1 presents the oxide compositions and processing details.

**Table 1** Summary of interface oxide types and processed batches

| Batch | Wafer | Interface Oxide Type | Fabrication Details |
|---|---|---|---|
| 1 | W1 & W2 | Thermally Grown | Dry-grown to 30 nm, enhanced with PECVD to 70 nm, annealed in N2O atmosphere |
| 2 | W3 | CVD | Polyoxide layer formed by fully oxidizing a 40nm polysilicon layer, additional CVD oxide layer to reach 100 nm |
| 2 | W4 | ALD | 20 nm ALD oxide layer combined with an 80 nm CVD layer |

For wafers $W_1$ and $W_2$, the oxides were thermally dry-grown to 30 nm and further enhanced with Plasma-Enhanced Chemical Vapor Deposition (PECVD) to reach 70 nm. These layers were then annealed at a high temperature in an $N_2O$ atmosphere to ensure robust oxide formation. Wafer $W_3$ included a polyoxide layer formed by fully oxidizing a 40nm polysilicon layer and adding a Chemical Vapor Deposition (CVD) oxide layer to reach a total thickness of 100 nm. Finally, Wafer $W_4$ utilized a dual-step oxide process, combining a 20 nm layer of Atomic Layer Deposition (ALD) oxide with an 80 nm CVD layer, for a unique approach to oxide formation.

Some experimental outcomes from Batch 1 ($W_1$ and $W_2$) have been previously presented in [3], encompassing detailed analyses of the critical regime investigation and the parameters influencing degradation. Conversely, samples from Batch 2 ($W_3$ and $W_4$) were fabricated for separate experiment using the same measurement equipment.

## 3. Gamma Irradiation Facility, Dosimetry and Exposure Procedure

The gamma radiation experiments in this study were conducted using a 60Co source, in collaboration with the 'Research Center for Nanodevices' at Hiroshima University (HU), Japan. The gamma irradiation facility at HU is equipped with a specialized source

comprising fifteen rod-shaped elements. Each element contains 60Co, sealed and arranged within a cylindrical container [14]. This configuration enables the emission of dual photons, with 1.17 and 1.33 MeV energies, yielding an average energy of approximately 1.25 MeV.

For the irradiation testing of the SiC inverters, the process was calibrated using the ESR-alanine dosimetry technique. This approach ensured precision in measuring the absorbed radiation doses, a critical aspect of the experimental setup.

The SiC samples were subjected to a spectrum of dose rates, specifically at 17.9 rad(Si)/s, 7.3 rad(Si)/s, and 2.47 rad(Si)/s. It is important to highlight that the 60Co source inherently emits low-energy secondary photons, a characteristic that could potentially introduce noise into the experimental data. To mitigate this, an Aluminum/Lead (Al/Pb) filter was positioned in front of the samples during the radiation exposure. This configuration was essential for maintaining reliable data acquisition. It effectively eliminated most of potential noise and allowed for accurate assessment of the SiC inverters' response to Gamma radiation.

A important aspect of the study was the variation in the intensity of the 60Co source, providing a diversified approach to understanding the radiation response of these differently processed wafers. The investigation of wafers W3 and W4 followed the methodology elucidated in [2], with a special focus on evaluating the Enhanced Low Dose Rate Sensitivity (ELDRS). To further investigate the impact of radiation on the ICs' performance, we conducted additional tests under various biasing conditions ((VCC = VIN = 0 V), biased with VIN = "0" (VCC = 10V), and biased with VIN = "1" (VCC = 10V)). The exposure/measurement ratio was maintained at 10/1, consistent with the methodology employed in previous studies [2, 3].

## 4. Results and Discussion

In the ensuing discussion, we delve into the nuances of the inverter's transfer characteristics under varying doses of radiation exposure, as elucidated in Figures 2 and 3. These figures clearly illustrate the variations in the output voltage transfer characteristics, particularly the transition from a High (logic state 1) to a Low (logic state 0) state. To maintain clarity and focus in the graphical representation, the inverse transition is not included in these figures. Furthermore, Figures 2b and 3b are instrumental in showcasing the behaviors of $I_{CC}$ (Supply Current) during the transient phases in both the High-to-Low and Low-to-High directions [9].

An observation from this analysis is the fundamental similarity in the degradation patterns and curve shapes across the different samples, indicating a consistent degradation mechanism in the inverters when subjected to gamma radiation. This uniformity in response is suggestive of a shared underlying process affecting the devices in a comparable manner.

However, notable differences can be observed in the upper part of the transient response characteristics, particularly in the range of $V_{IN}$ = 5.5 to 8 V, as depicted in Figures 3a and 4a. These discrepancies are hypothesized to stem not from variations in the device processing but rather from electromagnetic interference in the power grid of the bunker where the Device Under Test (DUTs) were exposed to radiation. This interference likely influenced the results, leading to the observed deviations in the transient response characteristics at certain voltage intervals.

Learning how inverters react to radiation is key for figuring out how well they will work in places with gamma rays. We have seen that these inverters tend to break down in

a predictable way. Plus, things like electromagnetic interference also affect them. This gives us a full picture of how tough and reliable these inverters are when they are put to the test in tough environments.

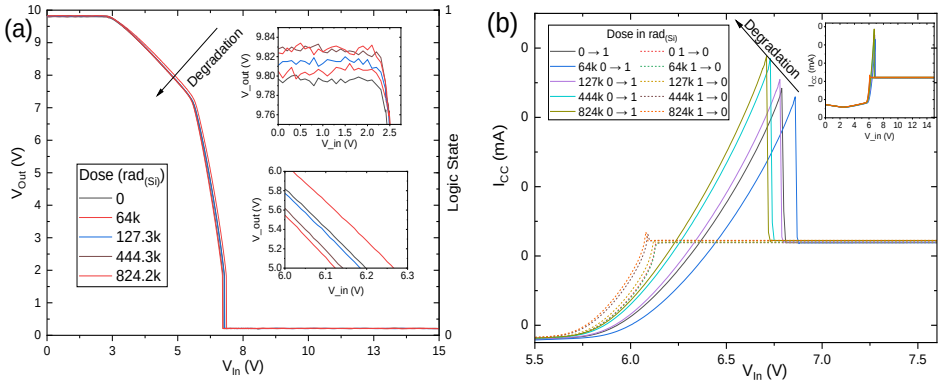


**Fig. 2** Measured transfer characteristics of SiC Inverter Batch 1 (a) Voltage output characteristic $V_{OUT}$ (V), (b) Supply Current $I_{CC}$ (A) for input voltages between 0 and 15 V(inset) and magnified for 5.5 to 8 V

Nevertheless, it's crucial to highlight a notable distinction in the profile of the minor peak (1→0) depicted in Figure 3b. This difference suggests the existence of an extra leakage in the Output Stage, as shown in Figure 1, which was not detected in Batch 1.

In Figure 4, we provide a detailed view that clarifies the results shown in Figure 3, focusing on the degradation dynamics of the Supply Current ($I_{CC}$) during the signal transitions. These transitions, from low to high levels (solid line) and high to low levels (dashed line) during the radiation exposure process, are analyzed. Additionally, for a complete understanding, the input voltages ($V_{IN}$) corresponding to the $I_{CC}$(max) values are also clearly outlined.

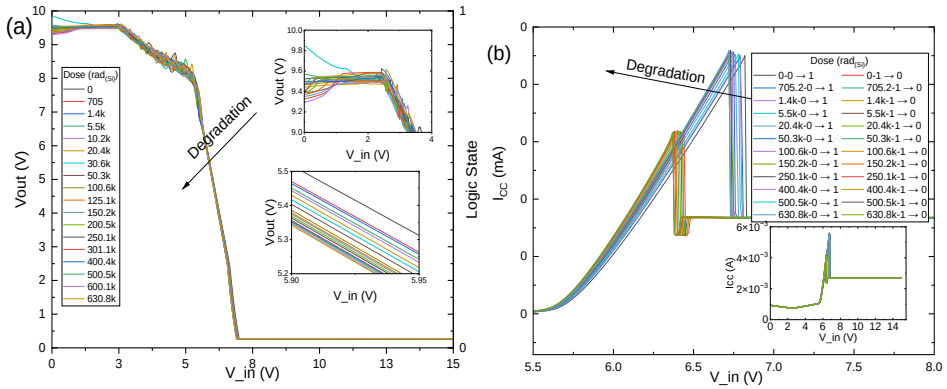


**Fig. 3** Measured transfer characteristics of SiC Inverter Batch 2. (a) Voltage output characteristic Vout (V), (b) Supply Current Icc (A) for input voltages between 0 and 15 V (inset) and magnified for 5.5 to 8 V

Upon detailed scrutiny of these dynamics, it is discernible that during the direct transition phase (from 0 to 1), Batch 1, as illustrated in Figures 3a and 4a, exhibits a significant shift in $V_{IN}$, by approximately 7.5%, predominantly within the initial three measurement iterations.

This shift subsequently reaches a saturation point at higher doses. Concurrently, the $I_{CC}$ demonstrates a minor, albeit progressive, degradation over time. In contrast, Batch 2, as shown in Figures 3b and 4b, manifests a lesser degree of $V_{IN}$ degradation, approximately in the range of 1-1.5%. Although fluctuations in $I_{CC}$ values are noted, these do not conclusively point to any substantial degradation in this parameter.

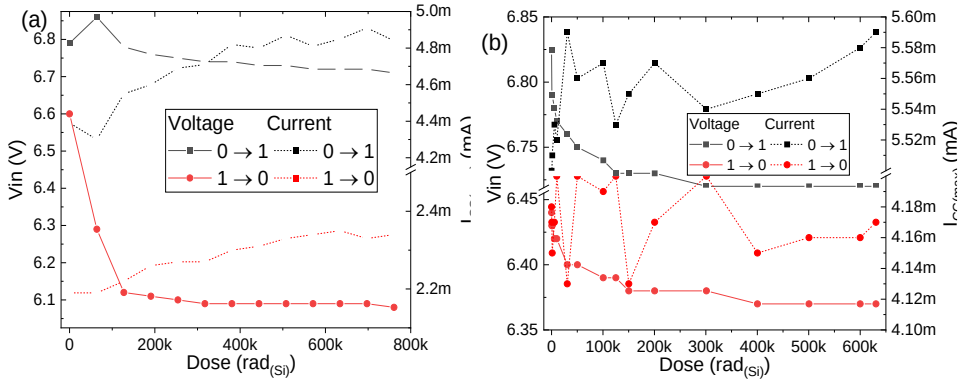


**Fig. 4** Dynamics of parameter degradations for SiC Inverters in (a) Batch 1 and (b) Batch 2

Building upon previous findings [3], it is understood that the circuit comprising $Q_1$, $Q_2$, and $Q_4$, as depicted in Figure 1a, is pivotal in mediating the transition between low and high logic states. At the discrete device level, we have identified that degradation is predominantly influenced by alterations in the base-emitter region. A notable observation is the higher $I_{CC}$ (max) peak during the reverse transition, which is primarily attributed to the diode $D_1$.

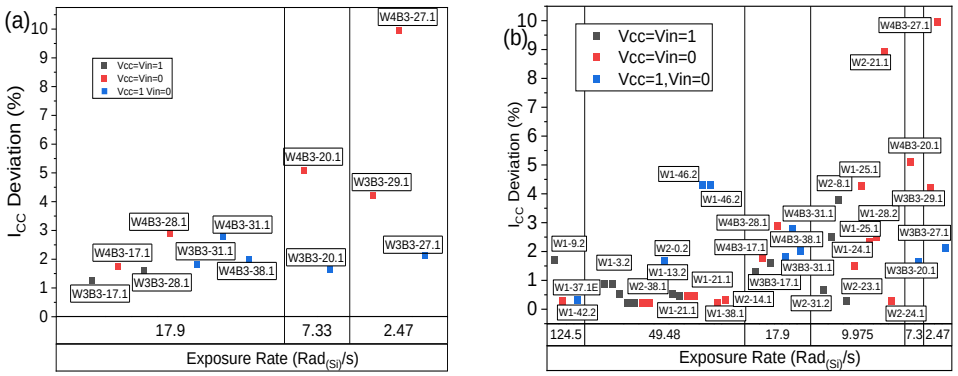


**Fig. 5** Deviation of $I_{cc}$ parameter for Batch 1 and 2 in Relative units. Dose rates in units off Rad/s

In this segment of our analysis, we focus on two distinct batches of semiconductor In this segment of our analysis, we focus on two distinct batches of semiconductor devices: Batch 1, encompassing $W_1$ and $W_2$, which featured thermally grown oxide, and Batch 2, comprising W3 and W4, with CVD oxides.

Figure 5 provides a comparative analysis of the radiation-induced degradation in the supply current ($I_{CC}$) for both Batch 1 and Batch 2 SiC inverters under various biasing conditions, with each sample receiving a minimum total dose of 600 krad. The degradation is presented in relative units, emphasizing the deviation in $I_{CC}$ across different dose rates, as the primary focus of this academic research is to understand the degradation dynamics rather than certifying the devices for a specific dose threshold. The circuit was irradiated under three distinct conditions: unbiased ($V_{CC} = V_{IN} = 0$ V), biased with $V_{IN}$ = "0" ($V_{CC}$ = 10V), and biased with $V_{IN}$ = "1" ($V_{CC}$ = 10V). It is important to note that the $I_{CC}$ deviation observed at $V_{CC} = 0$ signifies the leakage current induced by radiation even when the circuit is not actively operating.

From the standpoint of radiation resistance, Batch 1 ($W_1$ and $W_2$) demonstrated enhanced performance. This result is congruent with theoretical expectations, as thermally grown oxide is known for its denser structure and reduced defect density. Furthermore, the annealing process used in these devices is crucial for reducing proton ($^{+}H$) accumulation within the oxide layer, which in turn improves radiation hardness.

Conversely, $W_3$ of Batch 2 showed higher radiation resistance, due to the superior quality of its interface oxide, which naturally had less imperfections before being exposed to gamma radiation. However, $W_4$ from the same batch showed the least favorable outcome in terms of radiation resilience. This observation was somewhat unexpected, considering conformal coatings applied by the ALD process on the base-emitter-oxide interface were hypothesized to improve radiation hardness. A plausible explanation for this discrepancy could be the potential incorporation of impurities during the chemical-based ALD process.

Further analysis between $W_1$ and $W_3$, and $W_2$ and $W_4$ (each having slightly varied SiC layer compositions) confirmed that the bulk effects of gamma radiation are relatively less critical. Additionally, the presence of the Enhanced Low Dose Rate Sensitivity (ELDRS) effect was confirmed. Nevertheless, it is evident that there is considerable room for improvement in optimizing the SiC-$SiO_2$ interface.

All circuits analyzed demonstrated minor degradation at gamma radiation doses nearing 700 kRad (below 6%) compared to silicon inverters. The most critical operational state was identified in the passive mode ($V_{CC} = V_{IN} = 0$ V), where a consistent build-up of induced charge in the oxide and interface could potentially lead to early IC triggering without any loss in logical levels without diminishing in logical levels.

Our study highlights the superior radiation resilience of thermal oxides in SiC ICs compared to CVD and ALD oxides. We've identified a significant vulnerability of these ICs in passive mode, which opens new avenues for future studies. Despite some degradation under high gamma radiation, SiC ICs hold great promise for high-radiation environments like space and nuclear facilities. The study also confirmed the presence of the ELDRS effect and the less critical nature of gamma radiation's bulk effects. The most crucial finding is the minor degradation of these circuits at high gamma doses and the potential of SiC-based ICs in challenging environments, pointing to their viability as robust alternatives to traditional silicon-based electronics. Future work will focus on further enhancing the SiC-$SiO_2$ interface and assessing these ICs under various radiation sources, underscoring their potential and limitations.

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