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Original scientific paper

DESIGN OF A SCPLL FOR APPLICATION IN DISTRIBUTED FREQUENCY BANDS

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Abstract. *The manuscript presents the design of a Switched Controlled Phase Locked Loop (SCPLL), a pivotal component in communication systems. Comprising a Phase Frequency Detector (PFD), Charge Pump (CP), Low Pass Filter (LPF), and Voltage Controlled Oscillator (VCO), the PLL is instrumental in maintaining precise signal synchronization. This novel SCPLL incorporates a versatile Phase Locked Loop architecture. The VCO noteworthy feature is its ability to operate within distributed frequency bands, Lower band (LB) and Upper band (UB), specifically ranging from 45 MHz to 600 MHz and 850 MHz to 1.04 GHz. Higher-order low pass filters is demonstrated to be highly effective in reducing unwanted spurious emissions, thereby enhancing signal purity. The Switched Controller (SC) within this system offers the ability to select the desired frequency band and filter order, providing adaptability and control over system performance. Spur reduction is found to be approximately -4 dBc in UB while negligible difference in LB on replacing first order filter by 2nd order filter. The experimental Phase noise value of the proposed SCPLL is estimated to be -93.15 dBc/Hz at 1MHz and -118.79 dBc/Hz at 10 MHz respectively. Power Consumption of the circuit is found to be 1.8 mw with an area of 0.0023 mm^2. In terms of efficiency, the circuit demonstrates an impressive tradeoff between the frequency of operation, phase noise, spur reduction and power.*

Key words: *Switched Controlled (DSC); Phase Locked Loop (PLL); Tuning Range; Spur*

1. INTRODUCTION

Phase Locked Loop (PLL) represents an electronic circuit which is widely used in equipment design for communication system like AM radio receivers, frequency de-modulators, multipliers, dividers and frequency synthesizers. As a control mechanism, a PLL is engineered to align the phase of an input signal with that of a reference signal, consequently generating an output signal in sync with the reference signal. The utility of PLLs extend

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across electronic systems, providing capabilities for the generation of signals that are stable, accurate and capable of frequency adjustment. Contemporary research endeavors are concentrated on the system-level development of PLLs that are not only cost-efficient and power-conservative but also reliable, exhibiting reduced phase noise and enhanced stability. These qualities are essential for achieving optimal performance in PLLs [1-5]. Shruti Suman et al. developed a Phase Locked Loop (PLL) leveraging an advanced Voltage-Controlled Oscillator (VCO) architecture, enabling a frequency spectrum from 2.26 GHz to 3.44 GHz through the modulation of control voltage between 1 V and 3 V. Nevertheless, their design overlooked the aspect of phase noise [6]. In contrast, Armaroli et al. presented a behavioral modeling technique for Charge Pump PLLs (CP-PLLs) in the time domain, incorporating nonlinear components. They introduced a simplified simulation strategy by segmenting the network into multiple directional blocks. Innovative models for both the Phase Frequency Detector (PFD) and VCO were proposed, with the charge pump model being developed from the dynamics of its input signals. For a second-order PLL, they predicated their analysis on certain assumptions related to the closed-loop natural frequency and damping ratio to determine the crossover frequency. Their algorithms demonstrated a remarkable efficiency in simulation time, completing in just 70 seconds of CPU time, though the discrete nature of the circuit resulted in increased noise [7]. Acco et al. explored both discrete linear and nonlinear models for CP-PLLs, specifically examining the inclusion of a frequency divider circuit. Within their discrete-time linear model, the equations governing the VCO, N-divider, and filter were linear and simple, in contrast to the nonlinear characteristics of the PFD. They achieved a linear representation of the entire system suitable for the CP-PLL locked state by approximating the link between phase error and average current input. This event-driven and nonlinear model offers precise representation of both unlocked and overload conditions, achieving efficiency in simulation time. A notable parallel was observed between the discrete nonlinear model and the event-driven approach in terms of state variable estimation. They detailed a second-order model through nonlinear piecewise independent difference equations based on small error signals, underscoring the model's effectiveness in accurately depicting CP-PLL dynamic behaviors [8].

The VCO, PFD, and charge pump are critical components in CP-PLL architecture. Gogoi et al. presented a four-stage distributed band VCO with a 1049 MHz frequency and 157 µW power consumption [9]. Maneatis et al. developed a delay cell for a ring oscillator achieving 141 MHz frequency [10]. Yan et al. introduced a three-stage VCO operating in the 1.3–1.8 GHz range, but with high power consumption [11]. Tu et al. proposed a two-stage VCO covering 2.5–5.2 GHz, with a phase noise of -90.1 dBc/Hz at 1 MHz offset [12]. Kim et al. designed a four-stage oscillator with low phase noise at 900 MHz [13], while Meng Lieh et al. achieved a tuning range of 479 MHz to 4.09 GHz with a phase noise of -93.3 dBc/Hz at 1 MHz offset [13]. Further contributions include Mukherjee et al.'s development of two PFD architectures with lock-in detection, enhancing average gain and reducing the blind zone to 3 ps [14], Sundaram et al.'s PFD using pass transistor logic and delay cells, achieving operation without a dead zone and 28.8 µW power consumption at 100 MHz [15], and Pradhan et al.'s PFD with pass transistor logic, low power consumption, no dead zone, and a minimized blind zone of 44.23 ps [16]. Nelakuditi's work proposes an efficient linearized charge pump design aimed at improving both power and phase noise performance in fractional-N PLLs [17].

Babaie et al. introduced a charge-sampling phase-locked loop (CSPLL) with a charge-domain sub-sampling phase detector, enhancing phase-detection gain while reducing in-band proposed a charge pump circuit with improved mismatched current, suitable for portable wireless devices [17]. Soltani et al. introduced a digital calibration scheme for jitter reduction, achieving significant reductions in peak-to-peak and RMS jitter at a 1.6 GHz operating frequency [18]. Jin-Yue at el presented a 1-GHz PLL frequency synthesizer designed for IEEE 1394b PHY applications, using a 4-stage ring oscillator to produce a 1-GHz frequency. This design is a third-order, type-2 charge pump PLL that consists of a charge pump of low ripple and a VCO based on a ring oscillator. The system breaks down the 1 GHz clock into 200MHz, 100MHz, 50MHz, and 25MHz frequencies. It has a quick settling time of 4 μs and a low period jitter of 2.1 ps rms. The unique aspect of this design is its ability to provide various frequencies and phases using the same VCO, effectively working across both higher and lower frequency ranges without the need to modify the circuit design [20]. Meanwhile, Homayoun's at el created a model that accurately measures how small signals are transmitted through second-order CP-PLLs, considering both minor and significant signal effects on stability. They found that the stability is affected when different parts of the loop signal overlap, but maintaining the loop bandwidth at nearly half of the input frequency helps keep the CP-PLLs stable [21]. The literature review identifies critical gaps, such as high phase noise, spurious outputs (spurs) at wide frequency ranges, and high power consumption, which are significant challenges in PLL design. Our proposed PLL addresses these issues by implementing an innovative design focused on minimizing phase noise and spurs across extensive frequency bands, while also emphasizing power efficiency. By incorporating the flexibility to select between first and second-order filters, our design enhances adaptability and performance, effectively overcoming the limitations highlighted in current research and offering a more efficient and versatile solution for PLL applications. The paper is organized to sequentially cover the development and examination of a SCPLL system. Section 2 discusses the proposed PLL design. Section 3 delves into the operating bands of the PLL. Section 4 provides an analysis of the system. Finally, Section 5 concludes the paper with a summary of the findings and contribution.

2. PROPOSED VCO

A novel PLL architecture is proposed, designed to provide versatile performance in terms of filtering order and frequency band, thereby meeting the evolving requirements of modern communication systems. Fig. 1 shows the proposed PLL design. The core components of the proposed PLL comprise a PFD characterized by low power consumption and minimal phase noise, CP, 1st and 2nd order LPF, a distributed frequency bands VCO, SC and a Voltage Divider circuit. A key feature of our SCPLL design is the flexibility to switch between 1st and 2nd order filtering configurations and frequency bands depending on the specific application needs. The SC, featuring two input pins CS1 and CS2 and three output pins S1, S2 and S3, plays a pivotal role in this adaptability. Specific combination of the pins CS1 and CS2 will facilitate PLL to transit between 2nd and 3rd order operation and at the same time switching between the frequencies band. This dynamic behavior is facilitated through the utilization of three control switches namely S1, S2, and S3 which dictate the filter order and frequency range of the PLL.

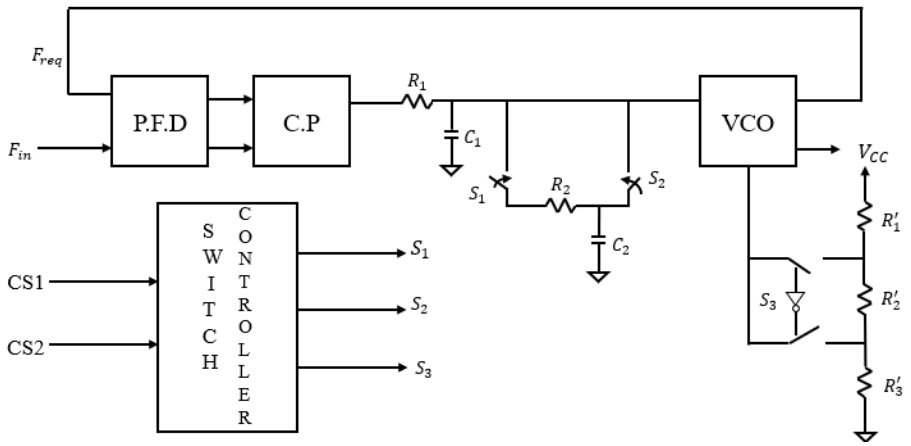


Fig. 1 Proposed PLL

In Table 1, we provide the operation of the SC. When S1=' off ', S2=' off ', and S3=' on ', the PLL operates as a 1st order filter within the frequency band of 45 MHz to 600 MHz. Similarly, when S1=' off ', S2=' off ', and S3=' off ', the PLL functions as a 1st order filter but within a higher frequency range of 850 MHz to 1.04 GHz. In contrast, with S1=' on ', S2=' on ', and, S3=' on ', the PLL switches to a 2nd order filter within the 45 MHz to 600 MHz frequency band. Finally, when S1=' on ', S2=' on ', and S3='off', the PLL adopts a 2nd order filtering configuration within the 850 MHz to 1.04 GHz frequency range. This flexible and adaptive behavior, as illustrated in the ac-companying table, is further supported by the control switches CS1 and CS2.

Table 1 Operation of the Switch Controller

Control Switches		Output Switches			PLL order	Frequency Band
CS1	CS2	S1	S2	S3		
Off	Off	Off	Off	On	2nd	45 Mhz to 600 MHz
Off	On	Off	Off	Off	2nd	850 Mhz to 1040 MHz
On	Off	On	On	On	3rd	45 Mhz to 600 MHz
On	On	On	On	Off	3rd	850 Mhz to 1040 MHz

The proposed Switched Controlled Phase Locked Loop (SCPLL) introduces dynamic operation across two frequency bands, optimizing phase noise, Jitter, area, power consumption and spur reduction. The integration of higher-order low pass filters and a Switched Controller (SC) allows for real-time selection of frequency bands and filter orders, improving spurious emission suppression and power efficiency while maintaining compact design and enhanced performance

3. OPERATING BANDS

Fig. 2 shows the circuits used for designing SCPLL namely PFD, Charge Pump, delay cell and VCO. The oscillation frequency of the PLL is calculated based on the delay introduced by the delay cell, where the time constants T_c (charging) and T_d (discharging) are used. A general equation (1) that incorporates these time constants is utilized to determine the frequency.

When S2 is on (bypassing R2), the compensating zero is removed the compensating zero is removed, reducing phase margin and causing a first-order filter response. This may lead to slower settling, increased overshoot, and potential instability. When S2 is off, the zero from R2 and C2 improves phase margin, resulting in a second-order filter response. This enhances stability, with a faster and smoother transient response, reduced overshoot, and minimal oscillations. To maintain the right phase and desired oscillation the ratio of capacitances (C2/ C1) is considered as 20 [22]. In case the capacitors of the filters used are poly-poly capacitors then bottom-plate switching is typically preferred. This minimizes parasitic effects and noise coupling into the sensitive VCO tuning node. Switching on the top plate could introduce parasitic capacitance from routing and potentially affect the VCO's stability. The use of bottom-plate switching helps maintain consistent loop filter performance and minimizes interference with the charge-pump dynamics.

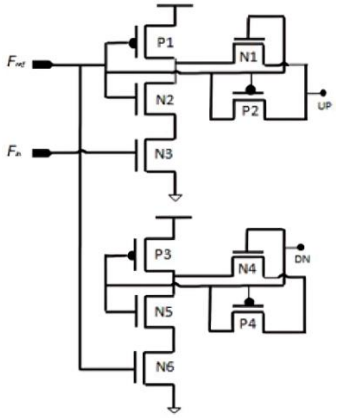
$$T_{const} = R_{total} * C_{total} \tag{1}$$

Where, R_{total} represents the resistance encountered along both the charging and discharging routes, while C_{total} refers to the aggregate capacitance, which encompasses all the parasitic capacitances combined. Hence the oscillating frequency can be given by equation (2).

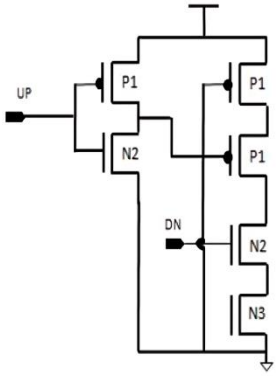
$$f_d = \frac{1}{T\_c + T\_d} \tag{2}$$

The delay cell is designed for dual-loop ring architecture within a voltage-controlled oscillator (VCO), as referenced in studies [9]. The primary loop is driven by transistors M1 and M2, and the secondary loop by M3 and M4, enhancing oscillatory amplitude through this dual-loop approach. The frequency of the ring VCO is modulated by transistor M13. The feedback mechanism of the latch comprises transistors M5 through M12, facilitating precise control over the latch delay time via Vcntr2. Simultaneously, Vcntr1 enables the VCO's operation across both low and high frequency ranges, ensuring versatile performance.

$$T_{const\_1} = R_{total\_3} * C_{total\_L} \tag{3}$$



(a)



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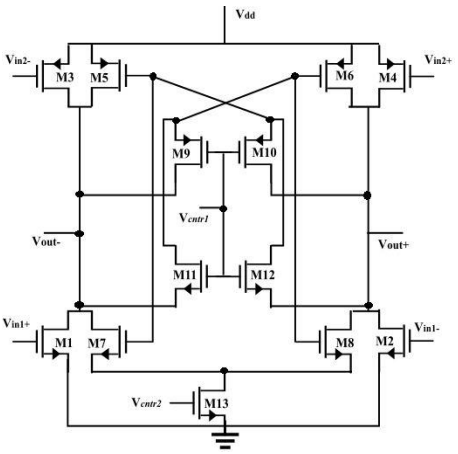

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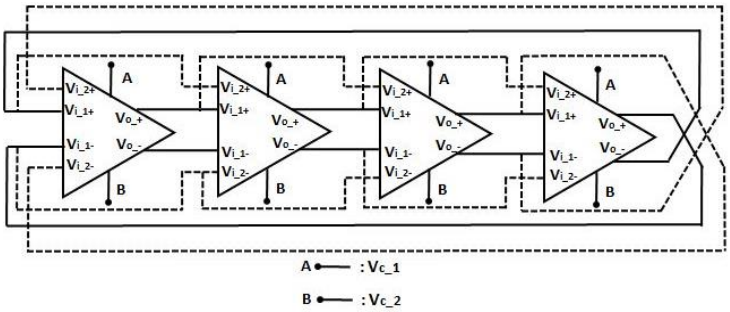


(d)

Fig. 2 (a) PFD[2] (b) CP (c) Delay Cell [9] (d) VCO [9]

The settling behavior of the analog control voltage during state transitions is now highlighted in the graph of Fig. 3, specifically for a control voltage of 0.6 V. The analysis shows that a settling time of approximately 8 ns is necessary when the operating frequency is 750 MHz, with the given control voltage. At an operating frequency of 1 GHz, the 8 ns delay would contribute an additional 18.06 dBc/Hz of phase noise at a 1 MHz offset. This would lead to a significant increase in the phase noise at that offset due to the delay-induced jitter.4. Plot the RMS and peak-to-peak jitter based on the whole input frequency range.

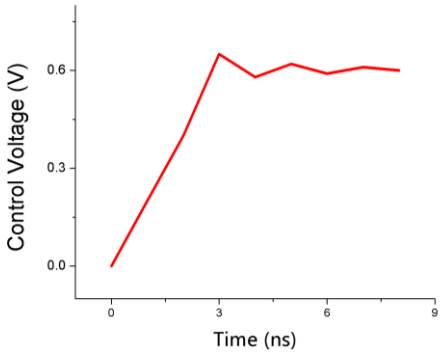


Fig. 3 Transient analysis when the control voltage is 0.6 v and the transition takes from path one to two.

R_{total_3} represents the effective resistance of the M3 MOSFET while C_{total_L} denotes the total parasitic capacitance linked to the output voltage $V_{out\text{-}}$. It can be determined using the following formula

$$R_{total\ 3} = \frac{1}{M_p C_{oxide} \frac{W_{id}}{L_{en}} \left(\left| V_{olt\_gs} \right| - \left| V_{olt\_tp} \right| \right)} \tag{4}$$

$$\begin{aligned} C_{total\_} = {} & C_{c\_db1} + C_{c\_gd1} + C_{c\_db3} + C_{c\_gd3} + C_{c\_ds3} + C_{c\_db5} + C_{c\_gd5} \\ & + C_{c\_db7} + C_{c\_gd7} + C_{c\_db9} + C_{c\_gd9} + C_{c\_db11} + C_{c\_gd11} \\ & + C_{c\_in\_x} \end{aligned} \tag{5}$$

where
M_p is Mobility of holes
C_{oxide} is oxide capacitance
W_{id} is Channel width of p-type transistor
L_{en} is Channel Length of p-type transistor
V_{olt_gs} is voltage between gate and source
V_{olt_tp} is threshold-voltage of p-type transistor

$C_{c\_in\_x}$ refers to the capacitance at the input of the subsequent stage, C_{c_db}, C_{c_gd} and C_{c_gs} represent the capacitances between drain-body, gate-drain, and gate-source of the transistor, respectively. Load Voltage of the delay circuit V_{c_load} can be approximated by equation (6).

$$V_{C_{Load}} = -(V_{out\_o} - V_{load})V_{out\_o} \exp\left(-\frac{T_c}{T_{const\_1}}\right) \tag{6}$$

V_{out_o} and V_{load} are the delay cell output voltages in the terminals V_{out-} and V_{out+} respectively.

Now, supposing $T_{\_c}$ is the time interval in which capacitor charges to a value αV_{out_o} then

$$\alpha V_{out\_o} = V_{out\_o} - (V_{out\_1} - V_{load}) \exp\left(-\frac{T_c}{T_{const\_1}}\right) \tag{7}$$

α which is constant ranges from 0 to 1.

$$T\_c = T_{const\_1} \ln\left\{\frac{V_{out\_o} - V_{load}}{V_{out\_o}(1-\alpha)}\right\} \tag{8}$$

Similarly, $T_{\_d}$ can be approximated by equation (9) and total time period, T_f can be determined using equation (10)

$$T\_d = T_{const\_2} \ln\left\{\frac{V_{Load} - \alpha V_{out\_o}}{V_{Load}(1-\beta)}\right\} \tag{9}$$

$$T_f = T\_c + T\_d = T_{const\_1} \ln\left\{\frac{V_{out\_o} - V_{load}}{V_{out\_o}(1-\alpha)}\right\} + T_{const\_2} \ln\left\{\frac{V_{Load} - \alpha V_{out\_o}}{V_{Load}(1-\beta)}\right\} \tag{10}$$

Hence oscillation frequency for the four stage VCO can be given by equation (11)

$$F_{4\_s} = \frac{1}{4T_f} \tag{11}$$

In the proposed PLL four stages VCO is incorporated with two control voltages V_{c_1} and V_{c_2} that are obtained by integrating a voltage divider circuit with the SCPLL as shown in Fig 4. Two different bands of frequency that is LB- 45 MHz to 600 Mhz and UB -850 MHz to 1.04 GHz are obtained by setting V_{c_1} to two different voltages 0.2 V and 0.77 V while changing V_{c_2} from 0 V to 1 V. The two bands are shown in Fig 5 (a) and (b).

Thus, from the formulae it can be clearly interpreted that higher the mobility lower will be the resistance or in other words resistance is inversely proportional to mobility. And resistance is directly proportional to time constant hence oscillating frequency is inversely dependent on resistance and directly dependent on mobility. So, transistor with higher mobility can play crucial role in improving the oscillating frequency.

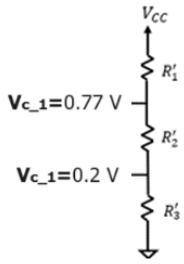
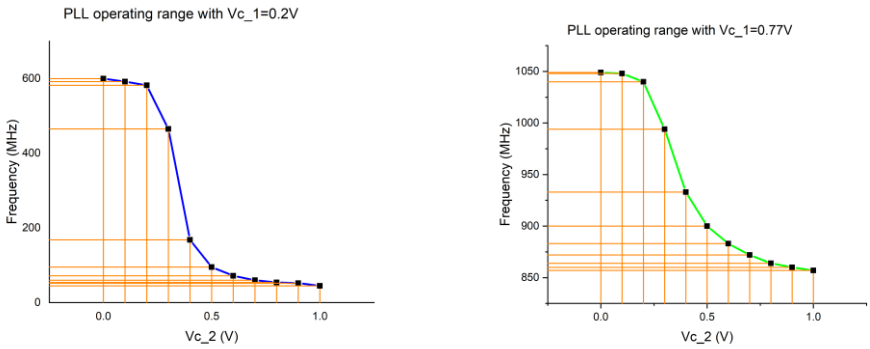


Fig. 4 Voltage Division Circuit



(a) (b)

Fig. 5 Frequency bands of SPCLL (a) Lower band (b) Upper band

4. ANALYSES

4.1. Phase Noise

Considering the key components that contribute to the overall phase noise, the parameters are defined as follows:

PDF_{noise}: Noise contribution from the PFD
CP_{noise}: Noise contribution from the CP
LPF_{1noise}: Noise contribution from 1st order Low Pass Filter (LPF)
LPF_{2noise}: Noise contribution from 2nd order LPF
VCO_{noise}: Noise contribution from VCO
K_{VCO}: VCO sensitivity in Hz/V

The switch settings (c1, c2) determine the operation mode of the PLL, affecting the noise analysis due to the selection of different LPFs and operating bands. We represent the mode selection as M_{select}(s1, s2,s 3), which will alter the effective LPF noise contribution and the VCO noise characteristics. The total Phase noise $L_T(f)$ of the SCPLL can be represented as sum of contributions from each component, adjusted by the loop filter's transfer function, $H(f)$ and transfer function of the closed loop, $T_c(f)$ as approximated in equation (12).

$$L_T(f) = \frac{PFD_{noise}}{|T_c(f)|^2} + \frac{CP_{noise}}{|H(f)T_c(f)|^2} + \frac{LPF_{noise}(M_{select}(s1,s2,s3))}{|H(f)T_c(f)|^2} + \frac{VCO_{noise}}{|H(f)|^2} \quad (12)$$

Where LPF_{1noise} ($M_{select}(s1,s2,s3)$) is determined by the current mode of operation, switching between LPF_{1noise} and LPF_{2noise}, and affecting VCO_{noise} depending on the frequency band. $T(f)$ is the closed loop transfer.

$H(f)$ represents transfer function of the selected LPF, which depends on the mode of operation. For 1st order it can be obtained with equation (13), where f_{c1} is the cutoff frequency.

$$H(f) = \frac{1}{1 + j\frac{f}{f_{c1}}} \quad (13)$$

For 2nd order $H(f)$ can be determined using equation (14), and f_{c2} is the cutoff frequency.

$$H(f) = \frac{1}{\left(1 + j\frac{f}{f_{c2}}\right)^2} \quad (14)$$

Fig. 6 and Fig. 7 depicts the Phase Noise Analysis of the SCPLL with first and second order filters respectively. Table 2 presents the corner analysis of output (O_Noise) and phase noise (P_N) for lower band frequency and Table 3 presents for Upper band frequency. Thus, from the analysis it can be concluded that the effect due to process parameters variation and other conditions is not much and gives satisfying results. Fig.8 shows a plot of rms jitter against entire frequency sweep.

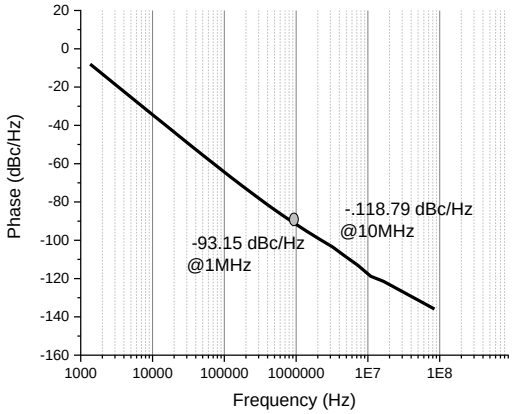


Fig. 6 Phase Noise of SCPLL (1st order Filter)

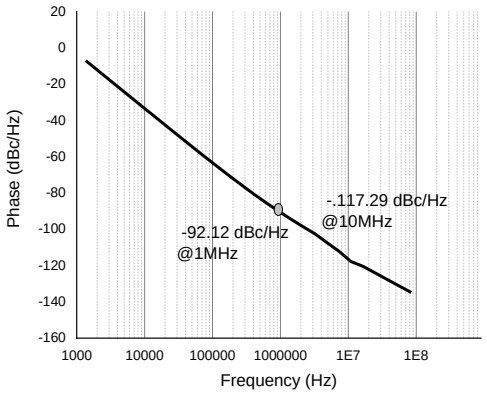


Fig. 7 Phase Noise of SCPLL (2nd order Filter)

Table 2 Corner_Analysis at *Vcntr1*=0.2 V and *Vcntr2*=0.1V with 1st order filter

Process Coners	Pre-Layout @1MHz		Pos-Layout @1MHz		Pre-Layout @10 MHz		Pos-Layout @10 MHz	
	O_Noise (dB)	P_N (dBc/Hz)	O_Noise (dB)	P_N (dBc/Hz)	O_Noise (dB)	P_N (dBc/Hz)	O_Noise (dB)	P_N (dBc/Hz)
NN	-94.21	-93.10	-92.56	-91.94	-121.56	-118.56	-118.15	-116.16
FF	-95.58	-94.88	-93.87	-92.65	-122.11	-118.85	-118.74	-116.98
FS	-93.86	-92.13	-91.42	-90.45	-119.20	-116.99	-116.85	-114.56
SF	-94.16	-92.98	-91.98	-91.24	-120.23	-117.08	-117.45	-115.56
SS	-92.45	-91.06	-90.84	-89.65	-118.44	-115.77	-115.22	-113.53

Table 3 Corner_Analysis at *Vcntr1*=0.2 V and *Vcntr2*=0.1V with 2nd order filter

Process Coners	Pre-Layout @1MHz		Pos-Layout @1MHz		Pre-Layout @10 MHz		Pos-Layout @10 MHz	
	O_Noise (dB)	P_N (dBc/Hz)	O_Noise (dB)	P_N (dBc/Hz)	O_Noise(dB)	P_N (dBc/Hz)	O_Noise (dB)	P_N (dBc/Hz)
NN	-94.21	-92.12	-92.05	-90.23	-119.04	-117.10	-117.54	-115.47
FF	-95.58	-92.95	-92.56	-91.05	-120.02	-117.81	-118.02	-116.22
FS	-93.86	-90.88	-89.14	-88.87	-117.08	-116.11	-114.34	-113.32
SF	-94.16	-91.49	-90.21	-89.10	-118.10	-116.98	-115.78	-114.87
SS	-92.45	-90.07	-88.41	-87.45	-116.11	-115.87	-113.56	-111.02

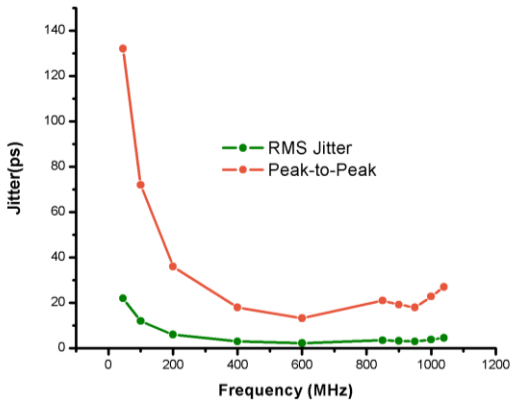
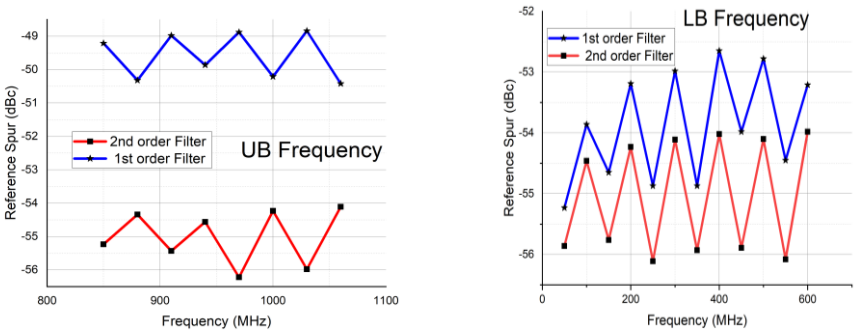


Fig. 8 RMS Jitter and Frequency Plot

4.2. Spur

A reference spur in Phase-Locked Loop (PLL) is a type of spurious signal that originates from imperfections in the reference signal used to control the PLL. These spurs are generated due to the inherent noise characteristics, such as jitter or phase noise, present in the reference source. When the PLL locks to the reference signal, any fluctuation or instability within this signal can modulate the output frequency, leading to the creation of additional, undesired frequency components alongside the main output signal. Reference spurs are particularly problematic because they directly impact the purity and stability of the PLL's output, potentially degrading the overall performance of systems that rely on precise frequency generation and control. Fig.9 (a) and (b) shows the effect of spur in the UB and LB due to the 1st and 2nd order filters. In the high frequency band the impact of high order filter is more significant with a difference of approximately 4dBc reference spur in this case.

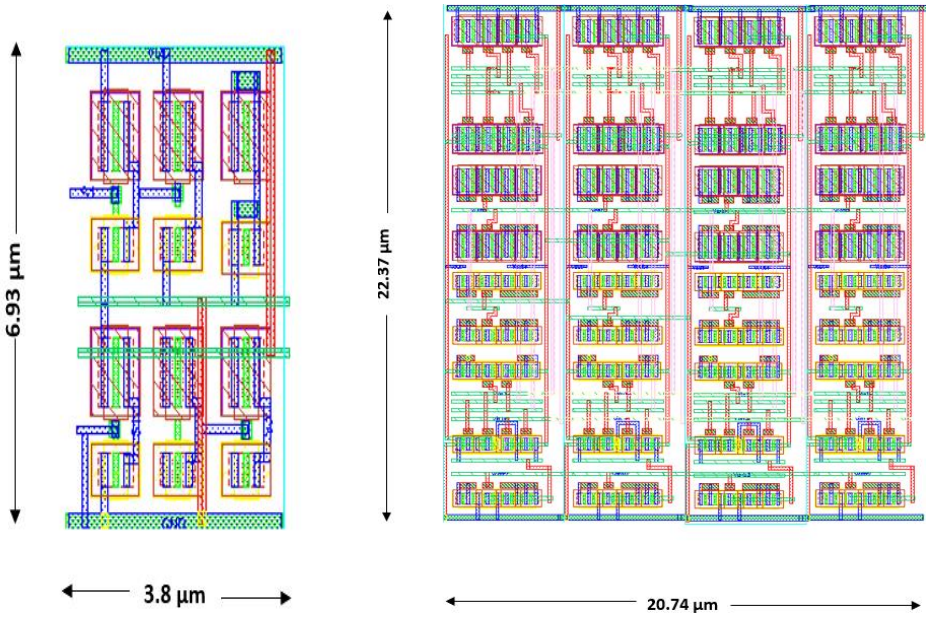


(a) (b)

Fig. 9 Reference Spur vs Frequency for (a) UB and (b) LB

The proposed SCPLL is implemented using cadence CMOS 90 nm technology. The switch controller circuit layout design is 3.80 µm x 6.93 µm and that of four-stage VCO layout is 24.74 µm x 22.37 µm which are depicted in Fig. 10 (a) and (b). And finally, the

proposed SCPLL layout dimension is 65.61 µm x 36.47 µm, thus the total area is 0.0023 mm^2 as in Fig. 11.



(a) (b)

Fig. 10 Layout of the (a) switch Controller (b) VCO

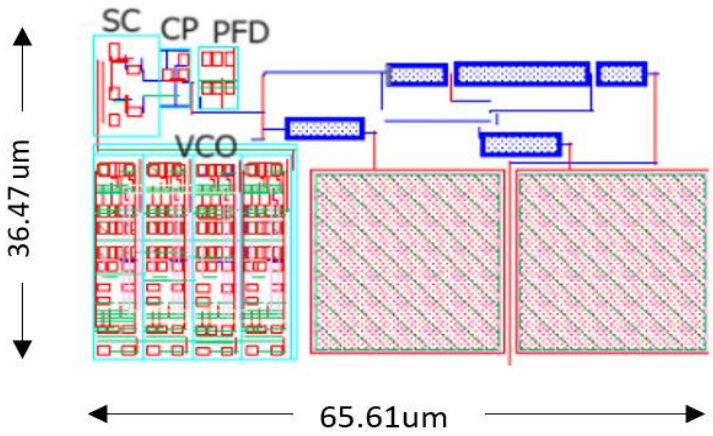


Fig. 11 SCPLL Layout

The proposed SCPLL is implemented using cadence CMOS 90 nm technology. The switch controller circuit layout design is 3.80 µm x 6.93 µm as shown in Fig. 10, while the four-stage VCO layout design depicted in Fig. 11 is 24.74 µm x 22.37 µm. And

finally, the proposed SCPLL layout dimension is 65.61 µm x 36.47 µm, thus the total area is 0.0023 mm^2 as in Fig. 12. A comparison table 4 is presented to give demonstration of tradeoffs between various parameters like operating frequency, area, power and reference spur. In the design, it should be ensured that in the case of poly-poly capacitors, careful consideration is given to the switching of the bottom-plate or top-plate to minimize parasitic capacitance and maintain signal integrity. When switching the top plate, it can help reduce parasitic effects, improving isolation and minimizing interference, especially in high-frequency bands like the Upper Band (850 MHz to 1.04 GHz). Conversely, switching the bottom plate may offer advantages in terms of faster switching speeds and more efficient routing, but it requires careful design to avoid increased parasitic capacitance that could affect overall performance. In terms of design tradeoffs, the system optimizes the frequency range, phase noise, and spur reduction by dynamically adjusting the filter order and operating frequency. As highlighted in Table 2, the tradeoff parameters—frequency range, phase noise, area, and spur reduction—are significantly improved when compared to existing designs, as indicated by the comparative Figure of Merit (FOM).

The Figure of Merit (FoM) for the proposed PLL is calculated using Equation (15) and is found to be 0.08998, which is quite favourable compared to values reported in existing literature. This indicates the PLL efficient balance between power consumption, phase noise, and operational frequency, showcasing the design's competitive performance within its domain.

$$FOM = L(\Delta f) - 20\log\left(\frac{f_{osc}}{\Delta f}\right) + 10\log\left(\frac{P_{avg}}{1\text{mW}}\right) \tag{15}$$

Table 4 Comparison Parameters

	This Work	[23] 13’	[24] 12’	[25] 23’
Voltage (V)	1	0.6	0.7	1.0
Freq (GHz)	0.045-0.6, 0.850 -1.04	0.48	1	0.5 -2
Reference Frequency (MHz)	49	1	1	1
CMOS Tech.	90 nm	90 nm	90 nm	90 nm
Area (mm^2)	0.0023	0.19	13.5	0.02
Power (mw)	1.8	0.771	37	1.2
Ref. Spur (dBc)	-56 &-50 (2^{nd} & 1^{st} Order Filter)	---	---	----
Phase Noise (dBc/Hz)	-93.15	-89	-96	-89.0
Jitter (RMS) ps	3	--	--	5.69

5. CONCLUSION

This research paper presents a breakthrough in Phase Locked Loop (PLL) technology with the development of a Switched Controlled Phase Locked Loop (SCPLL), enhancing communication systems' adaptability and performance. The SCPLL's versatile architecture allows operation across wide frequency bands (45 MHz to 600 MHz and 850 MHz to 1.04 GHz), with higher-order low pass filters effectively minimizing spurious emissions for improved signal purity. The system's Switched Controlled enables dynamic selection of frequency bands and filter orders, offering significant flexibility. Experimental outcomes reveal substantial spur reduction and exceptional phase noise performance, demonstrating an impressive trade-off be-tween frequency operation, signal integrity, power consumption (1.8 mW), and compactness (0.0023 mm2). This novel SCPLL design showcases potential advancements in synchronization and signal integrity for future communication net-works, marking a significant contribution to PLL technology.

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