FACTA UNIVERSITATIS
Series: **Electronics and Energetics** Vol. 38, Nº 3, September 2025, pp. 375 - 395
https://doi.org/10.2298/FUEE2503375V

Original scientific paper

STRUCTURAL DESIGN AND PERFORMANCE ANALYSIS OF DOUBLE GATE POCKET TFET FOR LOW POWER APPLICATIONS

Manish Verma[1], Pradipta Dutta[1], Arindam Basak[1], Ramesh Kumar Meena[2]

[1]Kalinga Institute of Industrial Technology, Bhubaneswar, Odisha, India
[2]Department of Interdisciplinary Courses in Engineering, Chitkara University Institute of Engineering & Technology, Chitkara University, Punjab, India

ORCID iDs: Manish Verma https://orcid.org/0009-0007-5228-4497
Pradipta Dutta https://orcid.org/0000-0002-2518-2184
Arindam Basak https://orcid.org/0000-0003-3943-4415
Ramesh Kumar Meena https://orcid.org/0000-0001-9822-8246

Abstract. *This research investigates Tunnel Field Effect Transistors (TFETs), a paradigm shift in low-power electronics, leveraging band-to-band tunneling for superior subthreshold slope and reduced power dissipation compared to conventional MOSFETs. We elucidate the underlying physics of TFET operation, analyzing the interplay between device geometry, material properties, and band structure engineering. A comprehensive analysis of key performance metrics, including on-current, off-current, and subthreshold swing, is conducted, considering the impact of critical device parameters. Furthermore, this work presents a novel vertical TFET architecture demonstrating enhanced performance and scalability compared to conventional planar devices. The vertical structure minimizes parasitic resistances and enables efficient band-to-band tunneling, leading to significant improvements in device characteristics. Challenges associated with both conventional and vertical TFETs, including material integration and performance limitations, are critically examined alongside potential mitigation strategies. The potential applications of TFETs are explored across diverse domains, including low-power digital circuits, RFICs, and neuromorphic computing, highlighting their significance in addressing the escalating demand for energy-efficient electronics in the era of AI and IoT. Finally, future research directions, emphasizing the need for interdisciplinary collaboration and innovative approaches to materials, device engineering, and circuit design, are outlined to unlock the full potential of TFETs in shaping the future of electronics.*

Key words: *TFET, MOSFET, DG-TFET, Junction less TFET, Doping less PNPN TFET, LVTSCR (Low-Voltage Trigger SCR)*

Received November 16, 2024; revised January 12, 2025 and February 12, 2025; accepted February 19, 2025
Corresponding author: Ramesh Kumar Meena
Department of Interdisciplinary Courses in Engineering, Chitkara University Institute of Engineering & Technology, Chitkara University, Punjab, India
E-mail: rameshkumarmeena@gmail.com

1. INTRODUCTION

Conventional Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs), the cornerstone of modern electronics, face increasing challenges in meeting the ever-growing demand for low-power and high-performance devices. As device dimensions shrink towards the nanoscale, MOSFETs encountering limitations such as short-channel effects and an approaching the fundamental limit to their subthreshold slope, hindering further improvements in energy efficiency. To overcome these limitations, Tunnel Field-Effect Transistors (TFETs) have emerged as a promising alternative [1,2,3].

Unlike MOSFETs, which rely on thermal activation to generate carriers, TFETs leverage band-to-band tunneling, a quantum mechanical phenomenon, to facilitate electron transport across the semiconductor bandgap. This mechanism enables steeper subthreshold slopes and lower power consumption compared to conventional MOSFETs. The concept of utilizing tunneling for transistor operation dates back to the 1990s. Decades of research have led to significant advancements, including the development of experimental prototypes and a deeper understanding of the underlying tunneling physics. Early prototypes faced challenges such as low on-state currents and complex fabrication processes. However, persistent research efforts have resulted in improved designs with sharper subthreshold slopes and reduced power consumption [1,3,4].

Recent years have witnessed a surge in research activities focused on addressing critical issues such as temperature sensitivity, on-state current limitations, and scalability challenges. Advanced TFET designs, incorporating novel materials and device architectures, hold significant promise for future low-power and energy-efficient electronics. Collaborative efforts are ongoing to optimize TFET performance and integrate them into various semiconductor applications, paving the way for a new era of energy-efficient and high-performance electronics [1, 2, 3, 4].

TFET emerged in the early 1990s as a potential solution to overcome the limitations of conventional MOSFETs, namely high power consumption and shallow subthreshold slope [1]. TFETs leverage band-to-band tunneling, a quantum mechanical phenomenon, to facilitate efficient electron transport across the semiconductor band-gap. Decades of advancements have led to experimental prototypes and a deeper understanding of tunneling physics [2].

The primary goal of TFET research is to enhance the device performance and reliability through the optimization of material properties, device configurations, and fabrication methods. The initial prototypes face challenges such as low on-state currents and complex fabrication processes. However, persistent research efforts have resulted in improved designs with sharper sub-threshold slopes and reduced power consumption [5, 6]. The investigation into using quantum tunneling to enhance transistor performance began in the 1990s. The 2000s witnessed significant theoretical work to understand tunneling physics and TFET operation, culminating in the demonstration of practical prototypes. In the 2010s, experimental validation and production of TFETs showcased their potential for lower operational voltages and improved sub- threshold characteristic compared to MOSFETs [7].

In recent years, TFET research has focused on addressing temperature sensitivity, on-state currents and scalability issues. Advanced TFET designs hold promise for future low-power and energy efficient devices [8]. Collaborative efforts are ongoing to optimise TFET performance and integration across various semiconductor applications as technology continues to evolve [9].

Table 1 Comparison between MOSFET and TFET

Feature	MOSFET	TFET
Operating Principle	Carrier transport via thermal excitation over a potential barrier	Carrier transport via quantum-mechanical tunneling through the bandgap
Subthreshold Slope (SS)	Typically > 60mV/decade	Theoretically < 60 mV/decade, enabling steeper switching
On-State Current	Generally higher than TFETs	Can be lower than MOSFETs, depending on design
Leakage Current	Higher than TFETs in the off-state	Lower than MOSFETs in the off-state
Power Consumption	Higher due to larger subthreshold swing	Lower due to steeper subthreshold swing
Material Requirements	Mature Si-based technology readily available	Requires precise control of bandgap and interface properties
Manufacturing Complexity	Relatively mature and well-established	More challenging due to precise control of tunneling junctions and interfaces
Temperature Dependence	Moderate temperature sensitivity	More sensitive to temperature variations
Scalability	Highly scalable with current CMOS technology	Scaling challenges related to maintaining tunneling efficiency at smaller dimensions
Applications	High-performance computing, digital logic, analog circuits	Low-power electronics, IoT devices, wearable technology

2. Literature Review

Research on TFETs primarily focuses on analyzing there unique quantum tunneling characteristics and their potential impact on future semiconductor technologies. Extensive investigations have been conducted to delve into the fundamental physics governing TFET operation, including the mechanisms of band-to-band tunneling and the interplay between material properties and device performance. Literature highlights the challenges associated with designing TFETs, such as achieving high on- state currents, mitigating temperature sensitivity, and enhancing material heterostructures to bolster tunneling efficiency. Researchers have explored various TFET configurations, including both homogeneous and heterogeneous architectures, as well as the integration of novel materials such as III-V compounds and 2D materials [11]. This body of research significantly advances our understanding of TFETs and propels the exploration of innovative methodology to optimize their utility in semiconductor applications.

Research on TFETs has intensified, driven by their potential to revolutionize low-power electronics through the exploitation of band-to-band tunneling. Extensive investigations have delved into the fundamental physics of TFET operation, including the intricate interplay between device geometry, material properties, and band structure engineering [1, 12, 14, 15, 16]. A key focus of current research is to address the challenges associated with achieving high on-currents while maintaining steep subthreshold slopes [1, 17, 18, 19].

Table 2 Literature Review of Previous Articles

Researcher	Year	Title	Key Findings	Reference
Geege et al.	2023	Vertically-Grown TFETs: An Extensive Analysis	Examines dual-material gate heterojunction V-TFET topologies.	12
Maria Jose et al.	2022	A Novel L-Gate TFET with Improved Performance and Suppressed Ambipolar Effect	Various structures and modeling of TFET.	31
A.K. Singh et al.	2022	GaSb/GaAs Type-II Heterojunction TFET on SELBOX Substrate for Dielectric Modulated Label-Free Biosensing Application	A novel type-II heterojunction TFET for Biosensor Application.	11
N Reddy et al.	2021	TFET Based Biosensors: Recent Advances and Future Prospects on Device Structure and Sensitivity	Review on future application based on TFET.	14
Tripathy et al.	2020	Device and Circuit-Level Assessment of GaSb/Si Heterojunction Vertical Tunnel-FET for Low-Power Applications	Advancement on TFET device with performance.	10
D Barah et al.	2019	TFET on Selective Buried Oxide Substrate with Improved I ON /I OFF Ratio and Reduced Ambipolar Current	Proposed new structure for TFET.	15
S Singh et al.	2018	Vertical TFET Analysis for Excessive Low Power Digital Applications.	Proposed new structure for vertical TFET.	16
Tamak & Mehra	2017	Review on Tunnel Field Effect Transistors (TFET)	Review on TFET.	17
Turkane, Satish	2016	Review of Tunnel Field Effect Transistor (TFET)	Review on TFET.	18
Avei, U et al.	2015	Tunnel field-effect transistors: Prospects and challenges	Prospects and challenges on TFET.	5

Researchers are actively exploring innovative materials and device architectures to enhance tunneling efficiency and mitigate performance limitations. These include the integration of III-V semiconductors, 2D materials, and novel heterostructures [11, 14, 15, 21, 30, 31]. Furthermore, significant progress has been made in understanding the impact of process variations and device-to-device variability on TFET performance [21, 22, 30]. Recent studies have also highlighted the crucial role of advanced fabrication techniques and process optimization in ensuring the scalability and manufacturability of TFETs for large-scale integration [1, 12, 15]. While significant advancements have been made, challenges remain in achieving consistent and reliable TFET operation, including the suppression of leakage currents and the optimization of device stability [1, 19, 20]. Continued research efforts are essential to fully realize the potential of TFETs in future low-power electronics applications, such as mobile devices, IoT devices, and high-performance computing systems.

Reviews of the literature emphasize the crucial role of sophisticated fabrication methods and process optimization in ensuring the scalability and reproducibility of TFETs in real-world applications. Overall, while TFET technology holds significant promise for enabling energy-efficient electronics, further research is needed to overcome the remaining obstacles and fully realize its practical potential.

3. TFET Device Physics and Operation

Tunnel Field-Effect Transistors (TFETs) operate on the principle of band-to-band tunneling, enabled by their low bandgap semiconductor material. Their physics and operation are governed by intricate quantum mechanics. Key aspects include the tunneling mechanism, subthreshold behavior, gate control and voltage characteristics, band engineering, temperature sensitivity, and on-state current and efficiency. Understanding these properties is essential for optimizing TFET performance and applications across various fields [19-25].

Band-to-band tunneling (BTBT) is a quantum phenomenon where charge carriers traverse a semiconductor's energy bandgap, crucial for TFET operation. BTBT allows current flow by enabling carriers to tunnel through the bandgap, significantly impacting device conductance and current flow. TFET performance relies heavily on efficient BTBT control and engineering, guiding research to enhance TFET functionality for improved electronic applications [26].

Subthreshold swing is a critical parameter for evaluating transistor energy efficiency and switching behavior, particularly in TFETs. It measures how quickly the subthreshold current changes with gate voltage. TFETs, with their intrinsic band-to-band tunneling, can achieve a sharper subthreshold swing compared to MOSFETs, allowing operation at lower voltages and reduced power consumption. Optimizing TFET band structure, interfaces, and materials is crucial to minimize subthreshold swing, enhancing overall energy efficiency and performance in various electronic applications [27, 28].

4. TFET Application and Challenges

Tunnel field effect transistors (TFETs) are a promising alternative to traditional transistors in the electronics industry, offering superior performance and reduced power consumption. TFETs are particularly well suited for low-power integrated circuits, especially in energy-constrained devices such as wearable electronics and Internet of Things sensors. Their ability to operate at lower voltages and with a reduced subthreshold swing enables energy-efficient circuit designs, potentially extending battery life and improving device longevity. Additionally, TFETs show promise for high-frequency applications, addressing challenges such as heat dissipation and leakage currents, which could revolutionize high-speed, low-power communication systems.

However, integrating TFETs with existing CMOS technology remains a significant challenge, requiring innovative solutions for seamless integration into current manufacturing processes. Collaborative efforts between researchers and industry experts are essential to overcome these obstacles and establish TFET technology as a viable and scalable alternative for future electronic applications.

5. Various TFET Structures

Tunnel Field-Effect Transistors (TFETs) come in different configurations, each designed to optimize specific performance aspects. Heterogeneous TFETs integrate diverse materials or heterostructures to enhance tunneling efficiency, while homogeneous TFETs utilize uniform semiconductor materials, simplifying production.

III-V TFETs incorporate compound semiconductor materials such as gallium arsenide (GaAs), known for their high electron mobility, making them suitable for high-speed applications. 2D material TFETs employ atomically thin materials such as graphene or transition metal chalcogenides, offering flexibility and transparency for innovative device applications. Nanowire TFET utilize semiconductor nanowires to enhance electrostatic control and scalability, making them ideal for advanced technology nodes. Each TFET structure offers unique advantages and is tailored to meet specific application requirements, showcasing the ongoing innovation and versatility of TFET technology [18].

6. TFET SIMULATION

TFET simulation, essential for advancing Tunnel Field Effect Transistors (TFETs), involves modeling the intricate quantum tunneling mechanisms that govern their operation. By predicting key device properties such as on-state current, off-state leakage, and subthreshold swing, simulations offer valuable insights into TFET performance.

Table 3 Various TFET Structures

TFET Structure	Description	Advantages	Application
Surface TFET	Junction between n-type and p-type semiconductors.	Low-power, high-speed.	High-speed, low-power devices.
Gate-all-around TFET	Gate surrounds the channel.	Improved performance, reduced leakage.	Optoelectronic devices.
Feedback TFET	Source and drain regions swapped.	Enhanced efficiency, reduced leakage.	Signal oscillators, amplifiers.
Vertical TFET	Channel oriented vertically.	Higher drive current, reduced leakage.	High-Speed Communication 5G/6G, Data Centres
Double-gate TFET	Two gates control the channel.	Improved performance, reduced leakage.	High-density integrated circuits.
PNPN TFET	Four layers of doping.	Reduced short-channel effects, better reliability.	High-speed digital, RF devices.
Junctionless TFET	No distinct junction between source, channel, and drain.	Reduced short-channel effects, better scalability.	Low-power, high-speed devices.
Asymmetric TFET	Source and drain regions have different doping profiles.	Enhanced performance, reduced leakage.	High-Speed Communication Circuits., Low Power Electronics
Asymmetric gate TFET	Gate has different doping profiles on source and drain sides.	Improved performance, reduced leakage.	Analog and Mixed Signal Circuits
Gate-workfunction-engineered TFET	Gate material or doping is engineered to optimize performance.	Enhanced performance, reduced leakage.	Analog and Mixed Signal Circuits
Triple-gate TFET	Three gates control the channel.	Improved performance, reduced leakage.	High Speed Processors, Data Centres, Supersomputers

The TFET simulation was performed using Silvaco T-CAD in a 2D framework. The device characteristics were analyzed by incorporating key physical models, including

Band-to-Band Tunneling, Drift-Diffusion, and Poisson's Equation, while employing Fermi-Dirac Statistics to account for carrier distributions. To simplify the computational complexity, the Effective Mass Approximation was utilized. Optionally, the Non-Parabolic Band Structure and Hydrodynamic Model could be included for more accurate results.

Also, modeling tools facilitate the exploration of various material compositions and structural modifications, contributing to the development of more reliable and efficient TFETs. Thermal simulations further enhance our understanding by elucidating temperature distributions and informing thermal management strategies, thereby bolstering TFET reliability. Through TFET device simulations, we can obtain valuable parameter results, as shown in Fig. 1 to 11.

The illustrated TFET device is designed, Fig 1, for low-power applications by leveraging quantum tunneling for switching on and off.

1.1. Key Components and Operation

- Source and Drain Regions: The source is heavily doped with p-type material, and the drain is heavily doped with n-type material. This p-i-n structure is crucial for tunneling.
- Channel Region: The intrinsic (lightly doped or undoped) channel is 10 nm thick, ensuring efficient tunneling while maintaining sufficient gate control.
- Gate Structure: The double-gate structure (Gate 1 and Gate 2) enhances electrostatic control over the channel and the tunneling junction. Gate 1 is 20nm thick, and Gate 2 is 2nm thick.
- Oxide Layer (SiO_2): The 5nm thick silicon dioxide layer acts as an insulator, preventing direct current flow between the gate and the channel, ensuring gate control over the channel.

For describing the behaviour of the simulated Tunnel Field-Effect Transistors (TFETs) device structure, a set of equations is derived as such:

Table 4 Simulation parameters for the simulated TFET Device

Parameters	Simulated TFET
Channel Length (L_{ch})	10nm
Gate Length (L_G)	20nm
Source/Drain Extension Length (L_{ext})	2nm
Source/Drain Junction Depth (X)	20nm
Gate Oxide Thickness (t_{ox})	3nm
Channel Thickness (t_{ch})	5nm
Pocket Depth (X_p)	3nm
Substrate Thickness (T_{sub})	10nm

7. Simulated TFET Structure Operation

Off-State: In the off-state, the energy bands of the source and channel are misaligned due to the absence or minimal application of gate voltage. This misalignment results in a wide tunneling barrier, preventing carriers from tunneling through the channel and maintaining the device in a non-conducting state.

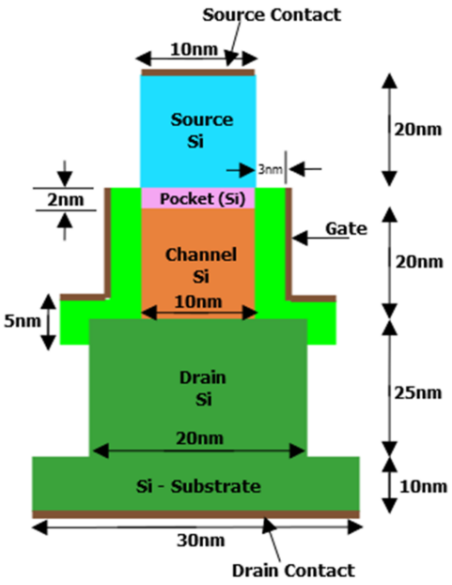

Fig. 1 Simulated TFET Device Structure

On-State: When a sufficient gate voltage is applied, the energy barrier between the source and the channel is reduced. This realignment allows carriers to tunnel from the valence band of the source to the conduction band of the channel. The thin channel (10 nm) and precise gate control facilitate this tunneling process, enabling current to flow from the source to the drain.

The TFET structure depicted combines a carefully designed channel, source, and drain regions with double-gate to effectively control quantum tunneling. This design offers significant advantages for low-power, high-efficiency electronic applications, making it a promising technology for future semiconductor devices.

The Current Flow lines graph in Fig. 2 illustrates the spatial distribution of current flow lines within a simulated TFET device. The peak near the beginning of the channel (around 0.02microns) indicates efficient tunneling from the source to the channel, suggesting a strong overlap between the wave-functions of the source and channel states.

As the current flows through the channel, it experiences variations due to factors such as potential barriers, scattering effects, and the presence of defects or impurities. The decrease in current flow lines towards the end of the channel (around 0.10 microns) might suggest potential current leakage or scattering effects, which can impact the device's overall performance.

The overall shape of the curve provides valuable insights into the carrier transport mechanisms and potential bottlenecks within the TFET device. Noteworthy features include a sharp peak in current flow lines, likely indicating the tunneling junction, and a region of reduced current flow, potentially attributed to a local potential barrier or charge trapping. A more pronounced peak in the current flow lines would indicate a more efficient tunneling process, while a flatter curve or multiple peaks might suggest variations in the channel's potential profile or the presence of defects. By analyzing the current flow lines, researchers can identify areas of high current concentration, potential leakage paths, and regions where device optimization might be necessary to improve performance and efficiency.

The Charge and Donor Concentration graph, shown in Fig. 3 below, illustrates the distribution of charge carriers and donor atoms within the TFET structure. The blue line represents the charge concentration, and the red line represents the donor concentration.

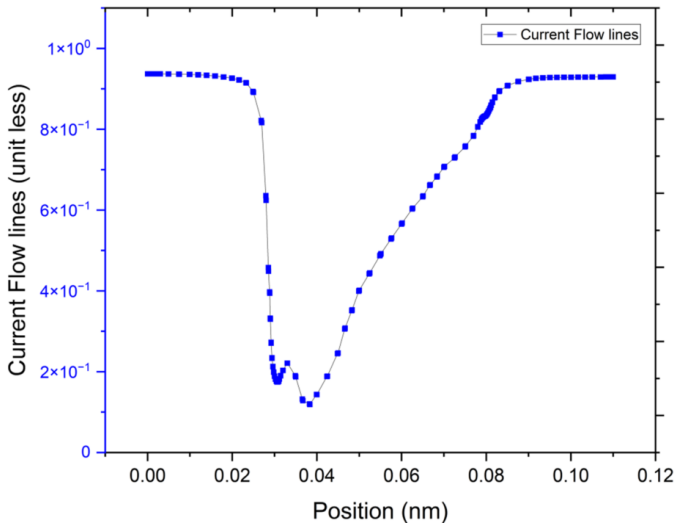

Fig. 2 Graph illustrating the variation of Current Flow Lines within a simulated Tunnel Field Effect Transistor (TFET) device The peak in current flow lines occurs as of the active tunneling region where electrons quantum-mechanically tunnel through the bandgap.

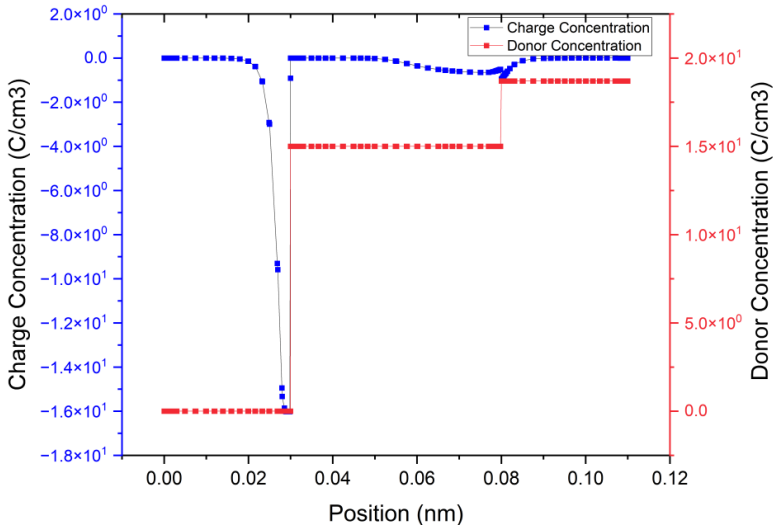

Fig. 3 Graph illustrating the distribution of Charge Concentration and Donor Concentration for a simulated TFET device. The blue line represents the Charge Concentration, while the red line represents the Donor Concentration. The x-axis represents the position along the device channel, measured in nanometers (nm).

In the source region, a high donor concentration and negative charge concentration indicate heavy n-type doping and a depletion region, respectively. The channel region exhibits a lightly doped or intrinsic nature with a near-zero charge concentration. In the drain region, a high donor concentration and positive charge concentration suggest heavy n-type doping and an accumulation region. Negative values for Charge Concentration signify an accumulation of electrons, while positive values suggest a depletion of electrons or the presence of holes. This graphical representation offers valuable insights into the device's charge distribution and the influence of doping on its characteristics. The sharp transition in Charge Concentration suggests the presence of a p-n junction or a Schottky barrier. The profile of the Donor Concentration highlights the role of doped regions in governing the device's electrical behavior.

$$E = -\nabla\psi \tag{1}$$

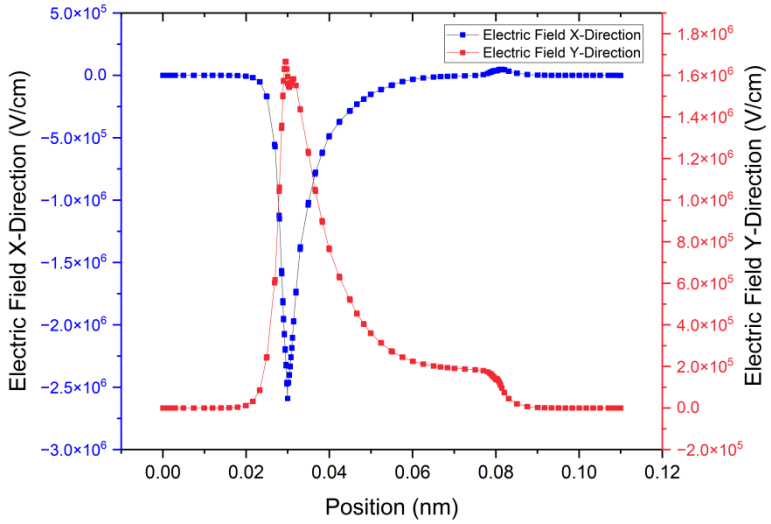

Fig. 4 Graph illustrating the spatial variation of Electric Field components (X and Y directions) within a TFET. X-Direction field shows a sharp peak (~ 1.8×10^6 V/cm), indicative of the tunneling junction. Y-Direction field exhibits a smaller magnitude and likely influences lateral carrier transport.

The Electric Field graph, as shown in Fig. 4, illustrates the distribution of the electric field within a simulated TFET structure. In the source region, a strong perpendicular electric field (Y-direction) is observed, primarily attributed to the p-n junction at the source-channel interface. Conversely, the X-direction electric field remains minimal. Within the channel, the Y-direction electric field gradually decreases, while the X-direction field increases, facilitating efficient carrier transport. In the drain region, the Y-direction electric field becomes negligible, and a strong X-direction field is present due to the p-n junction.

The increasing X-direction field in the channel enhances carrier transport, contributing to overall device performance. The low Y-direction field in the drain region helps to reduce leakage current and improve device characteristics.

The Recombination Rate graph shows the spatial distribution of electron-hole recombination events within the TFET, providing insights into potential leakage paths and performance limitations, as shown in Fig. 5.

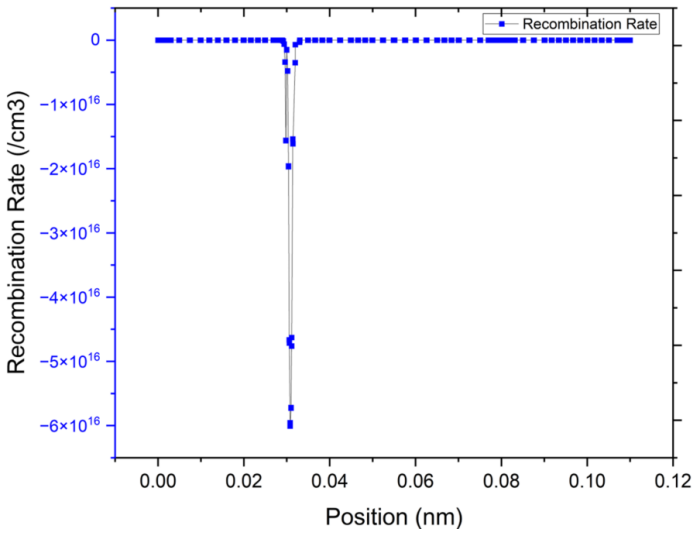

Fig. 5 Graph illustrating the spatial variation of Recombination Rate within a TFET. A sharp peak in recombination rate (~ -5x10^6 /cm^3) is observed, indicating a region of high carrier recombination activity, likely influenced by localized defects or carrier trapping.

The graph shows a sharp peak in the recombination rate at a specific position along the channel. This peak is such a-sly due to the presence of a potential barrier or a region of high electric field within the TFET. In this region, electrons and holes have a higher probability of encountering each other and recombining. The recombination rate is negative in most regions of the channel, indicating that generation is dominant over recombination.

$$R = \frac{np - n_i^2}{\tau_p \left(n + n_1\right) + \tau_n \left(p + p_1\right)} \tag{2}$$

where, R is recombination rate which describes the rate of electron-hole recombination with n_i as intrinsic carrier concentration, τ_n, τ_p are the carrier lifetimes for electronics and holes and n_1, p_1 are the parameters related to the trap states.

Meanwhile, the Electron Velocity graph illustrates the magnitude and distribution of electron velocities, revealing the efficiency of carrier transport and potential hot carrier effects that may impact device reliability, as shown in Fig. 6 and Fig. 7.

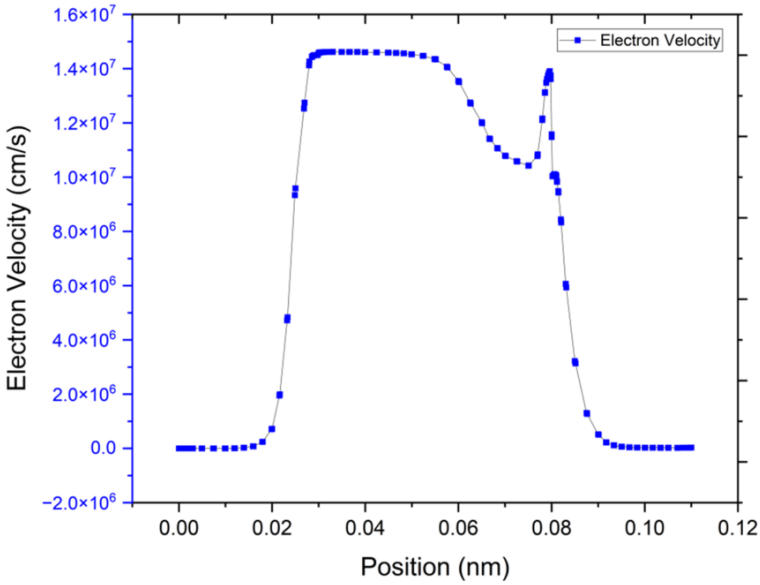

Fig. 6 Graph illustrating the spatial variation of Electron Velocity within a Tunnel Field Effect Transistor (TFET) device. A sharp peak in electron velocity (~1.5x10^7 cm/s), indicating the tunneling junction, and regions of reduced velocity, potentially attributed to carrier scattering or variations in the electric field.

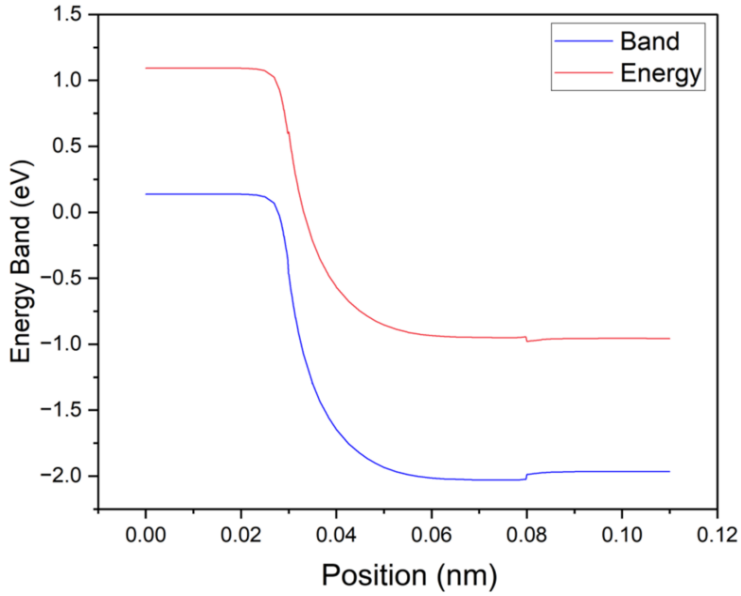

Fig. 7 Energy Band Diagram for the simulated TFET device. The band bending shows a significant potential drop (~1.5eV) across the tunneling junction, enabling band-to-band tunneling.

The peak in electron velocity near the source junction is a well-established phenomenon in semiconductor devices, resulting from several factors. Initially, a strong electric field gradient at the source-channel interface imparts significant kinetic energy to the injected electrons, resulting in a rapid increase in their velocity. However, as these charge carriers traverse the channel, they undergo scattering events with phonons and impurities, leading to energy dissipation and ultimately limiting their maximum achievable velocity. In short-channel devices, the constrained channel length may not afford sufficient distance for the electron velocity to attain steady-state conditions. Furthermore, non-uniform doping profiles within the channel can introduce spatial variations in the electric field and carrier mobility, further influencing the observed velocity distribution. The specific characteristics of the device, including its geometry, material properties, and operating conditions, exert a significant influence on the observed electron velocity profile.

The energy band graph illustrates the variation of conduction band energy and valence band energy along the channel of a TFET. The x-axis represents the position along the channel, measured in microns, while the y-axis represents the energy level, measured in electron volts (eV). We can see at the source region, the conduction band edge is significantly lower than the valence band edge, creating a deep potential well. This well attracts electrons from the source region, making them available for tunneling.

Also, there is a band-bending at 0.038 micron which occurs when there is a shift from the drain to the gate source channel of the simulated TFET device.

Fig. 8 illustrates the relationship between the applied gate voltage and a key performance metric of the TFET device, such as drain current, transconductance, or subthreshold swing. This graph is crucial for understanding the device's switching behavior, the modulation of the tunneling barrier, and the gate's overall control over the TFET's operation. The presented graph illustrates the transfer characteristics of a Tunnel Field-Effect Transistor (TFET) device, depicting the relationship between the applied Gate Voltage and the resulting Drain Current and Total Current. A salient feature of this graph is the abrupt increase in both currents at a specific threshold voltage, a characteristic behavior associated with TFETs where the dominant conduction mechanism is band-to-band tunneling. The slope of the curves in the subthreshold region, prior to the sharp transition, is notably steep, signifying enhanced control over the device's on/off states. A subtle offset is observed between the Drain Current and the Total Current, indicating the presence of leakage currents within the device, which can originate from sources such as reverse bias tunneling or surface leakage phenomena.

The Total Current graph shows the overall current flowing through the TFET device as a function of applied bias conditions, such as gate voltage or drain voltage, providing a comprehensive view of the current-voltage characteristics in both on-state and off-state regimes. By analyzing the Total Current profile, key performance metrics such as the on/off current ratio, subthreshold swing, and overall drive current capability can be determined, which are essential for evaluating the TFET's performance and its suitability for low-power applications.

$$I_D = I_0 \exp\frac{qV_{GS}}{k_B T}\left(1 - \exp\frac{-qV_{GS}}{k_B T}\right) \tag{3}$$

The presented equation, offers a simplified representation of the drain current (ID) within a Tunnel Field-Effect Transistor (TFET). This highlights the significant influence

of gate-source voltage (VGS) and drain-source voltage (VDS) on the device's current flow. The term '$\exp\frac{qV_{GS}}{k_BT}$' underscores the exponential relationship between current and gate voltage, a hallmark of tunneling-based devices. The term '$\left(1-\exp\frac{-qV_{GS}}{k_BT}\right)$' accounts for the impact of drain voltage on the current. It is important to note that this simplified model may not fully capture the intricate physics governing TFET operation, such as band-to-band tunneling (BTBT) phenomena, quantum mechanical effects, and the influence of device geometry.

$$S = \frac{dV_{GS}}{d\left(\log_{10} I_D\right)} \tag{4}$$

$$g_m = \frac{dI_D}{dV_{GS}} \tag{5}$$

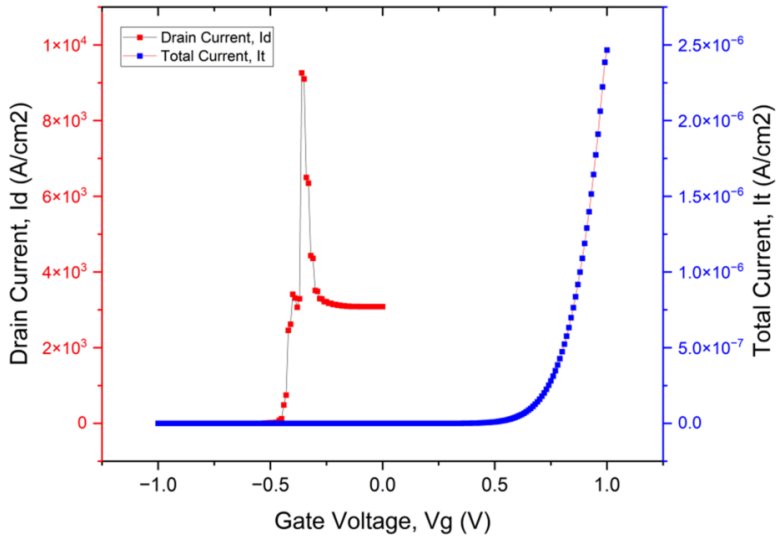

Fig. 8 Current Vs Voltage diagram for the simulated TFET device. Drain Current (Id) exhibits a steep subthreshold slope (~60mV/dec) and a peak current density of 1x10^4 A/cm^2. Total Current (It) shows a slight offset due to leakage currents.

The BBT E-Tunneling and H-Tunnelling Rate graph, as shown in Fig.9, represent the distribution of the band-to-band tunneling rates for electrons and holes, respectively, within the TFET structure. This graphs provide insights into the regions where efficient band-to-band tunnelling occurs, enabling the injection of charge carriers from the source to the channel and subsequently to the drain. The Conduction Current Density graph illustrates the spatial distribution and magnitude of the current density flowing through the TFET device structure under operational conditions, such as shown in Fig. 10. This graph provides valuable information about the regions contributing to the overall device current, as well as potential areas of high current crowding or leakage paths. By analyzing the

conduction current density profile, one can gain insights into the effectiveness of the tunneling process, the uniformity of carrier transport, and the overall efficiency of the TFET in terms of its on-state performance and switching characteristics Fig. 11.

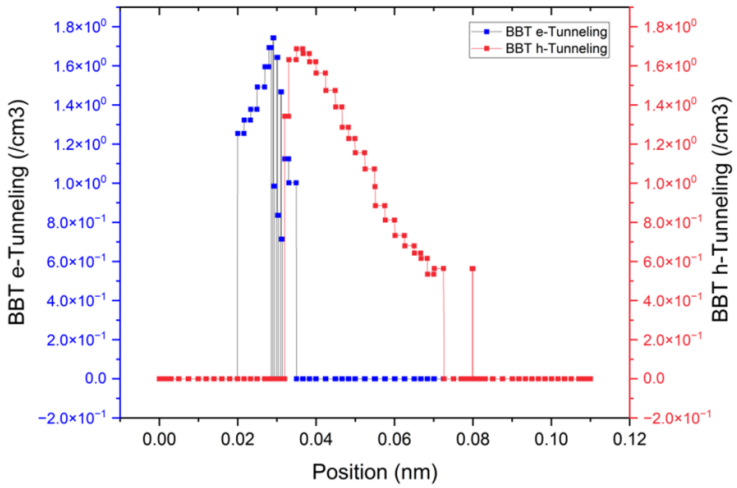

Fig. 9 Graph illustrating theBand-to-Band Tunneling (BBT) rates for electrons (e-Tunneling) and holes (h-Tunneling) within a TFET. Peak e-Tunneling rate (~1.6x10^9 /cm^3) occurs at ~0.04 nm, while h-Tunneling peak is lower and shifted slightly.

The graph shows that the majority of the current flow in the TFET occurs near the source region, where the tunneling probability is highest. As electrons move towards the drain, the tunneling probability decreases, leading to a reduction in current density. The presence of a negative current region might indicate potential issues or limitations in the device's performance.

$$G_{BTBT} = A.E^2 \exp\left(-B / E\right) \tag{6}$$

The graph shows that the majority of the current flow in the TFET occurs near the source region, where the tunneling probability is highest. As electrons move towards the drain, the tunneling probability decreases, leading to a reduction in current density. The graph displays the total current density as a function of position within a Tunnel Field Effect Transistor (TFET). The graph exhibits regions with negative current density values because of factors like under strong reverse bias conditions, electrons tunnel from the valence band of the drain to the conduction band of the source, leading to a reverse current flow. This reverse tunneling current opposes the conventional forward current, resulting in negative current density values. Moreover, the presence of trapped charges within the channel region also contributes to the localization of negative current densities. Finally, TFETs operate on a different principle, leveraging band-to-band tunneling. This quantum mechanical phenomenon allows electrons to tunnel through the energy barrier (bandgap) of the semiconductor material.

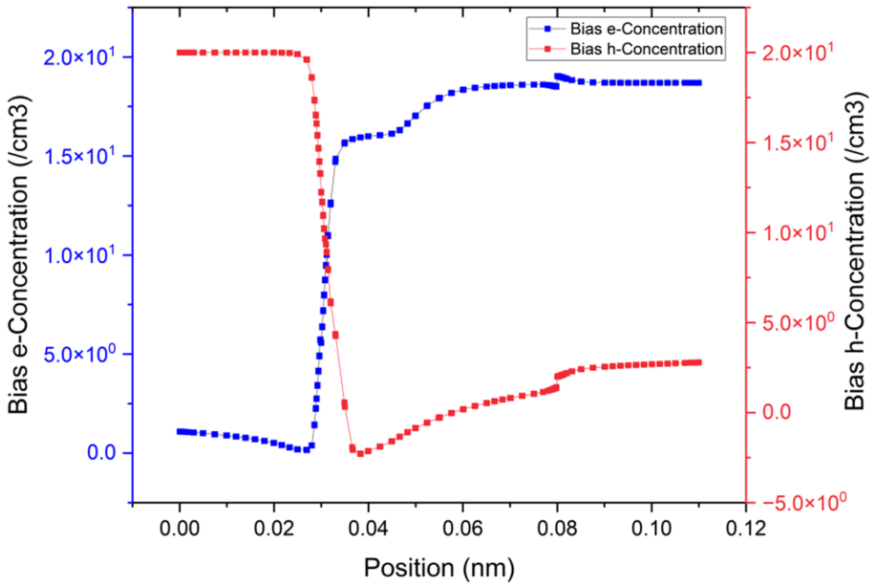

Fig. 10 Bias e-Concentration and h-Concentration diagram for the simulated TFET device. The plot shows a significant accumulation of electrons (e-Concentration) and a depletion of holes (h-Concentration) near the tunneling junction, indicating band bending and carrier separation.

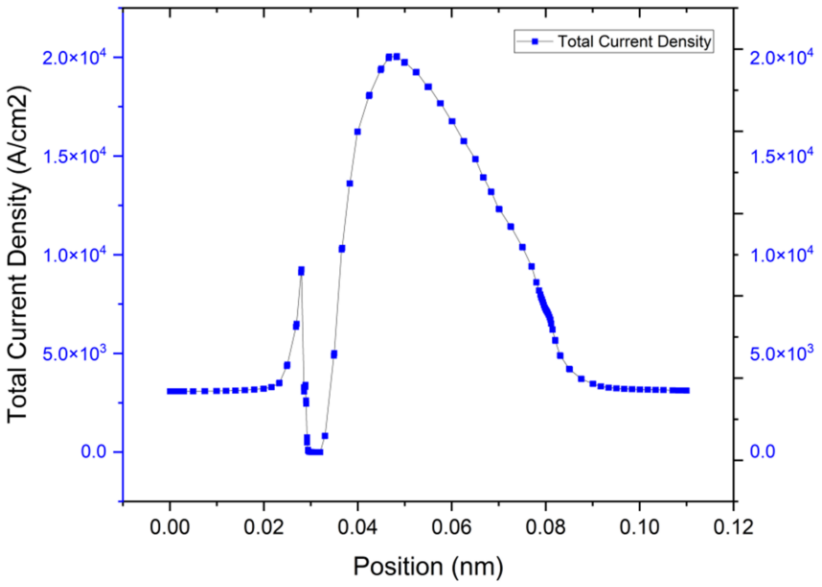

Fig. 11 Total Current Density diagram for the simulated TFET device

8. KEY OBSERVATIONS AND FINDINGS

The provided simulation results offer valuable insights into the operation and performance of a simulated TFET device. By examining the various graphs, we can understand the distribution of electron velocity, carrier concentrations, recombination rate, electric field, and tunneling rates within the TFET. Further optimization of the TFET structure, materials, and operating conditions can lead to even better performance.

The electron velocity profile shows efficient acceleration near the source, while the total current density peaks at the source region. Carrier concentration analysis reveals a depletion region near the source and drain, and a higher concentration of electrons in the channel. The recombination rate is low, indicating minimal electron-hole pair annihilation. The electric field is concentrated near the source and drain, driving electron transport. Tunneling rates are higher for electrons, suggesting efficient tunneling from source to drain. These findings highlight the potential of TFETs for low-power, high-performance applications. Future optimization and detailed analysis can further improve device performance.

9. TFET MODELING

To understand TFETs for ultra-low-power devices, we must delve into the intricate world of BTFET modeling which involves constructing complex mathematical frameworks to simulate the quantum mechanical phenomena underlying TFET operation. These models shed light on the band-to-band tunneling pathways and their influence on device performance by examining tunneling processes.

Moreover, TFET modeling characterizes carrier transport behaviors, heterostructure configurations, and material properties, all of which are critical factors in determining TFET operating features. By integrating these elements, TFET modeling predicts crucial device metrics such as energy efficiency and guides the optimization of TFET design for future energy-efficient electronic applications.

The fabrication of Tunnel Field-Effect Transistors (TFETs) involves a complex series of steps utilizing advanced techniques. Substrate preparation, often using silicon or III-V compounds, is crucial for device performance. Layer deposition, including the semiconductor channel and gate insulator, is achieved through precise methods such as CVD and MBE to ensure optimal material quality.

Engineering material interfaces and heterostructure is essential for achieving desired tunneling characteristics. Doping techniques are employed to create source and drain regions with specific doping profiles, ensuring optimal device functionality. Advanced lithography and etching techniques are used to define the device dimensions and patterns.

To enhance TFET performance and reliability, thermal treatments and annealing stages are implemented to improve material quality, activate dopants, and alleviate process-induced stresses. Rigorous quality control and alignment methods are essential throughout the fabrication process to ensure consistency and uniformity. These steps are crucial for producing high-performance TFETs suitable for various high-speed and low-power electronic applications.

10. DISCUSSION

TFET and MOSFET are prominent semiconductor devices with distinct characteristics. MOSFETs employ gate voltage control to regulate channel conductivity, while TFETs utilize quantum tunneling for efficient current flow. TFETs offer a steeper sub-threshold slope, leading to lower power consumption, but their on-state current may be limited compared to MOSFETs. TFET performance is influenced by material properties and heterostructure, making them susceptible to temperature variations.

MOSFETs excel in high-performance applications due to their robust on-state current and well-established manufacturing processes. TFETs, on the other hand, are increasingly favored in ultra-low-power electronics for their exceptional energy efficiency and ability to operate at lower supply voltages. To compete effectively in high-performance environments, ongoing research is essential to address TFET limitations and enhance their performance benchmarks.

A variety of TFET variations, including mixed TFETs, III-V TFETs, 2D material TFETs, and nanowire TFETs, offer unique advantages. Understanding these variations is crucial for optimizing TFET designs to meet specific application requirements and drive advancements in high-performance electronic devices.

The simulated TFET structure device exhibits several novel features, including a double-gate configuration with independent control of each gate, a pocket region beneath the channel for potential modulation, an ultra-thin 2nm gate oxide for enhanced electrostatic control, and a 10nm channel length that pushes the boundaries of device scaling. This combination of design elements presents a unique approach to TFET design, potentially offering improved performance metrics such as steeper subthreshold slopes and higher on-currents. Going forward a thorough simulation and analysis are required to fully evaluate the impact of these features on device performance and to assess the feasibility of fabricating such a device.

While the simulated TFET structure with its nanoscale dimensions presents challenges, these challenges also serve as opportunities for innovation and advancement in semiconductor technology. The pursuit of overcoming these limitations, such as minimizing gate leakage through advanced gate dielectric materials and optimizing channel engineering to mitigate short-channel effects, will drive significant research and development efforts. Addressing these challenges will not only lead to improved TFET performance but also pave the way for the development of novel materials and fabrication techniques with broader applications in nanoelectronics.

The simulated TFET structure, with its 2nm gate oxide and 10nm channel length, serves as a compelling platform for further research and development. The challenges which may be associated with the simulated device, including gate leakage and short-channel effects, present opportunities for innovation in materials science, device engineering, and fabrication techniques. These challenges can drive the development of novel gate dielectric materials, advanced channel engineering techniques, and improved process control to overcome these limitations and realize the full potential of TFETs.

Tunneling in TFETs primarily relies on BTBT, where electrons directly traverse the energy barrier between the valence and conduction bands due to a strong electric field. However, other mechanisms also influence tunneling. Trap-Assisted Tunneling (TAT) occurs through localized energy states within the bandgap created by defects, affecting current flow. Phonon-Assisted Tunneling involves interactions between electrons and

lattice vibrations, impacting tunneling probability. At high electric fields, Impact Ionization generates electron-hole pairs, further contributing to the tunneling current. These combined mechanisms determine the overall tunneling current in TFETs and significantly impact their performance characteristics. TFET performance hinges on a delicate interplay of material properties and device engineering. Bandgap, heterojunction band offsets, and dielectric constants dictate tunneling probability and current drive. Meanwhile, channel length, gate geometry, and strain engineering sculpt the electric field, guiding tunneling paths and optimizing metrics like subthreshold swing and on/off current. Striking the right balance between material selection and device architecture is key to unlocking TFET's full potential.

TFETs significant advantages of the various practical applications. In medical wearable devices like glucose monitors, ECG, EEG, EMG monitoring machines, they provide ultra-low power consumption, extending battery life. For implantable medi-cal devices such as pacemakers and others devices, TFETs allow low-voltages op-eration, minimizing heat generation for safe use on the human body or others ob-jects. In IoT sensors for smart homes and environmental monitoring, TFETs ensure energy efficiency, supporting long-lasting battery operation. Mobile processors in smartphones benefit from reduced power consumption in both active and standby mode, battery life. Data centers uses TFET to reduce static power, lowering opera-tional cost. In non-volatile memory, TFETs enable low-energy read/write cycles, while in flexible electronics like e-skins and bendable displays, TFETs maintain me-chanical flexibility. Biomedical research tools, like DNA sequencers, leverage TFETs' low-voltage operation for sensitive measurements. High-frequency commu-nication devices for 5G benefits by TFETs' efficient switching, while ultra-low-power analog circuits in hearing aid optimize energy use. Finally, space application use TFET in low-power, heat-efficient circuits for energy-constrained environments.

Table 5 Comparison between Existing TFET structure and Simulated TFET structure

Parameter	Simulated TFET	Typical/Existing TFET
Source/Drain Extension Length	2nm	2-5nm
Pocket Region	3nm	Often present
Channel Length	10nm	5-15nm
Gate Length	20nm	20nm-25nm
Gate Oxide Thickness	3nm	1-3nm
Substrate Thickness	10nm	10-20nm
Material Choice	Si, III-V	Si, Ge, III-V

The simulated TFET device shows several advantages compared to typical/existing TFETs. It features a shorter source/drain extension length of 2nm, which can enhance tunneling efficiency and reduce leakage currents. The pocket region is optimized at 3nm, aiding in better control of the tunneling junction. With a channel length of 10nm and a gate length of 20nm, the device aligns with modern scaling trends, potentially offering improved performance and lower power consumption. The gate oxide thickness of 3nm is within the optimal range, ensuring effective gate control while minimizing leakage. The substrate thickness of 10nm is on the lower end, which can help reduce parasitic capacitance. The use of Si and III-V materials in the simulated TFET suggests a focus on leveraging high mobility and efficient tunneling properties, potentially leading to superior device performance compared to traditional Si or Ge-based TFETs.

ACKNOWLEDGEMENT

The simulation results presented in this analysis provide valuable insights into the operation and performance of a TFET device. The simulated TFET structure, characterized by its unique band-to-band tunneling mechanism, offers significant potential for low-power, high-performance electronic applications, with steeper subthreshold slopes, lower operating voltages, and enhanced energy efficiency over the conventional MOSFETs. However, challenges such as low on-state currents, temperature sensitivity, and material complexities may hinder their widespread adoption in high-performance applications.

Current research focuses on optimizing TFET design through material exploration, heterostructure engineering, and fabrication improvements. TFETs have the potential to become essential components in future energy-efficient electronic devices. While the simulation results are promising, further research and development are necessary to address challenges such as limited on-state current and susceptibility to temperature variations. By optimizing the TFET structure, materials, and operating conditions, researchers can unlock the full potential of this technology for future electronic devices.

REFERENCES

[1] A. Garg, R. K. Ratnesh, R. K. Chauhan, N. Mittal and H. Shankar, "Current Advancement and Progress in BioFET: A Review", In Proceedings of the 2022 International Conference on Signal and Information Processing (IConSIP), Pune, India, 2022, pp. 1-7,

[2] S. Hussain, N. Mustakim, S. Singha and J. K. Saha, "A Comprehensive Study on Tunneling Field Effect Transistor using Non-local Band-to-Band Tunneling Model", *J. Phys.: Conf. Ser.*, vol. 1432, no. 1, p. 012028, 2020.

[3] K. Baral, P. K. Singh, S. Kumar, A. Singh, M. Tripathy, S. Chander, and S. Jit, "2-D Analytical Modeling of Drain and Gate-Leakage Currents of Cylindrical Gate Asymmetric Halo Doped Dual Material-Junctionless Accumulation Mode MOSFET", *AEU – Int. J. Electron. Commun.*, vol. 116, p. 153071, 2020.

[4] U. E. Avci, D. H. Morris and I. S. Young, "Tunnel Field-Effect Transistors: Prospects and Challenges", *IEEE J. Electron Devices Soc.*, vol. 3, no. 3, pp. 88-95, 2015.

[5] N. N. Reddy and D. K. Panda, "A Comprehensive Review on Tunnel Field-Effect Transistor (TFET) Based Biosensors: Recent Advances and Future Prospects on Device Structure and Sensitivity", *Silicon*, vol. 13, pp. 3085-3100, 2021.

[6] K. Baral, P. K. Singh, S. Kumar, M. R. Tripathy, A. K. Singh, S. Chander, and S. Jit, "A 2-D Compact DC Model for Engineered Nanowire JAM-MOSFETs Valid for All Operating Regimes", *Semicond. Sci. Technol.*, vol. 35, no. 8, p. 085014, 2020.

[7] W. Y. Choi, B.-G. Park, J. D. Lee and T.-J. K. Liu, "Tunneling Field-Effect Transistors (TFETs) With Subthreshold Swing (SS) Less Than 60 mV/dec", *IEEE Electron Device Lett.*, vol. 28, no. 8, pp. 743-745, 2007.

[8] Z.-F. Han, G.-P. Ru and G. Ruan, "A Simulation Study of Vertical Tunnel Field Effect Transistors", In Proceedings of the 9th IEEE International Conference on ASIC, Xiamen, China, 2011, pp. 665-668.

[9] N. N. Reddy and D. K. Panda, "A Comprehensive Review on Tunnel Field-Effect Transistor (TFET) Based Biosensors: Recent Advances and Future Prospects on Device Structure and Sensitivity", *Silicon*, vol. 13, pp. 3085-3100, 2021.

[10] A. K. Singh, M. R. Tripathy, K. Baral and S. Jit, "GaSb/GaAs Type-II Heterojunction TFET on SELBOX Substrate for Dielectric Modulated Label-Free Biosensing Application", *IEEE Trans. Electron Devices*, vol. 69, no. 9, pp. 5185-5192, 2022.

[11] A. Sharon Geege and T. S. Arun Samuel, "Vertically-Grown TFETs: An Extensive Analysis", *Silicon*, vol. 15, no. 9, pp. 3783-3796, 2022.

[12] A. M. Jossy and T. Vigneswaran, "A Perspective Review of Tunnel Field Effect Transistor With Steeper Switching Behavior and Low Off Current (IOFF) For Ultra Low Power Applications". *Int. J. Eng. Technol.*, vol. 6, no. 5, pp. 2092-2104, 2014.

[13] M. R. Tripathy, A. K. Singh, K. Baral, P. K. Singh and S. Jit, "III-V/Si Staggered Heterojunction Based Source-Pocket Engineered Vertical TFETs for Low Power Applications", *Superlattices Microstruct.*, vol. 142, p. 106494, 2020.

[14] D. Barah, A. K. Singh, B. Bhowmick, "TFET on Selective Buried Oxide (SELBOX) Substrate with Improved ION/IOFF Ratio and Reduced Ambipolar Current". *Silicon*, vol. 11, no. 2, pp. 973-981, 2018.

[15] S. Singh and B. Raj, "Vertical Tunnel-FET Analysis for Excessive Low Power Digital Applications", In Proceedings of the First International Conference on Secure Cyber Computing and Communication (ICSCCC), Jalandhar, India, 2018, pp. 192-197.

[16] U. E. Avci, D. H. Morris and I. S. Young, "Tunnel Field-Effect Transistors: Prospects and Challenges", *IEEE J. Electron Devices Soc.*, vol. 3, no. 3, pp. 88-95, 2015.

[17] P. Kumar Kumawat, S. Birla, N. Singh, "Tunnel Field Effect Transistor Device Structures: A Comprehensive Review", *Mater. Today*, vol. 79, no. 2, pp. 292-296, 2022.

[18] S. Datta, H. Liu and V. Narayanan, "Tunnel FET Technology: A Reliability Perspective", *Microelectron. Reliab.*, vol. 54, no. 5, pp. 861-874, 2014.

[19] T. Nirschl, S. Henzler, C. Pacha, P.-F. Wang, W. Hansch, G. Georgakos and D. Schmitt-Landsiedel, "The Tunneling Field Effect Transistor (TFET) Used in a Single-Event-Upset (SEU) Insensitive 6 Transistor SRAM Cell in Ultra-Low Voltage Applications", In Proceedings of the 4th IEEE Conference on Nanotechnology, Munich, Germany, 2004, pp. 402-404.

[20] M. R. Tripathy, A. Samad, A. K. Singh, P. K. Singh, K. Baral, A. K. Mishra and S. Jit, "Impact of Interface Trap Charges on Electrical Performance Characteristics of a Source Pocket Engineered Ge/Si Heterojunction Vertical TFET with HfO2/Al2O3 Laterally Stacked Gate Oxide", *Microelectron. Reliab.*, vol. 119, p. 114073, 2021.

[21] M. R. Tripathy, A. K. Singh, K. Baral, P. K. Singh, A. K. Mishra, D. K. Jarwal and S. Jit, "Study of Temperature Sensitivity on Linearity Figures of Merit of Ge/Si Hetero-Junction Gate-Drain Underlapped Vertical Tunnel FET with Heterogeneous Gate Dielectric Structure for Improving Device Reliability", In Proceedings of URSI Regional Conference on Radio Science (URSI-RCRS), Varanasi, India, 2020, pp. 1-4.

[22] S. Singh and B. Raj, "Analytical Modelling and Simulation of Si-Ge Hetero-Junction Dual Material Gate Vertical T-Shaped Tunnel FET", *Silicon*, vol. 13, pp. 1139-1150, 2020.

[23] A. K. Singh, M. R. Tripathy, K. Baral and S. Jit "Design and Performance Assessment of HfO2/SiO2 Gate Stacked Ge/Si Heterojunction TFET on SELBOX Substrate (GSHJ-STFET)", Silicon, vol. 14, pp. 11847-11858, 2022.

[24] A. K. Singh, M. R. Tripathy, K. Baral, P. K. Singh and S. Jit, "Ferroelectric Gate Heterojunction TFET on Selective Buried Oxide (SELBOX) Substrate for Distortionless and Low Power Applications", In Proceedings of the 4th IEEE Electron Devices Technology & Manufacturing Conference (EDTM), Penang, Malaysia, 2020, pp. 1-4.

[25] D. Kumar, R. G. Mishra, R. Mishra and A. K. Shrivastava, "Impact of Band to Band Tunneling on Transient Performance of Dual Gate Tunnel Field Effect Transistor (TFET)", Int. J. Innov. Technol. Exploring Eng., vol. 8, no. 9, pp. 284-288, 2019.

[26] M. K. Yadav, S. K. Gupta, S. Rai and A. C. Pandey, "Al Embedded MgO Barrier MTJ: A First Principle Study for Application in Fast and Compact STT-MRAMs", *Superlattices and Microstruct.*, vol. 103, 314-324, 2017.

[27] M. K. Yadav and S. K. Gupta, "FeAl/MgO/FeAl MTJ with Enhanced TMR and Low Resistance Area Product for MRAM: A First Principle Study", *Micro and Nanostructures*, vol. 165, pp. 207192-207192, 2022.

[28] M. R. Tripathy, A. K. Singh, S. Chander, K. P. Singh and S. Jit, "Device-Level Performance Comparison of Some Pocket Engineered III-V/Si Hetero-Junction Vertical Tunnel Field Effect Transistor", In Proceedings of the 5th International Conference on Devices, Circuits and Systems (ICDCS), Coimbatore, India, 2020, pp. 180-183.

[29] D. Madadi and S. Mohammadi, "Switching Performance Assessment of Gate-All-Around InAs–Si Vertical TFET with Triple Metal Gate, a Simulation Study". *Nanoscale Res. Lett.*, vol. 18, p. 37, 2023.

[30] B. Ma, S. Chen, S. Wang, T. Han, H. Zhang, C. Yin, Y. Chen and H. Liu, "A Novel L-Gate InGaAs/GaAsSb TFET with Improved Performance and Suppressed Ambipolar Effect". *Micromachines*, vol. 13, no. (9), p. 1474, 2022.