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Original scientific paper

DESIGN OF LOW POWER CURRENT STARVED RING OSCILLATORS USING MODIFIED PARTICLE SWARM OPTIMIZATION

Sandeep Kumar Dash, Bishnu Prasad De, Bhargav Appasani, Nirmal Kumar Rout

School of Electronics Engineering, Kalinga Institute of Industrial Technology, Bhubaneswar, Odisha, India

ORCID iDs:	Sandeep Kumar Dash	https://orcid.org/0000-0002-7777-8289
	Bishnu Prasad De	https://orcid.org/0000-0002-1146-1692
	Bhargav Appasani	https://orcid.org/0000-0002-0878-7405
	Nirmal Kumar Rout	https://orcid.org/0000-0003-1983-792X

Abstract. *Ring oscillators (RO) are widely used for clock generation in RF applications. Design of RO is a very tedious process for RF IC designers using traditional methods like hand calculation or by simulator assistance. Traditional evolutionary optimization techniques, such as Particle swarm optimization (PSO) can be utilized for the design of the ROs. However, it shows limitations in convergence and stagnation. In this work to overcome these problems, PSO with Constriction Factor and Inertia Weight Approach (PSO-CFIWA) is applied to design a Current-starved Ring oscillator (CSRO). The optimum size of the CSRO transistors is obtained from PSO-CFIWA and designed in Cadence spectre using GPDK 90nm technology. The objective of the CSRO design is to have a 2 GHz oscillation frequency with optimized phase noise, power consumption, and figure of merit (FOM). The designed CSRO shows a 1.99963 GHz oscillation frequency, 348.48 μW power dissipation, –86.67 dBc/Hz phase noise, and FOM of – 157.25. The simulation results establish the effectiveness of PSO-CFIWA with its counterparts in RO design.*

Key words: *ring oscillator, current starved ring oscillator, FOM, phase noise, cadence*

1. INTRODUCTION

Ring oscillators (RO) are primarily used for clock generation, delay generation, and frequency synthesis for various radio frequency (RF) applications. The RO performance depends upon the frequency of oscillation, power dissipation, phase noise, area, and FOM. The designing of RO circuits at RF is a very challenging task for the designers due to trade-offs between various performance parameters. For designing the RO, designers need

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Corresponding author: Sandeep Kumar Dash
School of Electronics Engineering, Kalinga Institute of Industrial Technology, Bhubaneswar, Odisha, India.
E-mail: sandeepfet@kiit.ac.in

to consider these performance metrics as a benchmark to obtain the size of transistors and bias the circuit. Designers go through a time-consuming iterative manual process to obtain the proper size of the transistor to achieve target performance parameters. It was not always possible for designers to obtain the optimum results even after many design iterations.

To overcome this problem, an evolutionary algorithm is used in [1] to design an operational transconductance amplifier and Leap Frog filter. The multi-objective DIRECT (MODirect) optimization technique is used for optimizing various design parameters. In [2], the multi-objective evolutionary algorithm NSGAII is used to design RF low noise amplifier and leapfrog filter. In [3], the design of a nine-stage CMOS RO is reported with the help of CMODE. The RO circuit is implemented for a 2 GHz oscillation frequency with minimum FOM. In [4], NSGA-II is reported to optimize power dissipation and phase noise of five-stage CMOS RO. Four different heuristic algorithms are used in [5] to obtain the optimal channel width for the 3-stage CMOS RO that consumes the lowest average power. The fuzzy-modified Shuffled Frog Leaping Algorithm gives a superior solution as compared to the Genetic Algorithm, Fuzzy-GA, and Modified Shuffled Frog Leaping Algorithm. In [6], NSGA-II is applied to minimize the phase noise and power dissipation of the five, seven, and eleven-stage CMOS RO circuit. An intelligent sizing method is reported in [7] for the design of CMOS RO. In [8], graphical optimization is proposed for the optimization of RO. A novel design method is proposed for the optimal design of current-starved VCO [9]. In [10], the gravitational search algorithm is employed to design three VCOs with the objective of minimizing power and phase noise. Different VLSI circuits are optimally designed using different evolutionary techniques [11-21]. In [22], the design of RO is presented using the multi-objective binary cat swarm optimization (MOBCSO). In [23], five stage VCO is designed in 45 nm technology using PSO to optimize power consumption, phase noise and Figure of Merit (FOM). In [24], 8-stage VCO is designed with the help of Differential evolution (DE) and PSO to optimize three performance parameters. But it shows convergence and stagnation problem. The contribution of the paper is the application of the modified version of PSO, called PSO-CFIWA [25] for the optimal design of CSRO circuits. NSGA-II has high computational cost due to Pareto sorting and struggles with premature convergence, diversity maintenance, and scalability in high-dimensional problems. MOBCSO suffers from limited precision due to binary encoding, high computational overhead, slower convergence, and occasional sub-optimal solutions. MOMIPO has complex implementation, faces convergence issues in constrained design spaces, lacks robustness across varying problems, and struggles to balance conflicting objectives. Each algorithm requires further adaptations for efficient and robust RO optimization.

The novelty of this article is the application of the state-of-the-art algorithm in finding the device sizes for the design of a CSRO. This work aims to enhance the design efficiency of the CSRO by leveraging the PSO-CFIWA method to achieve better performance metrics.

The remaining part of the paper is organized as follows. Section 2 describes the performance parameters of CSRO. In Section 3, the evolutionary technique PSO-CFIWA is described for the design of a stage CSRO. In Section 4, the simulation results are presented. Finally, the paper has been concluded in Section 5.

2. CURRENT STARVED RING OSCILLATOR

The CSRO circuit can be designed by connecting an odd number of inverters in series as given in Figure 1. The oscillation frequency (f_{osc}) of a CSRO is expressed as:

$$f_{osc} = \frac{1}{2N\tau} \tag{1}$$

where N represents the inverter stages and τ denotes the average propagation delay of each stage.

The average power consumption of the CSRO circuit is given as:

$$P_{avg} = \eta\, N\, C_{tot}\, V_{DD}^2\, f_{osc} \tag{2}$$

where η varies between 0.7 to 0.9.

The phase noise [9] of the CSRO circuit is represented as:

$$L\{\Delta f\} = \frac{8}{3\eta}\frac{kT}{P}\frac{V_{DD}}{V_{char}}\frac{f_{osc}^2}{\Delta f^2} \tag{3}$$

where $V_{char} = \frac{\Delta V}{\gamma}$, ΔV is the overdrive voltage, γ represents the body effect coefficient, T denotes the absolute temperature, k represents Boltzmann constant, Δf is the offset frequency, *and* $\gamma = 2/3$.

The FOM of the RO circuit [6] can be calculated as:

$$FOM = 10\ \log_{10}\left[L\{\Delta f\}\frac{\Delta f^2}{f_{osc}^2}\frac{P_{avg}}{1mW}\right] \tag{4}$$

The primary objective of the CSRO circuit is to obtain a 2 GHz frequency of oscillation with minimum power dissipation, phase noise, and FOM. The following sizing constraints are considered for the design.

$$W_{n,\min} \le W_n \le W_{n,\max}$$

$$W_{p,\min} \le W_p \le W_{p,\max}$$

$$L_n = L_p = L = 180\ \text{nm}$$

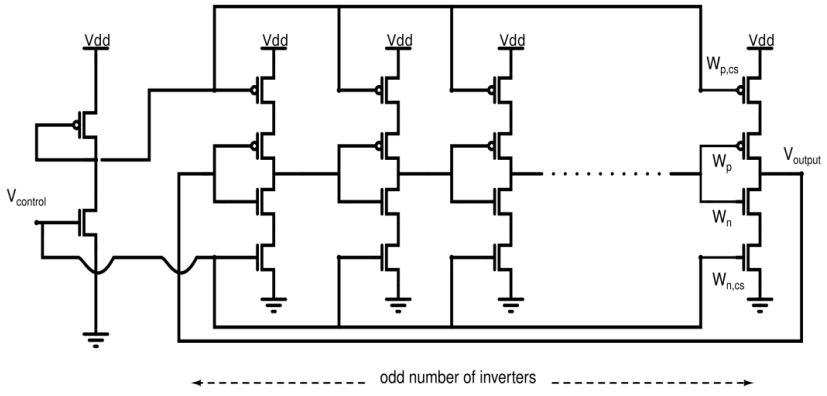

Fig. 1 Circuit diagram of the CSRO

3. EVOLUTIONARY ALGORITHMS EMPLOYED

PSO and PSO-CFIWA algorithms are described briefly.

3.1. PSO

Particle Swarm Optimization (PSO) is a versatile and robust population-based stochastic optimization method that operates with inherent parallelism. Unlike traditional optimization techniques, PSO can effectively handle objective functions that are non-differentiable. Compared to Genetic Algorithms (GA) and Simulated Annealing, PSO has a lower tendency to become trapped in local optima. Originally introduced by Kennedy et al. [26], PSO is inspired by the coordinated movement of bird flocks. It simulates the way birds navigate through a multi-dimensional space to optimize a given objective function. Each particle (representing a potential solution) keeps track of its own best-known position (pbest), based on its individual experience. Additionally, each particle has access to the best-known position within the swarm (gbest), which is determined from the personal bests of all particles. The position of each particle is updated by considering:

- The gap between the particle's present location and the highest position it has individually reached.
- The gap between the particle's present location and the best position found by the entire group.

The detailed description of PSO is given in [26]. The velocities of the particle vectors are modified as:

$$V_i^{(k+1)} = w \times V_i^k + C_1 \times rand_1 \times (pbest_i^k - X_i^k) + C_2 \times rand_2 \times (gbest^k - X_i^k) \tag{5}$$

The velocity and position of the ith particle vector at the kth iteration is denoted as V_i^k and X_i^k respectively. The parameter w represents the weighting function and parameters C_1 and C_2 both represents positive weighting factors. The terms $rand_1$ and $rand_2$ are randomly generated numbers within the range [0,1]. Additionally, $pbest_i^k$ signifies the best position achieved by the ith particle up to iteration k, while $gbest^k$ denotes the best position identified by the entire swarm at the same iteration.

The searching point is modified by:

$$X_i^{(k+1)} = X_i^k + V_i^{(k+1)} \tag{6}$$

The flow chart of conventional PSO is given in Figure 2.

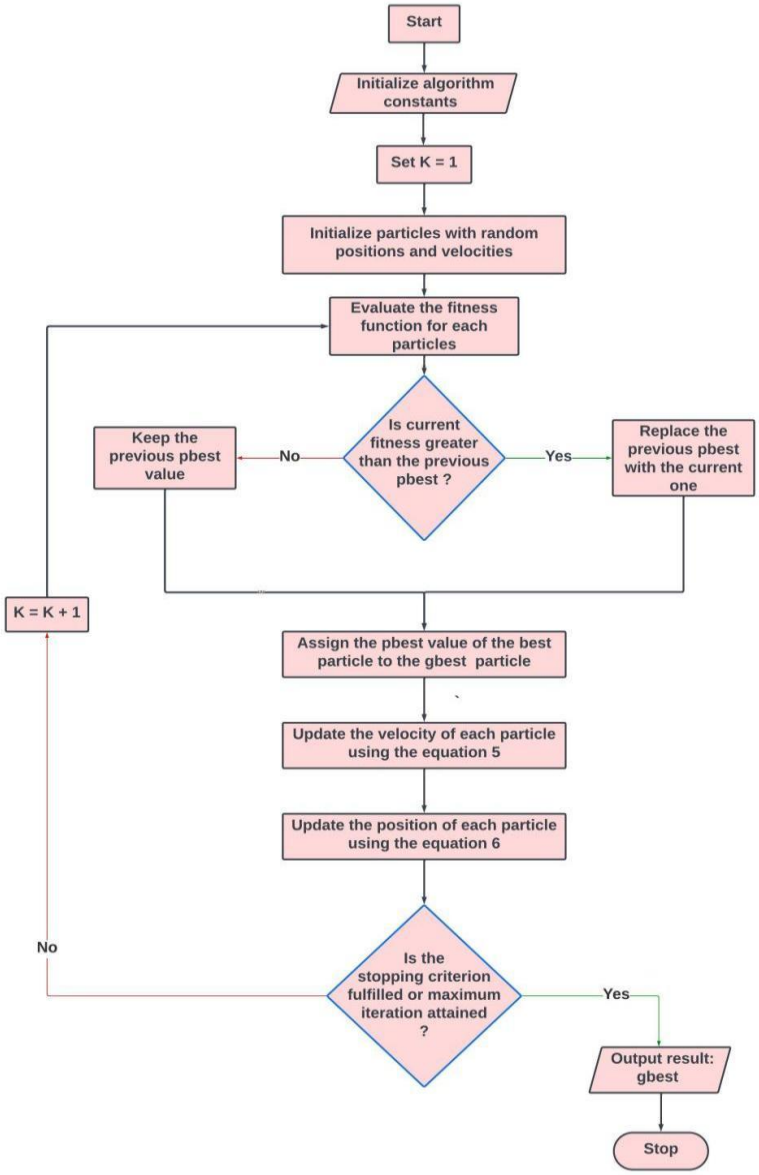

Fig. 2 Flowchart of PSO

3.2. PSO-CFIWA

For PSO-CFIWA [25], the velocity of (5) is changed in accordance with (7):

$$V_i^{k+1} = CFa \times (w^{k+1} * V_i^k + C_1 * rand_1 * (pbest_i - S_i^k) + C_2 * rand_2 * (gbest - S_i^k) \quad (7)$$

Normally, $C_1 = C_2 = 1.5\text{-}2.05$, and the Constriction Factor (CF_a) is given in (8):

$$CFa = \frac{2}{\left|2 - \varphi - \sqrt{\varphi^2 - 4\varphi}\right|} \tag{8}$$

where $\varphi = C_1 + C_2$ and $\varphi > 4$. For $C_1 = C_2 = 2.05$, the calculated value of $CF_a = 0.73$. The inertia weight (w^{k+1}) at $(k+1)^{th}$ cycle is expressed in (9).

$$w^{k+1} = w_{\max} - \frac{w_{\max} - w_{\min}}{k_{\max}} \times (k+1) \tag{9}$$

where, $w_{max} = 1.0$; $w_{min} = 0.4$; k_{max} = Maximum number of iteration cycles. The parameters of PSO-CFIWA are given in Table 1.

Table 1 Control parameters of PSO-CFIWA

Parameters	Value
Population size	10
Dimension	5
Iteration cycles (k_{max})	500
C_1	2.05
C_2	2.05
φ	4.1
CF_a	0.73
w_{max}	1.0
w_{min}	0.4

4. SIMULATION RESULTS

The thirteen-stage CSRO is designed in Cadence suite with GPDK 90 nm technology. The width (W) and length (L) size of NMOS and PMOS transistors are obtained from the proposed PSO-CFIWA optimization. The constraints for the CSRO are considered the same as in [9]. The sizing constraints and optimal sizing values obtained using PSO-CFIWA for CSRO are provided in Table 2.

Table 2 Obtained transistor size for CSRO

Sizing Parameter	Lower-Upper Limit	Optimized Value
$W_{n,cs}$ (nm)	1000-5000	1110
$W_{p,cs}$ (nm)	5000-20000	6370
W_n (nm)	200-500	328
W_p (nm)	400-1000	679
L (nm)	100-110	102.5

The oscillation waveform of the CSRO at the output of the CSRO is depicted in Figure 3. The output waveform of the CSRO is almost rail-to-rail with a 1.99 GHz frequency of oscillation.

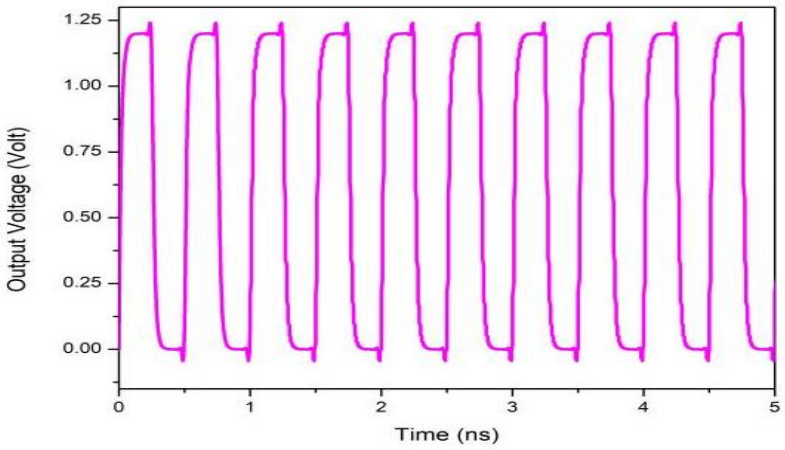

Fig. 3 Oscillation waveform of the CSRO

The power consumption estimation waveform of CSRO is depicted in Figure 4. The CSRO circuit consumes an average power of 348.48 µW. The phase noise plot of CSRO is depicted in Figure 5. The designed circuit is having phase noise of - 86.67 dBc/Hz at 1 MHz offset frequency.

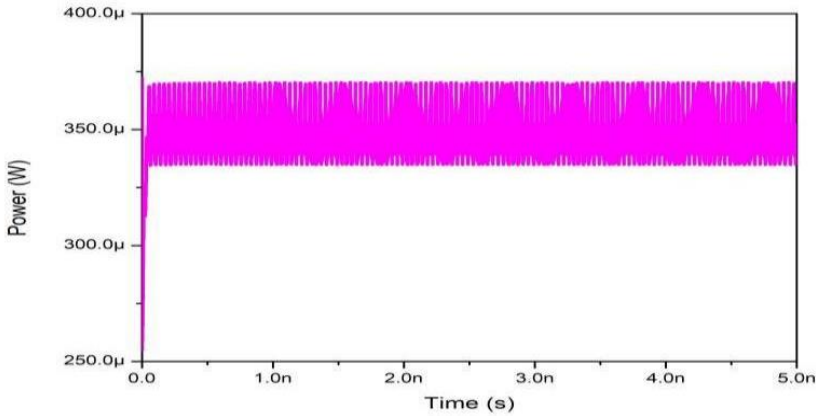

Fig. 4 Power estimation of the CSRO

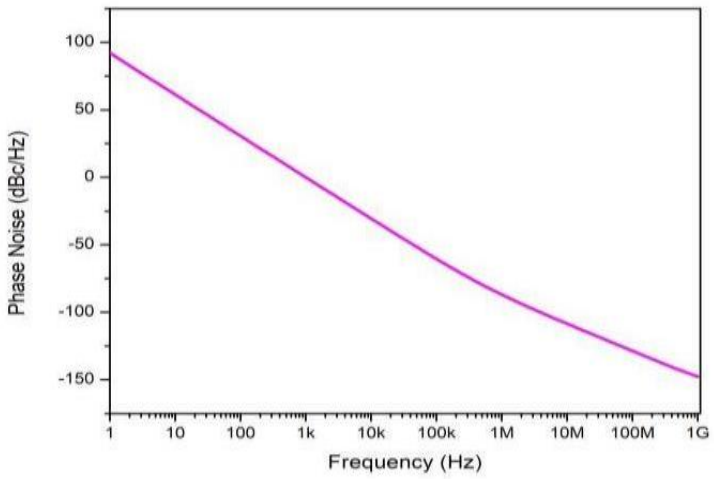

Fig. 5 Phase noise estimation of the CSRO

Figure 6 presents the influence of the control voltage on the oscillation frequency of the CSRO circuit. It is observed that the circuit initiates oscillation at a minimum control voltage of 0.1 V. Furthermore, the effect of supply voltage variation on the oscillation frequency is illustrated in Figure 7. A deviation of ±10% from the nominal supply voltage of 1.2 V results in a corresponding frequency variation, with the oscillation frequency ranging from 1.893 GHz to 2.06 GHz.

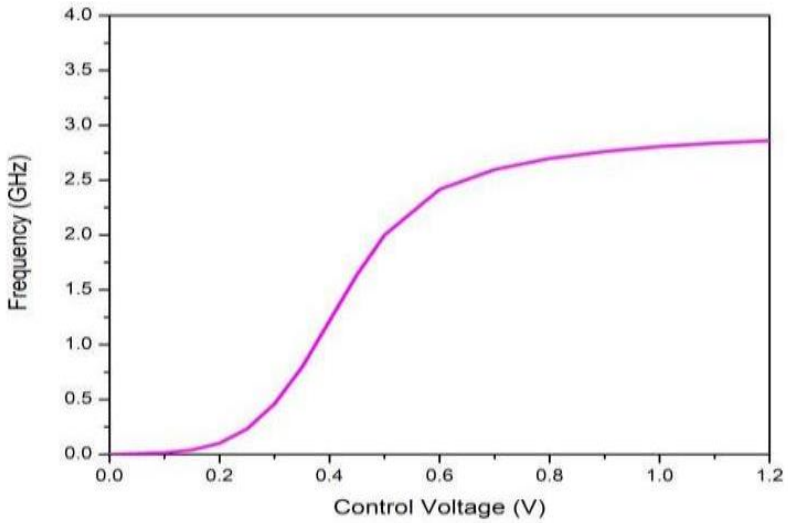

Fig. 6 Oscillation frequency vs control voltage plot

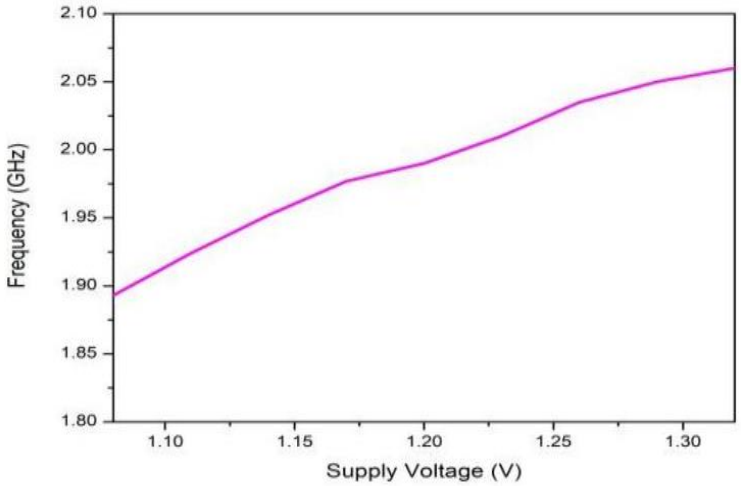

Fig. 7 Oscillation frequency vs supply voltage plot

Figure 8 depicts about change in CSRO oscillation frequency due to temperature changes. The oscillation frequency of CSRO varies from 2.42 GHz to 1.56 GHz due to temperature changes from -25℃ to 100℃. The change in oscillation frequency due to different design Processes is depicted in Figure 9. The designed CSRO shows oscillation frequency of 1.29 GHz, 1.48 GHz, 1.99 GHz, 2.25 GHz, 2.76 GHz at process corners SS, SF, NN, FS and FF respectively. Figure 7-9 establishes the design efficacy of the designed CSRO against PVT variations.

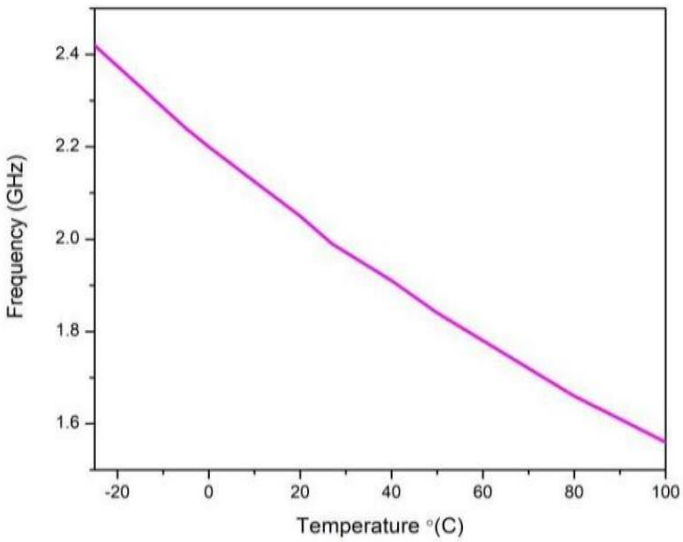

Fig. 8 Temperature vs oscillation frequency plot

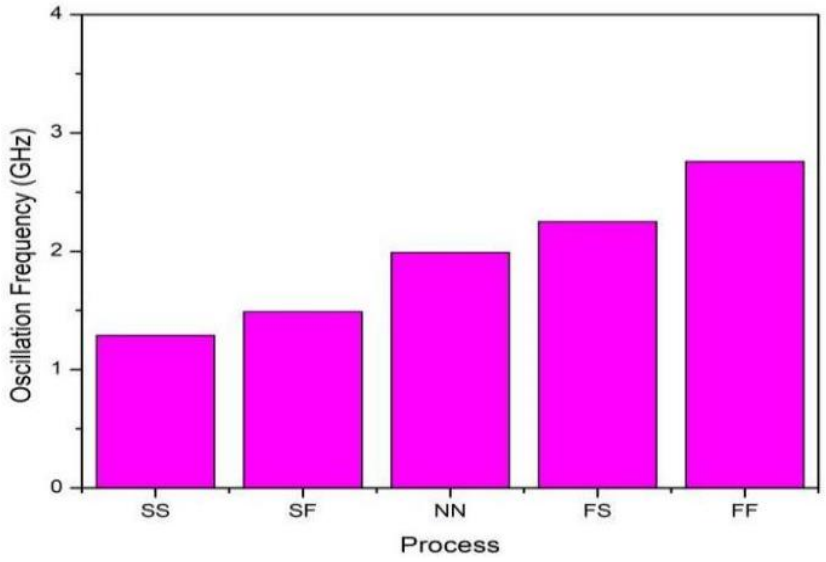

Fig. 9 Process vs oscillation frequency plot of the CSRO

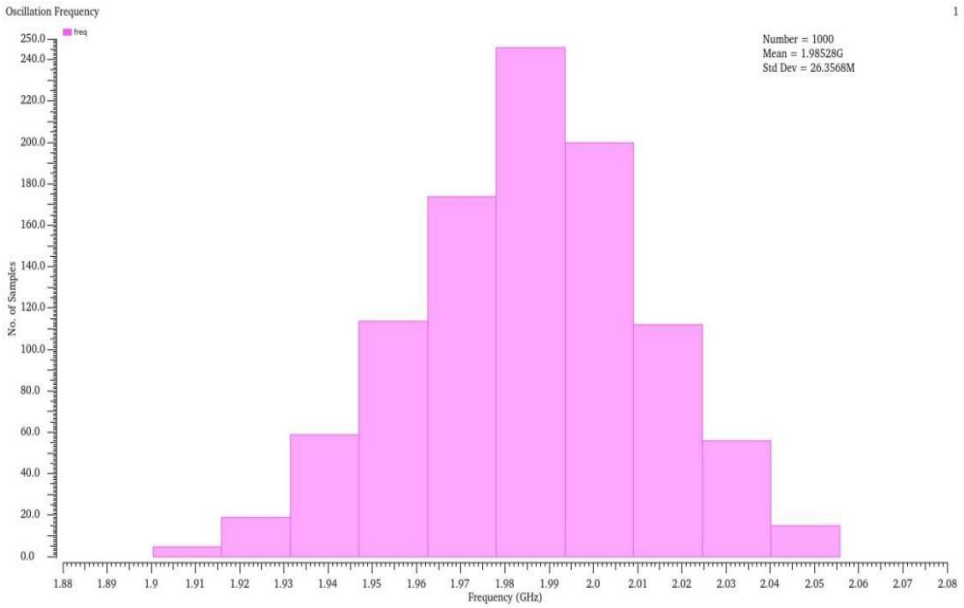

Fig. 10 Monte Carlo plot of the designed CSRO

The impact of mismatch and process variations on circuit performance was statistically evaluated using Monte Carlo (MC) simulation. For the MC simulation, 1000 samples were analyzed to ensure reliable statistical outcomes. Figure 10 presents histograms illustrating the oscillation frequency distribution. The mean and standard deviation of the oscillation

frequency were observed to be 1.985 GHz and 26.35 MHz, respectively. The MC simulation results indicate that the performance parameters of the optimized CSRO circuit exhibit minimal sensitivity to mismatch and process variations.

In Table 3, a comparison of performance parameters is reported with other reported work. Monte Carlo results and results reported in Table 2 prove the robustness of the designed CSRO circuit. The proposed PSO-CFIWA produce better FOM than [9, 20-22] for the design of CSRO. The proposed approach outperforms other methods in terms of solution quality, as shown in the comparative analysis within the paper. The Ref [12] shows better FOM than this work. MOPSO is better than PSO-CFIWA for multi-objective optimization problems because it is specifically designed to handle conflicting objectives, maintain solution diversity, and provide a Pareto front.

Table 3 Comparison of performance matrices of CSRO.

Parameter	IDEA [9]	MOPSO [12]	IDEA [18]	[19]	[20]	[21]	MOBCSO [22]	PSO [23]	DE [24]	This work
Technology	90 nm	180 nm	90 nm	180 nm	180 nm	90 nm	90 nm	45 nm	180 nm	90 nm
Frequency of oscillation (GHz)	2.0009	1.906	2.048	2.87	1.825	2.4	2.005	1.047	0.104	1.999
Average Power consumption (μW)	765.64	108	1062.5	1336	1278	1540	78.5	1.787	26410	348.48
Phase noise (dBc/Hz)	–88.33	–107.4	NR	NR	–85.37	–88.34	–86	–82.28	–129.01	–86.67
FOM	–155.48	–167.10	NR	NR	–149.53	–155.8	–149.06	NR	NR	–157.25

5. Conclusion

Three key performance parameters of the Current-Starved Ring Oscillator (CSRO) were optimized to meet the specified target requirements using the Particle Swarm Optimization with Comprehensive Fitness Indicator Weighted Average (PSO-CFIWA) approach. This optimization method was selected for its ability to balance multiple objectives effectively, leveraging its comprehensive fitness evaluation to achieve superior performance metrics. The CSRO circuit was designed using transistor dimensions derived from the PSO-CFIWA optimization process, designed to attain a target oscillation frequency of 2 GHz. Post-implementation, the circuit demonstrated an oscillation frequency of 1.999 GHz, with a power dissipation of 348.48 μW, phase noise of –86.67 dBc/Hz at 1 MHz offset frequency, and an FOM of –157.25. The improved FOM highlights the effectiveness of PSO-CFIWA in enhancing circuit performance by simultaneously optimizing multiple critical parameters. To ensure reliability and robustness, extensive simulations and analyses were conducted. Monte Carlo simulations were performed to study the effects of random mismatch and process variations on circuit performance. By incorporating a weighted average approach to balance competing objectives, PSO-CFIWA efficiently navigates the design space to achieve optimal solutions. This makes it a valuable tool for designing high-performance circuits where multiple performance

trade-offs must be carefully managed. In conclusion, the PSO-CFIWA-optimized CSRO circuit demonstrates exceptional performance, robustness, and reliability, setting a new benchmark for FOM in oscillator design. The combination of advanced optimization techniques and rigorous validation establishes this approach as a powerful methodology for achieving high-performance electronic designs. The PSO-CFIWA methodology can be extended to the design of other analog circuits, including operational amplifiers, filters, and similar applications. In recent years, several novel bio-inspired multi-objective optimization techniques have been introduced, which present an opportunity for further exploration. These methods could be applied to the design of the CSRO and used for comparative analysis against the performance metrics reported in this study, providing insights into their relative efficacy.

REFERENCES

[1] J. T. Biondi, C. Ciccazzo, V. Cutello, S. D'Antona, G. Nicosia and S. Spinella, "Multi- Objective Evolutionary Algorithms and Pattern Search Methods for Circuit Design Problems", *J. Universal Comput. Sci.*, vol. 12, no. 4, pp. 432-449, 2006.

[2] G. Nicosia, S. Rinaudo and E. Sciacca, "An Evolutionary Algorithm Based Approach to Robust Analog Circuit Design Using Constrained Multiobjective Optimization", *Knowl.-Based Syst.*, vol. 21, pp.175-183, 2008.

[3] P. K. Rout and D. P. Acharya, "Design of CMOS Ring Oscillator Using CMODE", In Proceedings of International Conference on Energy, Automation and Signal, Bhubaneswar, India, 2011, pp. 1-6.

[4] P. K. Rout, D. P. Acharya and G. Panda, "Constrained Multiobjective Optimization Based Design of CMOS Ring Oscillator", In Proceedings of International Conference on Computer Communication and Informatics, Coimbatore, India, 2014, pp. 1-5.

[5] F. Keivanian, "Minimization of Average Power Consumption in 3 Stage CMOS Ring Oscillator Based on MSFLA, Fuzzy-MSFLA, GA, and Fuzzy-GA", *Int. J. Comput. Appl.*, vol. 104, no. 16, pp. 30-37, 2014.

[6] P. K. Rout and D. P. Acharya, "Fast Physical Design of CMOS ROs for Optimal Performance Using Constrained NSGA-II", *AEU-Int. J. Electron. Commun.*, vol. 69, no. 9, pp. 1233-1242, 2015.

[7] A Mohammadi, M. Mohammadi and S. H. Zahiri, "Design of Optimal CMOS Ring Oscillator Using an Intelligent Optimization Tool", *Soft Comput.*, vol. 22, pp. 8151-8166, 2018.

[8] N. Gargouri, D. Ben Issa, Z. Sakka, A. Kachouri and M. Samet, "Design and Optimization of Differential Ring Oscillator for IR-UWB Applications in 0.18 µm CMOS Technology", *J. Circuits, Syst. Comput.*, vol. 26, no. 5, pp. 1-15, 2017.

[9] P. K. Rout, D. P. Acharya and G. Panda, "A Multiobjective Optimization Based Fast and Robust Design Methodology for Low Power and Low Phase Noise Current Starved VCO", *IEEE Trans. Semicond. Manuf.*, vol. 27, no. 1, pp. 43-50, Feb. 2014.

[10] M. Ghasemi, A. Mahanipour and M. Saneei, "Fast Optimization for VCOs Using GSA Algorithm," In Proceedings of Iranian Conference on Electrical Engineering (ICEE), Mashhad, Iran, 2018, pp. 315-319.

[11] S. K. Dash, B. P. De, P. K. Samanta, B. Appasani, R. Kar, D. Mandal and N. Bizon, "Optimal Design of Voltage Reference Circuit and Ring Oscillator Circuit Using Multiobjective Differential Evolution Algorithm", *J. Electr. Comput. Eng.*, vol. 2023, p. 7621594, pp. 1-11. 2023.

[12] S. K. Dash, B. P. De, R. Das, P. K. Samanta, W. Bhowmik, R. Kar, D. Mandal and A Bakshi, "Optimal Design of Current Starved Oscillator using MOPSO", In Proceedings of International Conference on Communication, Circuits, and Systems (IC3S), Bhubaneswar, India, 2023, pp. 1-4.

[13] R. Das, B. P. De, S. K. Dash, P. K. Samanta, W. Bhowmik, R. Kar and D. Mandal, "Multi-objective Optimization for Optimal Design of CMOS Ring Oscillator", In Proceedings of International Conference on Recent Advances in Electrical, Electronics, Ubiquitous Communication, and Computational Intelligence (RAEEUCCI), Chennai, India, 2023, pp. 1-4.

[14] S. Ghosh, B. P. De, R. Kar, D. Mandal and A. K. Mal, "Optimal Design of a 5.5-GHz Low-Power High-Gain CMOS LNA Using the Flower Pollination Algorithm", *J. Comput. Electron.*, vol. 18, pp. 737-747, 2019.

[15] S. Ghosh, B. P. De, K. B. Maji, R. Kar, D. Mandal and A. K. Mal, "Optimal Design of Ultra-Low-Power 2.4 GHz LNA for IEEE 802.15.4/Bluetooth Applications", *J. Circuits Syst. Comput.*, vol. 29, no. 16, pp. 1-19, 2020.

[16] A. Raj, S. Majumder and G. P. Mishra, "Design of a CMOS Based Ring VCO Using Particle Swarm Optimisation", *Analog Integr. Circuits Signal Process.*, vol. 119, pp. 309-317, 2023.

[17] P. R. Castañeda-Aviña, E. Tlelo-Cuautle, L.-G. de la Fraga, "Phase Noise Optimization of Integrated Ring Voltage-Controlled Oscillators by Metaheuristics", *AIMS Mathematics*, vol. 7, no. 8, pp. 14826-14839, 2022.

[18] P. K. Rout, D. P. Acharya, G. Panda and D. Nayak, "Process Corner Variation Aware Design of Low Power Current Starved VCO Power", In Proceedings of International Conference on Electronics and Communication Systems (ICECS), Coimbatore, India, 2014, pp. 1-4.

[19] V. G. Nasre and G. M. Asutkar, "Design of Current Starved Voltage Control Oscillator with Bandgap Reference in 0.18μm CMOS Process", In Proceedings of International Conference on Recent Innovations in Signal Processing and Embedded Systems (RISE), Bhopal, India, 2017, pp. 375-380.

[20] U. Nanda, D. Nayak, S. K. Pattnaik, S. K. Swain, S. M. Biswal, B. Biswal, "Design and Performance Analysis of Current Starved Voltage Controlled Oscillator", in *Microelectronics, Electromagnetics and Telecommunications. Lecture Notes in Electrical Engineering*, vol 521, 2019, Springer, Singapore.

[21] J. K. Panigrahi, D. P. Acharya and U. Nanda, "Performance Analysis of Dual Threshold CMOS based Current Starved Voltage Controlled Oscillator - A Review," In Proceedings of the 2nd International Conference on Artificial Intelligence and Signal Processing (AISP), Vijayawada, India, 2022, pp. 1-4.

[22] R. Das, et al., " Multi-Objective Optimization for Optimal Design of CMOS Ring Oscillator", In Proceedings of International Conference on Recent Advances in Electrical, Electronics, Ubiquitous Communication, and Computational Intelligence (RAEEUCCI), 2023, pp. 1-4.

[23] A. Raj, S. Majumder and G. P. Mishra, " Design of a CMOS Based Ring VCO Using Particle Swarm Optimisation", *Analog Integr. Circuits Signal Process.*, vol. 119, no. 2, pp. 309-317, 2024.

[24] P. R. Castañeda-Aviña, E. Tlelo-Cuautle and L. G. de la Fraga, "Phase Noise Optimization of Integrated Ring Voltage-Controlled Oscillators by Metaheuristics", *AIMS Mathematics*, vol. 7, no. 8, pp. 14826-14839, 2022.

[25] D. Chowdhury, B. P. De, S. Ghosh, N. K. Singh, R. Kar and D Mandal, "Optimization of Subthreshold Parameters of Graded-Channel Gate-Stack Double-Gate (GC-GS-DG) MOSFET Using PSO-CFIWA", in *Lecture Notes in Electrical Engineering*, vol. 904, Springer, 2023.

[26] J. Kennedy and R. Eberhart, "Particle Swarm Optimization", In Proceedings of IEEE International Conference on Neural Network, 1995, vol. 4, pp. 1942-1948.