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Editorial

EDITORIAL
THEMATIC ISSUE ON FAILURE MECHANISMS IN MICROELECTRONIC DEVICES

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Throughout the years, our knowledge of the root cause and physical behavior of critical failure mechanisms in microelectronic devices has grown significantly. However, the mechanisms that fully explain various experimental data have not yet been thoroughly elucidated and remain the subject of investigation. Findings and discussion of the thematic issue Facta Universitatis, Series Electronics and Energetics "Failure Mechanisms in Microelectronics Devices" should improve the research potential in the academic and industry environments in this area. For papers are published offering interesting and valuable scientific results.

The paper "Successive Irradiation and Bias Temperature Stress Induced Effects on Commercial p-Channel Power VDMOS Transistors" examines the effects of negative bias temperature (NBT) stress on irradiated commercial p-channel power VDMOS transistors, with a focus on contribution to threshold voltage shift of changes in gate oxide charge and interface traps. The research addresses the critical reliability concerns for these transistors, as shifts in the threshold voltage can notably influence device performance, particularly under conditions of elevated temperature and negative gate oxide fields. Considering that VDMOS transistors are power devices, high temperatures occur during their operation, which can cause NBT effects, and this definitely affects normal operation. Furthermore, the study investigates the implications of irradiation on the electrical parameters of VDMOS power transistors, highlighting the need for a thorough understanding of these effects. The experimental methodology includes both irradiation and subsequent NBT stress application. This paper provides a detailed analysis of both static and pulsed NBT stressing, with an emphasis on novel stress signals related to practical applications. The data presented in the paper were obtained by exposing components to NBT stresses with different polarizations on the gate, which were previously exposed to radiation to different doses, with and without polarization. Also, the results with different frequencies applied during NBT stress are presented. Results from the study elucidate the roles of gate oxide charge and interface traps in contributing to threshold voltage shifts, thereby offering critical insights into the reliability of p-channel power VDMOS transistors in various operational stress scenarios. Self-heating during both the operational and cooling phases of fresh and previously irradiated components were measured using IR camera These findings are instrumental for

the design and operation of electronic systems that utilize these transistors, ensuring improved reliability and performance.

The next paper "Evaluating NBTI and HCI Effects on Device Reliability for High-Performance Applications in Advanced CMOS Technologies" points to the fact that the integrated circuit (IC) industry faces significant reliability challenges as MOSFET devices age, particularly at advanced nodes. Key degradation mechanisms include hot-carrier injection (HCI), negative-bias temperature instability (NBTI), and positive-bias temperature instability (PBTI), affecting both PMOS and NMOS transistors. These aging effects alter critical parameters like drain current and threshold voltage, reducing device lifespan. This paper introduces a comprehensive aging framework for MOSFETs, accounting for PBTI, NBTI, and HCI with a focus on partial recovery in AC operations at advanced technology node of 22nm. A machine learning model enhances feature extraction, while the MOSRA approach accelerates SPICE simulations to optimize yield and reliability.

The following paper, "Impact of Interface Oxide Type on the Gamma Radiation Response of SiC TTL ICs" investigates the impact of Gamma Radiation on 4H Silicon Carbide (SiC) Transistor-Transistor Logic (TTL) integrated circuits (ICs), particularly focusing on inverters processed with distinct types of interface oxides: Thermally Grown, Chemical Vapor Deposition, and Atomic Layer Deposition. This research was conducted using a ^{60}Co source at Hiroshima University, applying varied radiation doses (17.9 $rad_{(Si)}$/s, 7.3 $rad_{(Si)}$/s, and 2.47 $rad_{(Si)}$/s) to assess the resilience of the SiC inverters under these conditions. Their findings reveal that thermal oxides (Batch 1: W_1 and W_2) demonstrate higher radiation resilience compared to ALD and CVD interface oxides (Batch 2: W_3 and W_4), attributable to their denser structure and fewer defects. The study also identifies that while the inverters exhibit marginal degradation at gamma doses nearing 700 krad (under 6%), the most critical operational state is the passive mode (V_{CC} = V_{IN} = 0 V), where the build-up of induced charge in the oxide and interface may lead to early IC degradation of the noise margins. The outcomes from this research provide insights into the processing flow and enhancement of SiC electronics. These results underscore the potential of SiC-based ICs in environments with high radiation levels, such as space missions, nuclear reactors, and medical applications, due to their enhanced radiation tolerance.

In the last paper, "Determing the Characteristics of the Localized Density of States Distribution Present in MoS2 2D FETs" the behaviour of MoS2 FETs, with channel lengths greater than the mean free path of carriers was analysed. Electrical behaviour of experimental devices with channel lengths of 5 μm and 0.1 μm was studied, modelled and simulated, concluding that the predominant transport mechanism observed was hopping. The presence of a localized density of states (DOS) distribution in the semiconductor layer, causing the behaviour observed in these devices, was studied and determined by both modelling and simulation.

Finally, I would like to take the opportunity to thank the authors and reviewers for their efforts. Without great enthusiasm and efforts from them, this thematic issue could not have been made.

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Editor-in-Chief