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MICROELECTRONICS PACKAGING TECHNOLOGY ROADMAPS, ASSEMBLY RELIABILITY, AND PROGNOSTICS

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Abstract. *This paper reviews the industry roadmaps on commercial-off-the shelf (COTS) microelectronics packaging technologies covering the current trends toward further reducing size and increasing functionality. Due to the breadth of work being performed in this field, this paper presents only a number of key packaging technologies. The topics for each category were down-selected by reviewing reports of industry roadmaps including the International Technology Roadmap for Semiconductor (ITRS) and by surveying publications of the International Electronics Manufacturing Initiative (iNEMI) and the roadmap of association connecting electronics industry (IPC). The paper also summarizes the findings of numerous articles and websites that allotted to the emerging and trends in microelectronics packaging technologies.*

A brief discussion was presented on packaging hierarchy from die to package and to system levels. Key elements of reliability for packaging assemblies were presented followed by reliabilty definition from a probablistic failure perspective. An example was present for showing conventional reliability approach using Monte Carlo simulation results for a number of plastic ball grid array (PBGA). The simulation results were compared to experimental thermal cycle test data. Prognostic health monitoring (PHM) methods, a growing field for microelectronics packaging technologies, were briefly discussed. The artificial neural network (ANN), a data-driven PHM, was discussed in details. Finally, it presented inter- and extra-polations using ANN simulation for thermal cycle test data of PBGA and ceramic BGA (CBGA) assemblies.

Key Words: *Microelectronics, ITRS, iNEMI, IPC, BGA, WLP, 3D, solder joint reliability, prognostic, neural network, PHM*

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1. ELECTRONICS PACKAGING TRENDS

1.1. Introduction

As with many advancements in the electronics industry, consumer electronics is driving the trends for electronic packaging technologies toward reducing size and increasing functionality. Microelectronics meeting the technology needs for higher performance (faster), reduced power consumption and size (better), and commercial-off-the-shelf (COTS) availability (cheaper). This paper emphasizes on three industry roadmaps for conventional microelectronics (see Fig. 1-1). The three key industry roadmap associations have chapters on microelectronics packaging, each with different perspective covering technologies from the die to assembly levels. The topics for each category were congregated by reviewing the recent reports of the international technology roadmap for semiconductor (ITRS) [1], the reports of the International Electronics Manufacturing Initiative (iNEMI) [2], and those of association connecting electronics industry (IPC) [3] in conjunction with surveying numerous articles and websites covering the trends in microelectronics packaging technologies. Fig. 1-1 summarizes the key perspectives of these three roadmap societies.

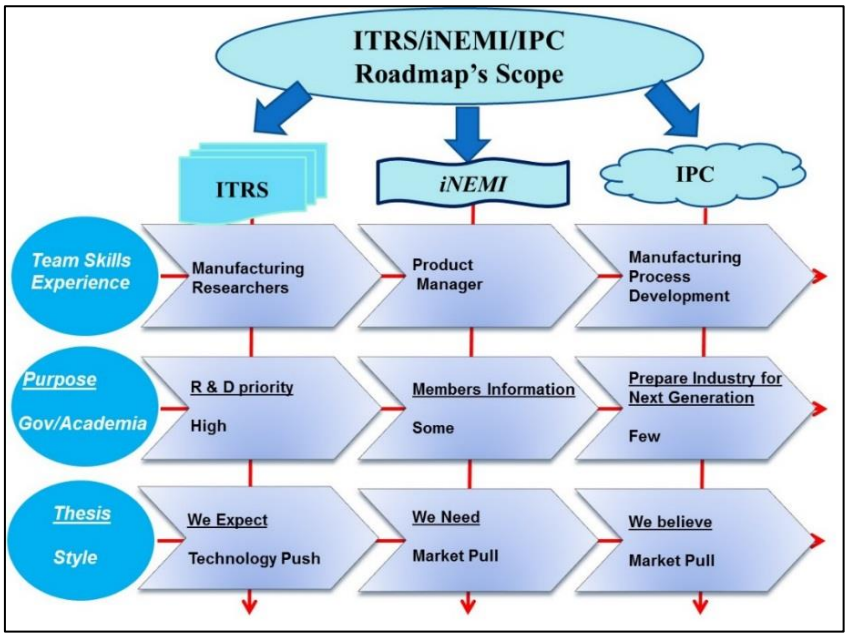


Fig. 1-1 ITRI, iNEMI, and IPC roadmap focus and development styles.

Fig. 1-2 illustrates the key technology coverages by a more recently introduced roadmap for organic and printed electronics applications. The roadmap is published by the Organic Printed Electronics Association (OE-A) [4]. Even though the printed electronics started to become a key growth technology, its scope is beyond this paper due to the breadth of work being performed in the area of conventional microelectronics packaging. This paper presents a summary of key findings regarding the packaging technologies including sing-chip, multi-chip, 3D stack, embedded active, materials, and hierarchy for microelectronics packaging.

Fig. 1-2 OE-A roadmap showing key technology and application coverage [4].

1.2. Key roadmap organizations

Industry roadmap organizations have been created to address trends in numerous technologies including microelectronic, optics, and printed electronics. Table 1-1compares key attributes and overlap areas of three industry roadmaps discussed in the following, i.e., ITRS, iNEMI, and IPC. The ITRS roadmap emphasis is on the front-end conventional microelectronics field, and it is sponsored by the world's five leading chip manufacturers. The objective of the ITRS is to ensure cost-effective advancements in the performance of integrated circuits and the products that employ such devices; thereby supporting the health and success of this industry.

Table 1-1 Team member make up and skills as well technology focus and development for ITRS iNEMI, and IPC —the key roadmap development industries for microelectronics sectors [3].

	ITRS	iNEMI	IPC
Team Makeup	Senior Techs. -Management -Engineers	Senior Techs. -Management -Engineers	Senior Techs. -Management -Engineers
Team Skills/Experience	Manufacturing Researchers	Product Managers	Manufacturing Process Develop.
Industry R&D Invest.	<10%	4-5%	>1%
Government and Academia Participation	High	Some	Few
Roadmap Purpose	R&D priority	Members' Information	Prepare Industry for Next Generation
Thesis	We Expect	We Need	We Believe
Style	Technology Push	Market Pull	Market Pull

iNEMI, a consortium of approximately 100 leading electronics manufacturers, suppliers, associations, government agencies and universities, is another industry roadmap provider. iNEMI roadmaps cover the future technology requirements of the global electronics industry by identifying and prioritizing gaps in technology and infrastructure. With the support of participant companies, iNEMI generates timely, high-impact deployment projects to address or eliminate those gaps.

The IPC electronic interconnection roadmap covers three basic elements: (1) the design and fabrication of semiconductors and their associated packaging; (2) the fabrication of the interconnecting substrate for both the semiconductor package and the product printed board; and (3) multiple levels of assembly and test. The IPC roadmap encounters challenges in covering increasingly fluid business relationships for the original equipment manufacturers (OEMs) and electronics manufacturing services (EMS's). Now, the OEM markets may be anywhere on the planet rather than previously they were a predominantly simple model of a vertically integrated company. Teams of experts from many organizations around the world have cooperated to ensure that the IPC roadmap presents the recommendations based on the vision and needs assessments of OEM, ODM, and EMS companies.

The OE-A, a working group within the German engineering federation (VDMA) was organized more than a decade ago to create a communication and development interface for various fields of research. It represents the entire value chain of organic electronics, from the materials supplier and equipment and product manufacturer through to the user. The OE-A's goal is to issue roadmaps that serves as a guide to the multitude of technical developments and help to define possible applications. While many of the developments of OE-A members are still in the test phase in the lab, a whole series of practical applications is already in use.

1.2.1. ITRS roadmap

For five decades, the semiconductor industry has distinguished itself by the rapid pace of improvement in its products-based miniaturization level. This is usually expressed as Moore's Law, but is also sometime called scaling. The most significant trend is the decreasing cost-per-function, which has led to substantial improvements in economic productivity and overall quality of life through proliferation of computers, communication, and other industrial and consumer electronics. To help guide these R&D programs in scaling, the Semiconductor Industry Association (SIA) met with corresponding industry associations in Europe, Japan, Korea, and Taiwan to participate in a 1998 update of its roadmap and to begin work toward the first ITRS, published in 1999. Since then, the ITRS has been updated in even years and fully revised in between years. The latest update of the roadmap is posted on the ITRS website. Fig. 1-3 shows the ITRS roadmap for printed CMOS Moore's Law and beyond, which more recently has been called "More than Moore" or its abbreviation, MtM.

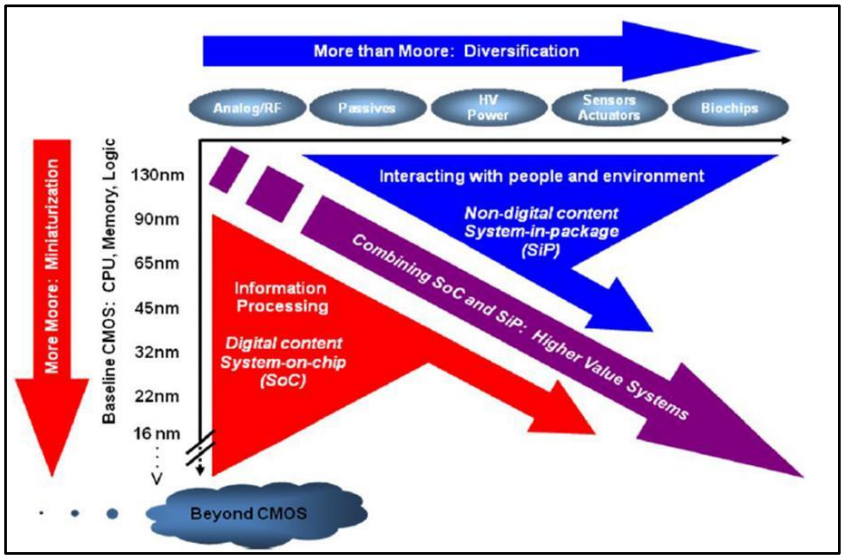


Fig. 1-3 Microelectronics packaging roadmap covering single chip, 2.5/3D stack, embedded active/passive, and printed electronics technologies.

The ITRS projects that by 2020–2025, many physical dimensions are expected to be crossing the 10 nm threshold. It is expected that as dimensions approach the 5–7 nm range it will be difficult to operate any transistor structure that is utilizing CMOS physics as its basic principle of operation. It is also expected that new devices, like the very promising tunnel transistors, will allow a smooth transition from traditional CMOS to this new class of devices to reach these new levels of miniaturization. However, it is becoming clear that fundamental geometrical limits will be reached in the above timeframe. By fully utilizing the vertical dimension, it will be possible to stack layers of transistors on top of each other. This 3D approach will continue to increase the number of components per square millimeter even when horizontal physical dimensions will no longer be amenable to any further reduction.

ITRS recognized the limitations of Moore's law (i.e., linear scaling) and proposed a methodology to identify those MtM technologies for which a roadmapping effort is feasible and desirable. The semiconductor community needs to depart from the traditional scaling "technology push" approach and involve new constituencies in its activities. ITRS materialized this new approach in 2011, when it added a MEMS chapter to the roadmap, and also aligned it with the iNEMI roadmap. The micro-electro-mechanical systems (MEMS) chapter aligns its effort towards those MEMS technologies associated with "mobile internet devices," a driving application broad enough to incorporate many existing and emerging MEMS technologies.

The limitation of Moore's law, increased costs of lithograph steps and wafer processing, are also driving the industry to find alternatives to improve the performance and functionality of electronic devices, lower the cost. Some experts predicts that significant technological advancement occurs through exponential system performance when the machines can do cognitive tasks more effectively than any human. Either way,

the need to integrate disparate technologies (logic, memory, RF, sensors, etc.) in small form factors is driving the industry to 3D integration as a solution for the advancement. For example, due to lack of technology readiness and cost, 2.5D technology (passive interposer) was first developed to be a bridge technology to 3D ICs, and has grown to be a package platform that is expected to co-exist alongside 3D ICs. Unlike in 3D-ICs, 2.5D technology (a.k.a., TSV-less) only the interposer, and not the dies themselves, needs through silicon vias (TSVs) to connect active die with package substrates. This allows for the use of existing die designs. These technologies are discussed in details in subsequent chapters.

1.2.2. iNEMI roadmap

iNEMI has been creating and exploiting technology roadmaps for the electronics industry for more than two decades. It projects trends for future opportunities and challenges for the electronics manufacturing industry. The roadmap is updated every two years, covering technology development and deployment by predicting future packaging, component and infrastructure challenges as well as describing critical technical and business elements required to support industry growth. The projects deliver solutions to identified gaps that allow the industry to continue on its fast paced speed. The iNEMI forms technology working groups (TWGs) to address the technology gaps.

The pace of change in packaging technology today has accelerated to the highest rate in history. Communication, transportation, education, agriculture, entertainment, health care, environmental controls (heating and cooling), defense, and research all rely heavily upon electronics today. This diversity of application and the never ending demand for both lower cost and higher performance cannot be achieved without major changes in architecture, materials and manufacturing processes. Today, these new technologies include SiP, wafer level packaging (WLP), wafer thinning, and through silicon vias (TSVs). In the near future, we will see additional changes with the incorporation of nano-materials.

Multi-core processors are now the norm for most computing applications. A consequence of the expected demise of the traditional scaling of semiconductors is the increased need for improved cooling and operating junction temperature reduction due to large leakage currents. The consumer's demand for thin multifunctional products has led to increased pressure on alternative high density packaging technologies. High-density three-dimensional (3D) packaging of complete functional blocks has become the major challenge in the industry.

- RF System-in-Package (SiP) applications have become the technology driver for small components, packaging, assembly processes, and high density substrates.
- The use of motion-gesture sensors in various consumer and portable devices has expanded the MEMS
- Gyroscope enables portrait-landscape mode (both 2D-axis and 3D-axis) is expected to see an exponential growth.
- Performance requirements such as increased bandwidth and lower power are driving 3D integrated circuits (ICs) designed with through silicon vias (TSV).

The need for continuous introduction of complex, multifunctional new products to address the converging markets (first identified in 2004) has continued to favor the development of functional, modular components or SiP (both 2D and 3D structures). This paradigm shift in the design approach increases the flexibility, shortens the product

design cycle, and places the test burden on the producers of the modules. Major paradigm shifts identified in the recent iNEMI roadmap include:

- Cloud-connected digital devices with sensors
- Optical interconnection
- Revolutionary transition in packaging technology
- Supply-chain infrastructure development while minimizing risk
- Next generations of fiber technology to keep up with capacity
- Wafer level packaging has come of age

In addition to the conventional packaging technology trend, iNEMI added printed electronic technology in its forecasting. For example, the 2013 iNEMI's "Large Area, Flexible Electronics Roadmap" chapter is building upon the 2011 first edition [2]. It added a comprehensive update based on a number of announcements made by industry since the previous publication. In addition, the iNEMI team identified paradigm shifts, enablers, and show stoppers. One key paradigm is the transition from the beginning of the 21st Century vision for completely printed electronic products to 'hybrid' products, where traditional electronic components are used in combination with printed components.

Other paradigm shifts include cost per area of functionality versus cost per function for silicon chip and integration of electronics in non-traditional objects and locations – ubiquitous electronics. A few gaps and show stoppers are also identified and presented. For example, it states that the rate of commercialization of materials and manufacturing/ processing equipment is occurring too slowly to meet the cost/performance/utility demands to enable near-term product launches Additionally, the rate of development of systems must accelerate—otherwise a window of opportunity may be lost for a disruptor to commercialize a new competitive product.

Seven areas of opportunity were identified by an industry survey performed by the iNEMI team. Those surveyed further predicted that the near-term commercialization opportunities will continue to be lighting, power (battery), and sensors (biological, chemical, and touch) followed later by the introduction of radio frequency (RF) devices (anti-tampering and authentication), photovoltaics, and displays. As with silicon-based component/subsystem technologies, it is envisioned that the technology and applications will mature over time, offering additional opportunities for integration into product emulators. As an example, as these technologies become more robust, it is possible that memory products may be developed for the aerospace and defense industries.

Near-term opportunities are classified as either (1) non-hybrid—an application that is comprised of only the emerging technology or (2) hybrid—an application that is manufactured using traditional electronics and devices, circuits, or components based on the new technology, e.g., a product with a printed display module and a silicon IC RF front-end. For non-hybrid application, one technical barrier concerns the development of in-line manufacturing quality control equipment. To benefit from the economies of scale that roll-to-roll (R2R) and printing offers, systems must be developed and qualified for testing of the fabricated devices, circuits, and components.

Conversely, hybrid flexible electronics systems comprised of printed electronics-based components (sensors, power, indicators, signage) integrated with traditional electronics (surface mount technology for passive devices and silicon based ICs) continue to receive greater attention for near-term commercialization opportunities. In order to achieve further commercialization, a dedicated, hybrid manufacturing platform must be developed. iNEMI

envisions that an R2R manufacturing platform combining several printing technologies (e.g., flexography, gravure, and micro dispensing) is required to enable realization of the market potential.

1.2.3. IPC roadmap

The IPC has been creating and exploiting technology roadmaps for the electronics industry for more than two decades; the first roadmap was published in 1993 and updated in 1994. Even though these documents did not follow the traditional roadmap format, but were more or less a compendium of needs of the industry looking ahead 4 years. The 1995 IPC roadmap was designed using classic timeline models with eight emulator OEM products. The 2000–2001 roadmap included 11 emulator products. The emulators were reconfigured to include information on four different topics: design issues, board fabrication issues, assembly issues, and purchasing trends. For the first time components and component substrate technology was incorporated. The 2013 roadmap becomes a departure by selecting emulators from the end-use application matrix, even though it attempted to match the definition by the OEM in the iNEMI roadmap.

The IPC roadmap is a resource for companies throughout the global electronics manufacturing industry who are embarking on business, technology, and strategic planning for the near and long term. The recent IPC roadmap concentrates on the "operational" segment of the electronic interconnect market, IPC always recommends that users consider the input from other roadmaps where it may pertain to their specific situation. New features of the IPC roadmap include a "stewardship" section that provides expanded content and scope, with an emphasis on true sustainability; explanation of new business models an expanded coverage of the printed electronics industry as it matures into a viable technology.

In summary, the ITRS is an emerging technology roadmap; it looks at a "technology push" covering the progress of technology and question as what products can be developed. This roadmap lacks the broader product context provided by the product technology roadmap. The product-technology roadmap is driven by product/process needs. This is the most common type of roadmap. A product-technology roadmap can be linked to "technology push" or "market pull." IPC and iNEMI are "market pull" roadmaps, which define desired products and asks what technologies are needed to support them.

1.2.4. OE-A roadmap

The OE-A, a working group within VDMA, was organized a few years ago to create a communication and development interface for various fields of research. It represents the entire value chain of organic electronics, from the materials supplier and equipment and product manufacturer through to the user. The OE-A's goal is to issue roadmaps that serve as guides to the multitude of technical developments and help to define possible applications. While many of the developments of OE-A members are still in the test phase in the lab, a whole series of practical applications are already in use. The OE-A has published four roadmaps. An adapted summary version of the 4th map, which projects near-term to long-term growth and applications, is schematically shown in Fig. 1-4. Here, the technology related to lighting and display are bundle together rather shown separately.

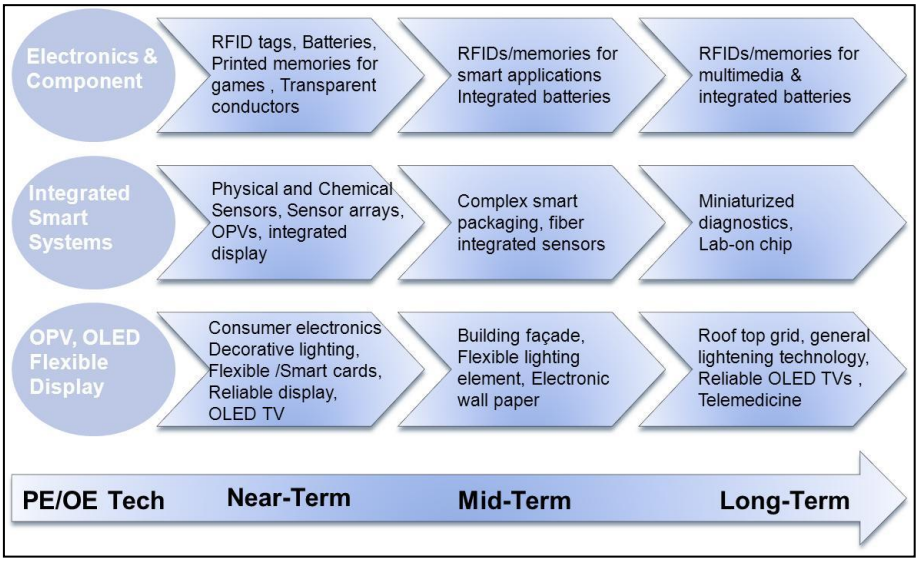


Fig. 1-4 iNEMI 2013 roadmap identification of paradigm shifts and enablers [2].

The three key areas defined are:

1. Electronics and components covering radio frequency identification, batteries, printed memory for games, and transparent conductors
2. Integrated smart systems including physical and chemical sensors, sensor arrays, and integrated displays
3. Organic photovoltaic (OPV), organic light emitting diode (OLED), and flexible displays, which encompass a large number of applications in consumer electronics, lighting, and flexible/smart cards

The OE-A has published the sixth edition of its roadmaps in 2015 with discussing key trends and challenges as shown in the following.

- OLED displays have become a true mass market item in mobile displays and are starting to penetrate the TV market
- Major industry sectors, such as automotive, consumer electronics, white goods, pharmaceuticals, and health care and packaging, have embraced organic electronics and are bringing products to the market
- Flexible, lightweight, mobile electronic products are gaining a larger position in the market, enabled by organic electronics
- Mobility of organic semiconductors and efficiency of OPV materials are continuing to increase rapidly, and becoming competitive with poly-Si is starting to look achievable
- Patterning processes are being scaled to smaller dimensions and improved registration
- Integration of printed and silicon based components to make hybrid systems is becoming more and more a subject of interest and looks to be one of the primary paths to further commercialization in the coming few years
- The industry is entering a phase of realistic growth, with significant revenues and with products appearing in more and more application areas

The 2015 OE-A roadmap team identified the following key challenges (a.k.a., Red Brick Wall) for which major breakthroughs are needed.

- Processes: resolution, registration, uniformity and characterization.
- Encapsulation: flexible transparent barriers at low cost.
- Materials: improvement of electrical performance, processability and stability.
- Development of appropriate standards and regulations for organic electronics.

2. SINGLE-CHIP PACKAGES

2.1. Introduction

Continuous significant changes are underway in the smart phones, mobile, computer, telecommunication, automotive, and consumer electronics industries. The common and pervasive requirements in all of these electronics are (1) ultra-low-cost, (2) thin, light, and portable, (3) very high performance, (4) diverse functions involving a variety of semiconductor chips and packaging, and (5) user friendliness. The packaging technologies are now considered to be the key enabler for system level microelectronics implementation. Packaging is designed to accommodate the lagging miniaturization of printed circuit board (PCB) since such miniaturization add significant cost of the final product.

For this reason, electronics functional chips are transformed by packaging scheme that enlarge the features for ease of assembly as well as protecting from environment. Fig. 2-1 shows schematically the purpose of microelectronics package from BGA to wafer level package (WLP) — molded and a more recent fan-out configurations. An interposer is used to accommodate the fine pitch of the chip as well as the next level interconnection, e.g. PCB.

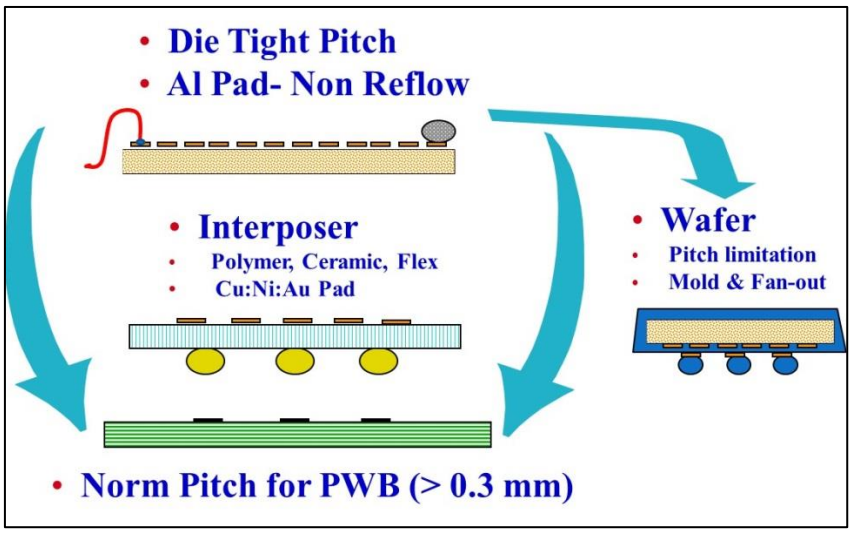


Fig. 2-1 Single-chip packaging concept from wire-bond to flip-chip ball grid array to wafer-level packaging (fan-in and fan-out).

In addition to ease-of-testing and assembly role, the packaging has the following features:

- Signal distribution, involving mainly topological and electromagnetic consideration
- Power distribution, involving electromagnetic, structural, and materials aspects
- Heat dissipation (cooling) , involving structural and materials consideration
- Protection (mechanical, chemical, electromagnetic) of components and interconnections

Furthermore, an electronic package must also function at its design performance level while still allowing for product that is high quality, reliable, serviceable, and economical.

Fig. 2-2 categorizes single-chip microelectronic packaging technologies into three key technologies: (1) plastic ball grid arrays (PBGAs), (2) ceramic column grid arrays (CGAs or CCGAs), and (3) and smaller foot-print wafer-level packages. There are numerous variation of packages in each category that will be discussed in the following sections.

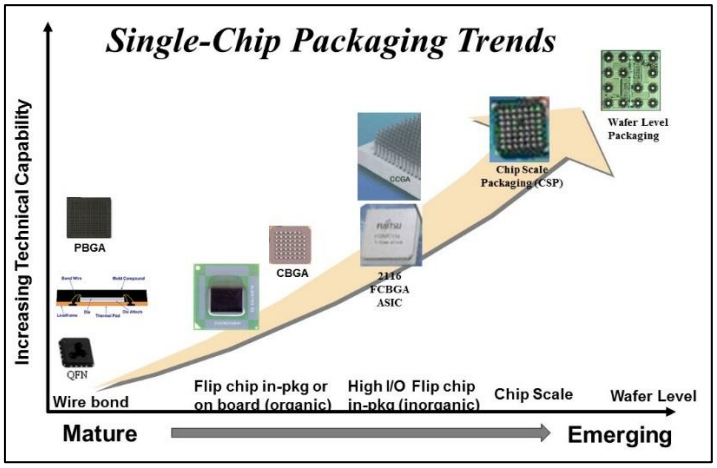


Fig. 2-2 Single-chip packaging trends from ball grid array (BGA) to wafer level packages (Fan-in or Fan-out).

PBGAs and chip scale packages (CSPs) are now widely used for many commercial electronic applications, including portable and telecommunication products. BGAs with 0.8-1.27-mm pitches are implemented for high-reliability applications, generally demanding more stringent thermal and mechanical cycling requirements. The plastic BGAs introduced in the late 1980s and implemented with great caution in the early 1990s, further evolved in the mid-1990s to the CSP (also known as a fine-pitch BGA) having a much finer features from 0.4-mm down to 0.3-mm pitches.

To accommodate higher I/O single-chip die, the flip-chip BGA (FCBGA) was developed. The FCBGA is similar to the PBGA, except that internally a flip-chip die rather than a wire-bonded die is used. Because of these developments, it has become even more difficult to distinguish different area array packages by size and pitch; its internal die attachment configuration should also be considered. The ultimate size reduction can be achieved by protecting single die at the wafer level, hence introduction of wafer level package (WLP). WLPs also addresses the key issues of using single bare die, and it improves ease of handling and functional testing.

For high-reliability applications, ceramic and hermetic packages of area array packages were implemented. The ceramic BGA (CBGA) package uses a higher melting ball ($Pb_{90}Sn_{10}$) with eutectic attachment to the die and board. Contrary to the PBGA version, the high-melt ball does not collapse during solder interconnection reflow, hence, a control standoff height for improved reliability. The column grid array (CGA) or ceramic column grid array (CCGA) is similar to a CBGA except that it uses column interconnects instead of balls; hence it has higher flexibility for improved reliability. The lead-free CGA uses copper instead of high-melting lead/tin column. The flip-chip BGA (FCBGA) is similar to the BGA, except that internally a flip-chip die rather than a wire-bonded die is used.

R. Ghaffarian [5-12] has published extensive work on the subject of BGA, PBGA, CSP, FPGA, and CGA assembly and reliability and provided challenges associated with the area-array packaging technology implementation for high-reliability applications. The work has covered process optimization, assembly reliability characterization, and the use of inspection tools (including x-ray and optical microscopy) for quality control and damage detection due to environmental exposures. The following sections summarize a number of these packaging technologies.

2.1.1. Ball Grid Array (BGA)

Ball grid arrays (see Fig. 2-3), with 1.27-mm pitch (distance between adjacent ball centers) and finer pitch versions with 1- and 0.8-mm pitches, are the only choice for packages with higher than 300 I/O counts, replacing leaded packages such as the quad flat pack (QFP). BGAs provide improved electrical and thermal performance, more effective manufacturing, and ease-of-handling compared to conventional surface mount (SMT) leaded parts. Finer pitch area array packages (FPBGA), also known as CSPs, are further miniaturized versions of BGAs, or smaller configurations of leaded and leadless packages with features generally less than 0.8-mm pitches.

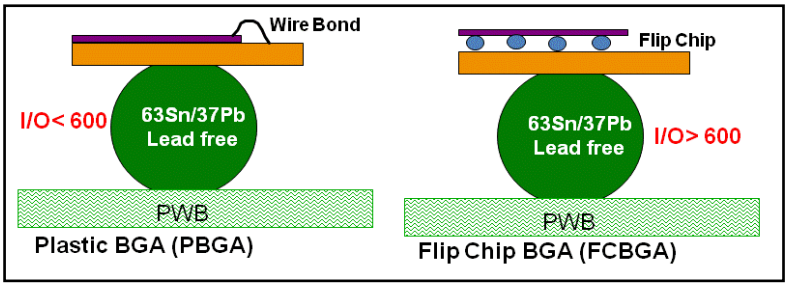


Fig. 2-3 Typical plastic ball grid array with internal wire-bond and flip-chip die for low and high-I/O package configurations, respectively.

2.1.2. Column Grid Array (CGA)

For high-reliability applications, surface mount leaded packages, such as ceramic quad flat packs (CQFPs), are now being replaced with CGAs with a 1.27-mm pitch (distance between adjacent ball centers) or less. Replacement is especially appropriate for packages with greater than 300 I/O counts where CQFP pitches become smaller, making them extremely difficult to handle and assemble. In addition to size reduction, CGAs also provide improved electrical and thermal performance; however, their solder columns are

prone to damage, and it is almost impossible to rework defective solder joints. Rework, re-column, and reassembly may be required to address solder defects due to processing or column damage prior to assembly due to shipping and mishandling.

CGA packages are preferred to CBGA (see Fig. 2-4) since they show better thermal cycle solder-joint reliability than their CBGA counterparts. Superior reliability is achieved for larger packages and for greater than 300 I/Os when resistance to thermal cycling is further reduced with increasing package size. All ceramic packages with more than about 1000 I/Os come in the CCGA style with 1.0-mm pitch or lower in order to limit growth of the package size.

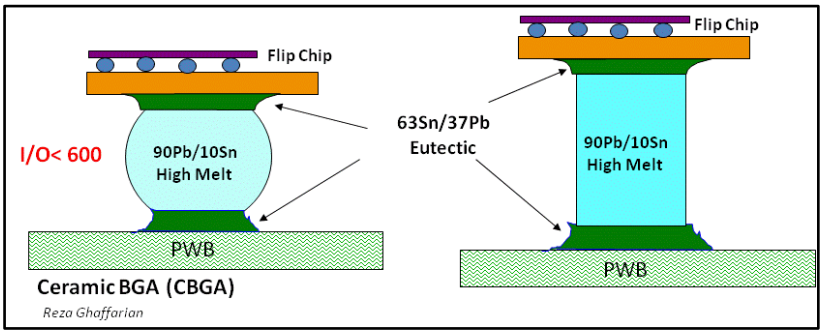


Fig. 2-4 Typical plastic ball grid array with internal wire-bond and flip-chip die for low and high-I/O package configurations, respectively.

Key recent trends in electronic packages for high-reliability applications are as follows:

- Ceramic quad flat pack (CQFP) to area array packages
- CBGA to CCGA/CGA (>500 I/Os) and land grid array (LGA)
- Wire-bond to flip-chip die within a package
- Hermetic to non-hermetic packages (>1000 I/Os)
- High-lead solder columns to columns with Cu wrap
- Pb-Sn to Pb-free, including potential use of a Cu column
- Land grid with conductive interconnects rather than Pb-free solder

2.1.3. Class Y- Non-hermetic Flip-chip CGA (FC-CGA)

S. Agarwal [13] reported that significant activities were carried out in recent years to address the non-hermetic flip chip CGA for use in high-reliability applications. The specification was updated to ensure that new requirements be added to cover all aspects of the packaging configuration including flip-chips, underfills, adhesives, and column attaches as well as introduction of the new test methods.

2.1.4. FLIP CHIP IN PACKAGE (FCIP)

Flip-chip assembly is fast becoming the assembly method of choice over wire-bond to connect a chip to a substrate (or package). The flip chip in package technology has been widely used in high performance FCIP applications for more than a decade. Elements of its success can be attributed to the establishment of high yield assembly processes and formulation of advanced underfill materials systems for high-reliability. It is widely known that underfills help to mitigate the effects of large coefficient of thermal expansion (CTE)

mismatches between silicon chips and organic substrates. To meet the demand for high I/O counts in high-performance and high-bandwidth applications, flip-chip I/O pitch needs to be reduced continuously.

Reduction of I/O bump dimension also raises significant challenges to package substrate technologies. Compared to other types of substrates, a silicon package has the advantages of excellent planarity, fine-pitch wiring, and matched CTE for Si chips. The key elements of an Si carrier include ultra-fine pitch interconnection capability, known-good die testability, as well as reworkability. Micro C4s can be fabricated through various methods, such as micro screen printing, molten solder ejection method (MSEM), or photolithographic electroplating.

2.1.5. CHIP SCALE PACKAGE (CSP)

The trend in microelectronics has been toward ever increasing numbers of I/Os on packages, which is, in turn, driving the packaging configuration of semiconductors. Key advantages and disadvantages of CSPs compared to bare die are listed in Table 2-2. Chip scale packaging can combine the strengths of various packaging technologies, such as the size and performance advantage of bare die assembly and the reliability of encapsulated devices.

The advantages offered by chip scale packages include smaller size (reduced footprint and thickness), lesser weight, a relatively easier assembly process, lower overall production costs, and improvement in electrical performance. CSPs are also tolerant of die size changes, since a reduced die size can still be accommodated by the interposer design without changing the CSP's footprint.

CSPs have already made a wide appearance in commercial industry as a result of these advantages, and now, even their three-dimensional (3D) packages are being widely implemented. Unlike conventional BGA technology at typically 0.8–1.27 mm pitch, CSPs utilize lower pitches (e.g., currently, 0.8 to 0.3 mm) and hence, will have smaller sizes and their own challenges.

Table 2-2 Pros and cons of chip scale package (CSP).

Pros	Cons
Near chip size	Moisture sensitivity
Widely used	Thermal management ▪ Limits package to low I/Os
Testability for known good die (KGD)	Electrical performance
Ease of package handling	Routability ▪ Microvia needed for high I/Os ▪ Pitch limited to use standard PWB
Robust assembly process ▪ Only for an area-array version	Reliability is poor in most cases
Accommodates die shrinking or expanding	Underfill required in most cases to improve reliability.
Standards	Array version ▪ Inspectability ▪ Reworkability of individual balls
Infrastructure	
Rework/package as whole	

2.1.6. Flip Chip on board [FCOB])

Flip-chip assembly is fast becoming the assembly method of choice over wire-bond to connect a chip. Direct attachment of flip chips on board (FCOBs) with fine-pitch solder bumps are being increasingly used to address performance, power, size, and I/O requirements. FCOBs require underfills to ensure solder bump reliability. However, added processing costs associated with underfill dispensing and curing, add challenges especially for fine-pitch assemblies. Reliability concerns due to underfill delamination make FCOBs a less likely option for future generations of microelectronic packaging. Furthermore, when low-K dielectric material (ultralow-K dielectric in the future) is used in the IC and when such ICs are assembled on organic substrates, the stiff solder bumps could crack or delaminate the low-K dielectric material under thermal excursions.

2.1.7. Wafer Level Packages (WLP) or Wafer Level Chip Scale Package (WLCSP)

Microelectronic packaging continues the migration from wire-bond to flip-chip first level interconnect (FLI) to meet aggressive requirements for improved electrical performance, reduced size and weight. For wafer bumping, solder electroplating is commonly employed, especially for fine pitch applications. Wafer level chip scale packaging (WLCSP) typically utilizes solder sphere placement technology to manufacture the bumps. In WLCSP, pitch and solder ball size are usually much higher and the number of I/O much lower than for flip chip in package (FCiP) applications. However, many companies plan to use WLPs for higher pin count applications, including analog parts with larger die sizes. This will increase the number of wafers to be processed, as well as the unit volumes. The memory die is one example of a large die whose adoption significantly increases the number of wafers.

One of the major drivers for the adoption of WLPs in portable products is form factor, and mobile phones increasingly contain WLPs, representing the largest single product application. Demands for greater functionality in smaller spaces is driving the adoption of WLPs in mobile phones faster than in any other segment of the market.

Fan-out wafer level package (FOWLP), a newly introduced WLP, is projected to grow rapidly within the next few years. Fan-out WLP are "re-configured" by placing known good ICs active face down on a foil and by over-molding them. These wafers are then flipped and processed in the wafer fab with redistribution layer (RDL), ball placing, and diced. Unlike fan-in WLP which has been commercialized since the late 1990's, FOWLP is not constrained by die size, and thus can offer an unlimited number of interconnects for maximum connection density. One can also achieve finer line/spacing, improved electrical and thermal performance and small package dimensions to meet the relentless form factor requirements and performance demands of the mobile market.

J.H. Lau [14] reviewed patents on CSP style packages with focus on lead frame, organic substrate with solder ball, fan-in and fan-out WLP. It also provided key advantages of FOWLPs over PBGAs and fan-in WLP. The key advantages of FOWLP over PBGA packages with solder-bumped flip chip are their lower cost, lower profile by eliminating the substrate and wafer bumping, lower process steps by eliminating the flip-chip reflow and flux cleaning and removing the underfill requirement. Also, FOWLP packages show better electrical and thermal performance and easier to implement for system-in-package (SiP) and 3D IC packaging. The latter characteristics also are true when FOWLP is compared to fan-in WLP. Other advantages include better wafer yield and using known good die (KGD) as well as enabling higher pin counts and embedding integrated passives.

2.1.8. Land-Grid-Array (LGA) Packaging Trend

Land-grid array (LGA) packages have been increasingly used in portable electronics and wireless products because of their low profiles on the printed wiring/circuit boards (PWB/PCB) and their direct Pb-free assembly process compatibility. Since LGA has a lower standoff height and different material properties compared with the conventional BGA package; its reliability behavior become of concern. A major concern is the board-level solder-joint reliability of the LGA packages under thermal loading. For high-reliability applications, this approach may become a popular approach with a much wider commercial industry implementation of restriction of hazardous substances (ROHS).

LGA in plastic package version with low I/O and sizes has been available for thinner consumer products because of lower cost and lower assembly standoff compared to ball-grid-array versions. In some cases, the LGAs are optimized for improved radio-frequency (RF) performance for wireless applications.

2.1.9. Conventional leadless packaging trends

In a 2003 paper [15], the authors stated that within the last few years, the QFN package has taken industry by storm and that the industry had already shipped one billion parts. Fig. 2-5 shows a number of early generation of leadless packaging configurations including the MicroLeadFrame® package (MLF®), which were introduced more than a decade ago.

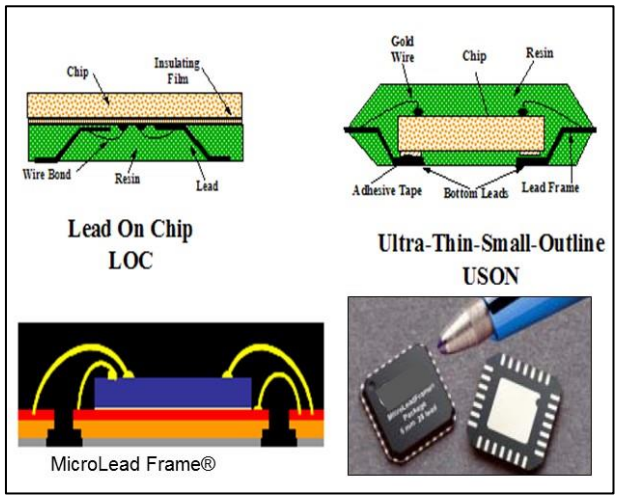


Fig. 2-5 Infusion of New Technology into the QML System G12 Class Y Effort at a Glance.

2.10. Advanced leadless packaging trends

IPC, the Association Connecting Electronics Industries [3] recently released the IPC 7093 specification, "Guidelines for Design and Assembly Process Implementation for Bottom Termination Components," covering the rapidly growing leadless packaging categories. The BTC is a generic term for packaging technologies which their external connections consist of metallized terminals that are an integral part of the package body

and intended for surface mounting. This class of components includes quad flat no-lead (QFN), dual-row/multi-row QFN (DRQFN/MRQFN), dual flat no lead (DFN), and land grid array (LGA). The standard describes the critical design, assembly, inspection, and reliability issues associated with BTCs.

Recently, A. Tseng, et al. presented information on an area array version of QFN, called advanced QFN (aQFN) package [16]. The aQFN is an improved version of conventional QFN with multiple row terminals accommodating higher number of I/Os. The number of I/Os become similar to that of CSP/FBGA packages with the advantage of lower cost for portable and telecommunication applications. The multiple-row QFNs; however, are more difficult to assemble, there are more opportunities for solder-joint bridging especially when pitch is smaller, and there are higher potential for risk due to thermo-mechanical environmental exposures. The thermo-mechanical solder-joint reliability of aQFN was improved by modifying packaging processes including double-sided etching of copper lead frame to create isolated copper posts with higher standoff.

3. Stack Packaging Technologies

3.1. Introduction

The demand for high-frequency operation, high-input/output (I/O) density, and low parasitic, as well as the need for package-level integration with small form factors and extreme miniaturization, have led to numerous 2.5D and 3D packaging technologies [see Fig. 3-1]. The vertically integrated 3D packages combine conventional flip-chip and wire-bond interconnection, build-up, and laminate substrates, and bring about package-level integration of disparate die and device functions through die or package stacking.

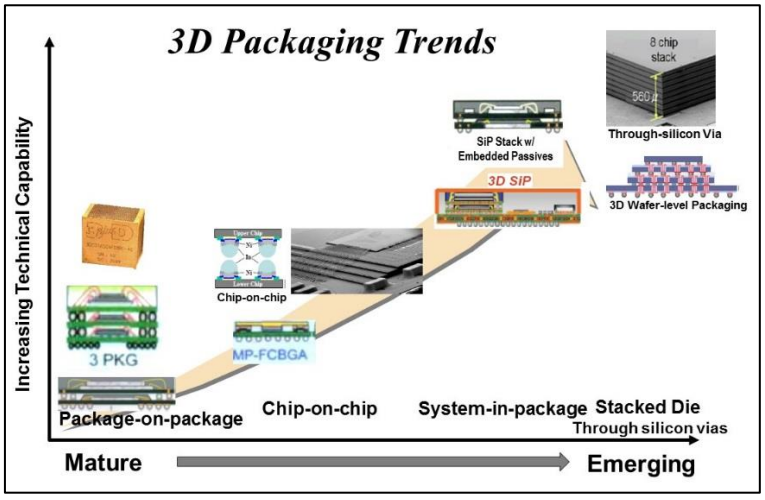


Fig. 3-1 2.5/3D packaging technologies showing conventional to advanced configurations.

From the existing 3D packaging technology options, wire-bonding is well developed for use in low-density connections of less than 200 I/Os per chip. This technology has limitations in meeting the increasing frequency requirements and increasing demands for

higher interconnection due to limitation of peripheral wire-bonding. In order to overcome such wiring connectivity issues, multiple flip-chip die with passive redistribution interposed have been introduced by industry for high-end applications. Ultimately the 3D chip stacking technology using through-silicon vias (TSVs) is being pursued by industry since it offers the possibility of solving serious interconnection problems while offering integrated functions for higher performance.

3.2. 3D Conventional Packaging Trends

For high-density packaging, the migration to conventional interconnection 3D, more than "Moore", has become mainstream. Even though initially conventional 3D packaging included leaded stack configuration, the trend is more towards area array interconnections. The conventional 3D packaging (see Fig 3-2) consists of stacking of packaged-devices, known as package-on-package (PoP), and stacking of die within a package, known as package-in-package (PiP) or system-in-package (SiP). Numerous variation of PoP and PiP technologies are in use today including staking of packages by using through mold via (TMV™) interconnection technology. The following sections provide further discussions on specific conventional and 3D packaging technologies.

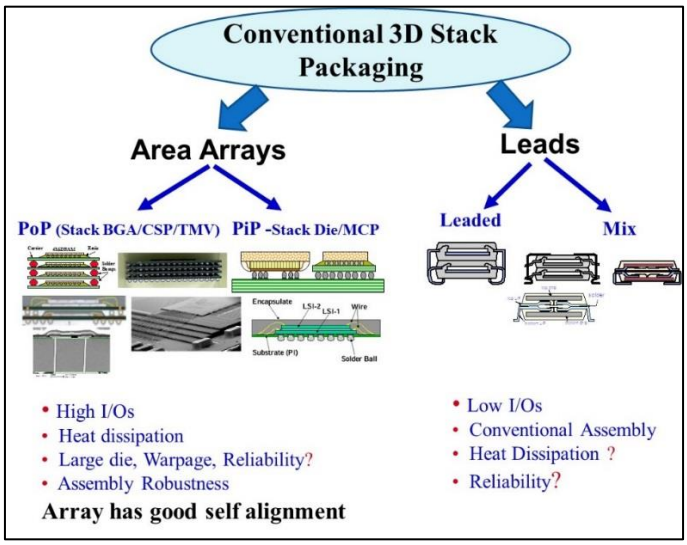


Fig. 3-2 2.5/3D packaging technologies showing conventional to advanced configurations.

3.2.1. Package-on-Package (PoP)

PoP is a packaging technology placing one package on top of another to integrate different functionalities while still remaining compact in size. This packaging technology offers procurement flexibility, lower cost of ownership, better total system costs, and faster time to market. typically, designers use the top package for memory application and the bottom package for application-specific integrated circuits (ASICs), baseband, or

processor applications. By using this technology, the memory known-good-die (KGD) issue can be mitigated since the memory to be integrated with the bottom package can be burned-in and tested before integration. PoP also answers issues with wafer thinning, die attach, wire-bond, and thermal dissipation. Three categories of the stack technologies are: (1) PoP with center mold and flip chip, (2) PoP with partial cavity structure, and (3) through-mold via (TMV™).

The TMV™ uses a matrix-molded platform for bottom PoP construction and creates through-via interconnections to the top surface via a laser ablation process [17]. Fig 3-3 illustrates the key elements of the bottom TMV™ PoP developed by the package supplier for their internal qualification and joint SMT studies. The 14 × 14 mm daisy-chain package incorporates a 200 I/O, 0.5 mm pitch top side interface, and 620 bottom BGAs at 0.4-mm pitch.

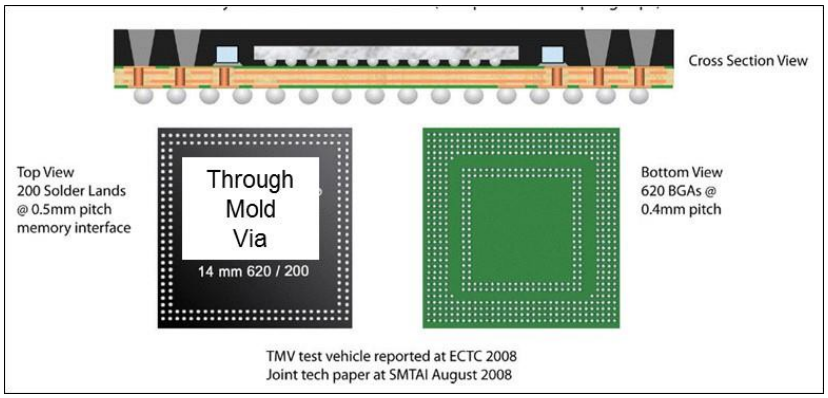


Fig 3-3 Cross-section top and bottom view of a new TMV™ PoP package [19].

The benefits of TMV™ technology include the following:

- Removes the pitch vs. package clearance bottlenecks to support future memory interface density requirements enabling the memory interface to scale with CSP pitch reduction.
- Improves warpage control and bottom package thickness reduction requirements by utilizing a balanced fully molded structure.
- Provides an increased die-to-package size ratio.
- Supports wire-bond, flip-chip, stacked die, and passive integration requirements.
- Leverages strong technology roadmaps and high-volume scale, from fine-pitch ball grid array (FBGA), stacked die, flip-chip CSP, and SiP platforms.
- Integrates proven laser ablation technology available from a host of laser process equipment suppliers.
- Expected to improve board-level reliability of the stacked memory interface using rules developed by package supplier.

3.2.2. Package-in-Package (PiP)

Handsets and other mobile handheld products are defining a new application for packaging technology that goes beyond the realm of traditional packaging. The optimum solution often lies in a judicious combination or hybridization of these seemingly dissimilar technologies and approaches. One such package is often called PiP. PiP with wire-bonded stack die is well established. Vertical chip stacking can be performed as chip-to-chip, chip-to-wafer, or wafer-to-wafer processes. Stacked die products inside a package results in the thinnest package with the highest board-level reliability and lowest assembly cost. Most of the time, stacked die are multiple memory chips and rarely mixed device types, such as stacked memory with logic devices added. Special low-profile wire-bonding has been developed and is a critical process for this technology.

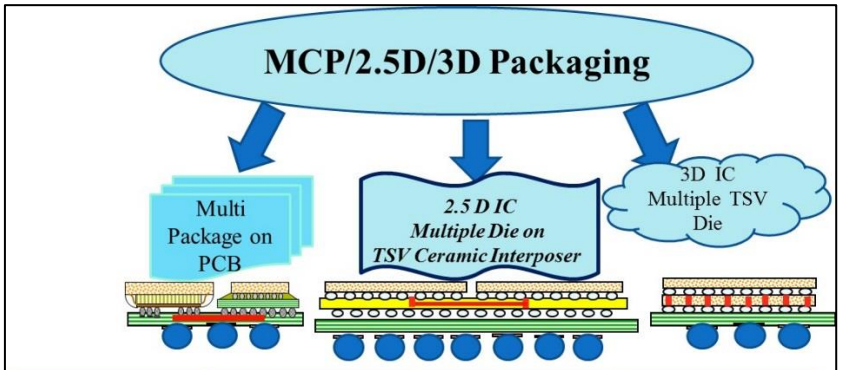
Stacked die concepts utilizing silicon spacers or epoxy filled with spherical spacers have been used. In the silicon-spacer concept, a thin piece of silicon is used to separate the active dies in the stack. In the glue-spacer concept, this is accomplished with a spherical-filled die-attach. Adding silicon into the package increases the bending resistance. Associated with this is the increased risk and/or propensity for cracks during assembly and/or reliability/qualification testing, either in the package body (molding compound) or in the die itself.

Flip-chip bonding is also used in PiP interconnection, either on its own or as a complement to wire-bonding. Flip-chip configuration may be applied to either the upper die or the lower ones, depending on the intent of the design. Flip chipping a bottom die directly onto the substrate enables that die to operate at a high speed. On the other hand, flip chipping a top die eliminates the use of long wires for connection to the substrate.

3.3. 2.5D/3D TSV Packaging Trends

Conventional 3D packaging technologies have limitation in meeting system performance, throughput, and power requirements. Although PiP and PoP packaging technologies allow for two or more chips and packages to be interconnected, they do not offer enough density, bandwidth or power to meet the requirements of next generation product roadmaps. The trade-offs between placing more functions on a chip (system-on-chip, SoC) versus placing more functions within a package (multi-chip package, MCP, or system-in-package, SiP) must be fully evaluated. Optimizing overall performance as well as total cost-of ownership are equally important. And perhaps one of the most significant issues is accelerating time-to-market, as it is a strategic enabler to the end users.

Fig. 3-4 compares the performance advantages of 2.5D/3D ICs to standard packages on a PCB; their relative interconnect density, thermal resistance, and power usage. A 2.5D IC package is a cost- and functional-effective interim solution instead of full 3D through silicon via (TSV) 3D packaging methods. The 2.5D packaging is defined by the use of a multilayer passive silicon interposer (TSV-less)—contrary to active interposer in 3D with TSV—as a substrate to interconnect multiple active die or die stacks in a side-by-side configuration. In a 3D IC TSV stack, solder bumps are used to join one die on top of another die (active) to allow the signals to travel between the die.



Performance	MPP (MCP)	2,5 D IC	3D IC
Density Index	1	~ 1 X	~ 10 X
Thermal Resistance factor	1	1	> = 2
Watt/Aggregate Bandwith	1	0.01 0.001	0.001 0.0001

Fig. 3-4 2.5/3D packaging technologies showing conventional to advanced configurations.

3.3.1. 2.5D (Passive TSV Interposer or TSV-less) Packaging Trends

The use of passive TSV interposer is key in 2.5D technology. In production of high I/O implementation, e.g., 2.5D TSV approach for Virtex-7 FPGAs, K. Saban [18] presented that TSVs are used to route the signals through the silicon interposer down to flip-chip solder bumps located on the interposer's bottom side. This device has four FPGA chips attached to a silicon interposer, which supports ~10000 silicon-speed connections between adjacent chips. The ICs themselves use much smaller copper (Cu) pillar micro-bumps for assembly onto the silicon interposer. For example, the 2.5D FPGA with a passive TSV addresses two key requirements of the programmable die and packaging challenges. Stacked silicon interconnect (SSI) technology interposer breaks the limitations of Moore's law by using multiple smaller die rather one large die. It also enables reducing the time required to deliver the largest FPGAs with the highest bandwidth in the quantities needed to satisfy end-customer volume production requirements.

System-on-chip (SoC) design is unable; however, to address these key technological challenges. An SoC comprises millions of gates connected by complex networks of wires in the form of multiple buses, complicated clock distribution networks, and multitudes of control signals. Successfully partitioning an SoC design across multiple FPGAs requires an abundance of I/Os to implement the nets spanning the gap between FPGAs. With SoC designs including buses as wide as 1,024 bits, even when targeting the highest available pin count FPGA packages, engineers must use data buffering and other design optimizations that are less efficient for implementing the thousands of one-to-one connections needed for high-performance buses and other critical paths.

Packaging technology is one of the key factors to this I/O limitation. The most advanced packages currently offer approximately 2000 I/O pins, far short of the total number of I/Os at the flip-chip die level. At the die level, I/O technology presents another

limitation because I/O resources do not scale at the same pace as interconnect logic resources with each new process node. When compared to transistors used to build the programmable logic resources in the heart of the FPGA, the transistors comprising device I/O structures must be much larger to deliver the currents and withstand the voltages required for chip-to-chip I/O standards. Thus, increasing the number of standard I/Os on a die is not a viable solution for providing the connections for combining multiple FPGA die. Stack silicon interconnect (SSI) technology solves the following key challenges:

- The amount of available I/O is insufficient for connecting the complex networks of signals that must pass between FPGAs in a partitioned design as well as connecting the FPGAs to the rest of the system
- The latency of signals passing between FPGAs limits performance
- Using standard device I/Os to create logical connections between multiple FPGAs increases power consumption

J. Casey [19] summarized the current state of interposer substrates as shown in Table 3-3. It was stated that the advancement of silicon performance is becoming more challenging as scaling is becoming more costly for technology solutions beyond CMOS. Integrated co-development of silicon and packaging solutions are needed to achieve new technologies with superior cost/performance metrics. Volumetric scaling also will be critical to future performance enablement and achieved by (1) tightly coupled modules and components and (2) 3D stacking and interposer integration.

Table 3-3 Key characteristics of ceramic, glass, and organic interposers for 2.5D packaging technology [18].

	Ceramic MCM	Organic MCM	Si Interposer	Glass Interposer	Organic Interposer
Dielectric Properties	Adequate	Good	Lossy	Excellent	Very good
Feature Dimensions	Mechanically defined	Down to ~10 µm L/S	Si-like lithography	Display like	Down to 5 µm L/S
CTE Induced Stress	Very good	Moderately high	Excellent	Tailorable	Moderately high
Cost	High	Moderate	Moderate	TBD	Low–moderate
Availability	Available	Available	Available	Development	Development

Fig 3-5 shows the product application for these interposers identified in another presentation [20]. The silicon interposer will dominate in the high end use; whereas in the mid-end, silicon will be key technology while organic/glass may also play a role. In the low end, organic, low cost glass or even low cost silicon if they exist will play a role. Specific production application are:

(1) Gaming, high definition television (HDTV), mobile tablets, computing, and servers,
(2) High end graphics cards will be the initial focus of high bandwidth memory (HBM) memory integration, and
(3) Mobile space has the potential to follow based on availability of low cost solutions.

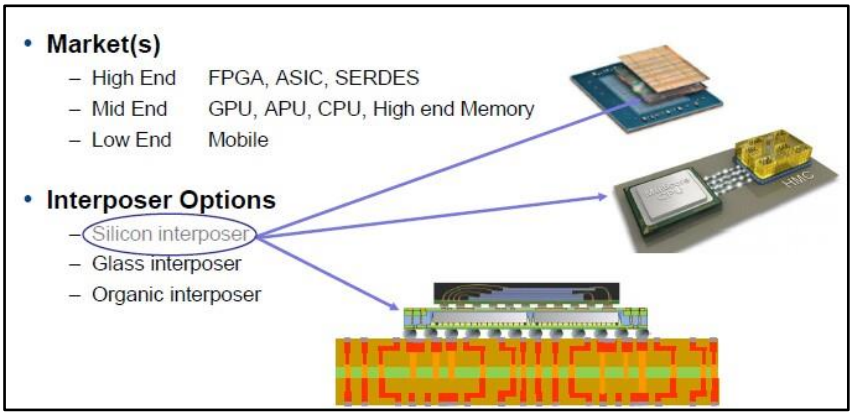


Fig. 3-5 Market for 2.5D interposer options including silicon, glass, and organic materials.

In a recent paper, C.G. Woychik et al. [21] discussed the options for 2.5D technologies with emphasis on assembling micro-bumped die (MBD) to a Si-interposer and then the interposer to an organic substrate. To achieve a high assembly yield and reliability, the key controls should be in place to minimize warpage, allow handling of extremely thin Si wafer, and to ensure integrity of micro-bump interconnects with fine pitch (typically can be < 45 µm pitch). The high density of pads and the large die size make it extremely challenging to ensure that all of the micro-bump interconnects are attached to a thin Si-interposer. The authors concluded that semiconductor fabrication facilities can produce robust and reliable devices with TSVs and that the manufacturing infrastructure exists to assemble the 2.5D packages in high volume.

J. Lau [23] summarized the impact of 3D IC integration on various industry sectors: (1) it has impacted a large number of industries including the chip suppliers, fab-less design houses, electronic manufacturing service, material and equipment suppliers, universities, and research institutes; (2) it has attracted the researchers and engineers to attend conferences, and workshops to present their findings and look for solutions of the latest technologies; and (3) it has forced industry to build standards, infrastructures, and ecosystems for 3D IC integration

J.H. Lau and C. Hsinchu [23] presented a "very low-cost interposer" using through-silicon holes (TSHs) with ability to build flip-chip die on both sides of the interposer for a 3D IC integration. The key feature of TSH interposers is that the holes are not metallized; thus, it eliminates several processing TSV steps including dielectric layer, barrier and seed layers, via filling, and Cu revealing. The TSH interposers requires formation of with either laser or deep reactive ion etching (DRIE) on a piece of silicon wafer and redistribution layers (RDL). The top-side chip is interconnected through RDLs, whereas to the bottom-side is interconnected through copper pillars and solder.

T. Mobley and S. Cardona [24] reasoned that the use of the glass interposer technology allows for a better system solution by increasing performance and improving reliability. A glass display consists of glass interposer display, low stressed drilled holes, and copper vias CTE matched to the display glass. The diameters of vias are approaching 40 µm in 300 µm thick glass wafers. The glass hole in this technology uses a funnel-like shape where the top side (entry) of the glass hole is 60 µm and the bottom (exit side) is 40 µm. The hole is then filled with copper material, thus creating a copper-based via. The

authors claim that the glass interposer technology is disruptive to the supply chain since the final via size is <50 µm and the copper is matched to the CTE of the glass, creating a true hermetic seal. The authors added that glass 2.5D and 3D packaging technologies solve hermetic problems by the integration of electronics directly into the glass.

A. Shorey et al. [25] demonstrated the ability to generate well-formed through and blind vias and fully populated test vehicles using glass interposers. Existing metallization technology was leveraged to generate very good Cu filling performance in glass in both wafer and panel formats. The electrical performance of glass generates tremendous incentive for using glass as a TGV substrate for 2.5D and 3D applications. Additionally, ability in tailoring of material properties such as CTE as well as the ability to form glass in thin large sheets of high quality enable development of cost effective processes.

Through-package vias (TPVs) and re-distribution layers (RDLs) are two key building block technologies for glass interposer. The TPV technology was presented by J. Tong et al. [26] covering detailed electrical modeling, design, and characterization using 3D glass interposers. High frequency characterization, up to 30 GHz, was presented for high aspect-ratio 55-µm diameter TPVs in 300-µm thin glass, formed by a novel focused electrical discharge method that is capable of greater than 1000 vias per second throughput. Such a glass interposer is ideal for 2.5D and 3D package integrations for high performance digital systems with high logic-memory. Glass has been proposed as a superior alternative to silicon because of its excellent electrical property and its scalability to large panel sizes leading to lower cost.

Fig. 3-6 shows another approach for 2.5D interposer is to use mixed of silicon bridges in a laminate rather than a more expensive silicon interposer [27]. This interposer packaging technology, embedded multi-die interconnect bridge (EMIB), enable very high-density die-to-die connections only where needed; hence, a lower cost and simpler 2.5D packaging approach. Standard flip-chip assembly within package is used for robust power delivery and to connect high speed signal directly from chip to the package substrate. EMIB is available for 14nm foundry use.

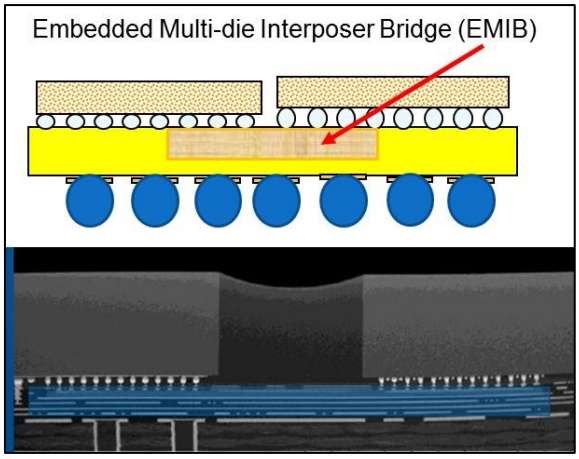


Fig. 3-6 A low-cost 2.5D laminate with silicon embedded bridge for effective flip-chip routing [27]

3.3.2. 3D (Active TSV Interposer) Packaging Trends

This category of packages with TSV stack die is often called "3D integration" in order to distinguish them from 3D packaging. Stacked memory die is a perfect choice for using TSV technology as all interconnections of each die align with the corresponding die located above and below. However, this is merely a building block for future designs as mobile terminals to supercomputers, which require maximum computing power using limited resources such as power consumption and volume for the next-generation of information processing devices. A 3D-integrated logic device with stacked memory matches this objective because the shortest and highly parallel connection between logic and high-capacity memory reduces the power consumption due to long-distance and high-frequency signal transmission, and realizes the highest device density.

Therefore, 3D TSVs refer to a stack package that contains two or more chips (integrated circuits) stacked vertically so that they occupy less space on a printed circuit board (PCB) (usually the same footprint as the bottom chip). TSVs replace edge wiring by creating vertical connections through the body of the chips. The resulting package has no added length or width. Because no interposer is required, a TSV 3D package can also be flatter than an edge-wired 3D or 2.5D package. Not all TSVs are the same. There are many variations of this technology.

The key on use of TSV technology is to address when it is advantageous to go vertical and when it is not. Stacking two wafers and integration with vertical vias is costly. This cost must be justified through performance gains, functional gains, or cost savings elsewhere in the system. The market for TSVs will be established when the benefits justify the cost. There is a growing consensus that several mainstream circumstances exist that justify the 3D integration.

Use of TSV 3D integration is rarely justified for form-factor miniaturization alone since in most circumstances, it is much more cost-effective to meet the form-factor needs by stack and wire-bond, or otherwise vertically integrate, at the package level. However, when identical memories are considered, use of TSV technology is advantageous since edge wire-bonding cannot easily be used. In addition, there are system advantages to thinning and stacking multiple memory die such that the aggregate memory has the same end form factor as one memory package.

The most explored advantage of 3D is its reduction of the interconnect distances between chip functions. Many researchers justify 3D from interconnect delay and interconnect power perspectives. From a theoretical viewpoint, the advantages can be substantial. Several studies have presented a Rent's Rule style of analysis supporting this premise [28, 29]. The basic argument relies on the fact that with each additional layer of transistors, there is a similar increase in the number of circuit functions that can be interconnected within a fixed wire length. This leads to a 25 percent or greater decrease in worst-case wire length [30], a similar decrease in interconnect power [31], and a modest decrease in chip area. However, experience shows that many designs do not realize the large theoretical advantages in practice. Fortunately, with careful choice, appropriate design applications can be found. For example, field programmable gate arrays (FPGAs) are very interconnect-bound and can achieve substantial performance and power improvements when recast in 3D [32].

J. Vardaman [33] and P.E. Garrou et al. [34] stating that stacking memory die to create a new "super-memory" chip is not the only 3D application involving memory. An interesting area of application is targeting logic-on-memory, which creates a high-bandwidth memory

interface to the logic. For many end applications, the demand for memory bandwidth is growing rapidly. In many cases, this is due to the increased use of multi-core processors. With the addition of each processor comes a similar requirement for increasing memory bandwidth. Similar bandwidths will be beneficial in other applications, including digital signal processing, graphics processing, and networking. This, by itself, gives a fairly natural case for 3D, one that has been only lightly explored, and then mainly in the context of general-purpose computer micro-architecture. For example, 3D caches can lead to 10 to 50 percent reductions in cache latency, depending on the benchmark used.

Table 3-2 lists strengths and weaknesses of various 3D technological approaches discussed in details in this section. The table also includes embedded die and use of newly implemented fan-out wafer level package for stacking build up. Regarding the 3D-TSV (3DIC), while the drivers for their applications remain constant, the time line for its adoption continues to shift due to technical challenges, infrastructure issues, and cost. Progress has been made in via formation and filling, but process steps such as debonding during wafer thinning still remain problematic. Progress has been made in design tools and methodology, but low-power design of 3DIC stacks remains in the early stages. Test, inspection, and reliability are yet to be fully implemented. Improvements in process yield and thermal solutions that lower cost are necessary. Key remaining technology gaps in 3D IC readiness are summarized in the following [35].

- Availability of commercial 3D electronic design automation (EDA) tools
- Micro bumping and assembly for stacked die
- Assembly of die on interposers
- The debond step in temporary bond/debond
- Thermal design and dissipation when logic is part of the stack
- Test methodology and solution
- Reliability data including drop test data
- Yield improvements that lower cost
- Infrastructure related issues such as hand-off point

Table 3-2 Key strengths and weakness of 3D packaging technologies.

3D Pkg Tech	Strengths	Weaknesses
Stack Wire bonded Die	• Low cost • Wide availability	• I/O density • KGD
Pop/PiP	• Separate testing • Existing package technology	• Height • Pkg design constraints
FOWLP as PoP	• Thin Package • Performance	• Limited infrastructure • Assembly yield
3D-TSV (3DIC)	• Performance • Density	• Cost • KGD/Test
Silicon Interposer	• Density • Die yield improvement	• Cost • Thermal
Embedded Die	• Low cost	• Yield

4. EMBEDDED COMPONENT TECHNOLOGIES

Passives usually refers to resistors, capacitors, and inductors; but it can also include thermistors, varistors, transformers, temperature sensors, and almost any non-switching analog device. The discrete passive component is a single passive element in its own leaded or surface mount technology (SMT) package. An on-chip passive is a passive element that is fabricated along with the active elements as part of the semiconductor wafer (die) where an on-package version uses passives on the package substrate using SMT.

For example, decoupling capacitors can be placed on either the top or bottom of the package. Each of these locations has its associated advantages and disadvantages. Top side decoupling capacitors (see Fig 4-1) have the advantage of efficient space utilization, but overall system equivalent series inductance (ESL) can be compromised because of the larger distance between the capacitors and the power and ground pins of the microprocessor. On the other hand, path length is decreased for bottom-side decoupling, but valuable real estate that could be used for I/Os is taken up.

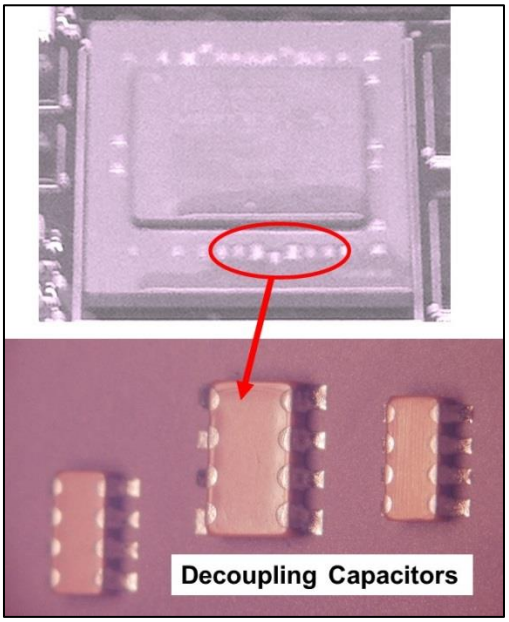


Fig. 4-1 Flip-chip column grid array (CGA) with exposed decoupling capacitors.

The concept of embedded, integrated, integral, arrayed, or networked passives involves manufacturing them as a group in or on a common substrate instead of discrete packages. In general, embedded components are defined as passive or an active device that is placed or formed on an inner layer of an organic circuit board, module or chip package such that it is buried inside the completed structure, rather than on top or bottom surface. The drivers are similar to SiP. Primary market segments using embedded components today include defense/aerospace, network infrastructure, and mobile communications. The key advantages are:

- Reduced product cost
- Added features
- Reduced size
- Improved performance
- Accelerated time to market

ITRS defines two types of passive/active devices for embedded applications. Embedded passive devices in PCB are categorized into either chip devices or formed devices. Also, there are two types of active devices: (1) wafer level package and (2) flip-chip die. The wafer level uses die with no copper post to enhance mechanical strength whereas the flip-chip uses die with stud bump or copper posts which are embedded in an organic laminates substrate. Fig 4-2 illustrates embedded packaging/PCB technology trends.

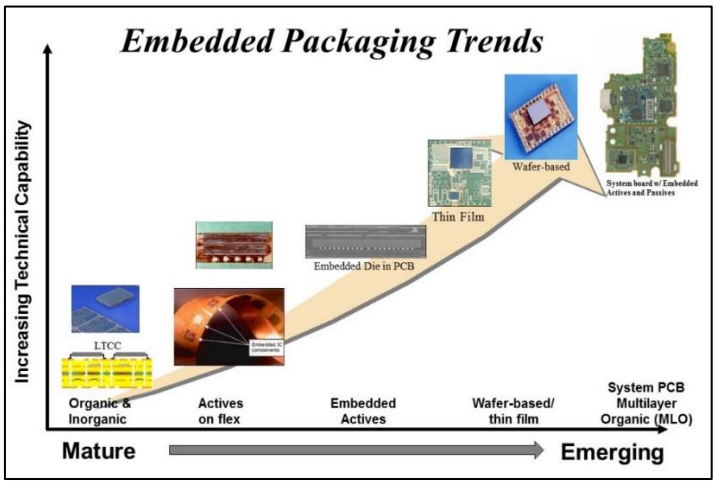


Fig. 4-2 Embedded passive and active in printed circuit board and package.

4.1. Embedded Passives

Embedded-passive technology plays a crucial role in the packaging platform because the passive components often occupy more than 80% of the real estate in the board, while the assembly cost accounts for around 70% of a product assembly cost. The embedded-passive technology makes an overall board size smaller, leading to the higher throughput. It also helps improve the electrical performance because it eliminates soldering, which in turn improves system reliability while achieving a cost reduction and a fast time to market by removing surface-mounted devices (SMDs). Such advantages as lower cost, compactness, reliability, and higher performance make the embedded passive technology a suitable package solution for the systems as well as a key technology for the higher integration.

Substrates for embedded passives are either organic PCB, ceramic (HTCC or LTCC) or thin film on ceramic or glass. LTCC (Low Temperature Co-fired Ceramic) is manufactured in a green ceramic state and then fired to produce a homogenous substrate. The techniques employed are widely available in the literature. Once fired, the substrate variates from the green state dimension introducing variability in the design. Being a 3D structure a planar EM field solver must be utilized for simulation. Coupling between structures cannot be

solved exactly with today's software capabilities, leading to an iterative design approach. Iterations numbering 3-5 to complete a design are not uncommon leading to a fairly lengthy and inflexible design cycle in a world where speed is essential to get products to the market.

Today's LTCC systems utilize a number of base materials, some openly available such as Dupont's LTCC and others proprietary. Establishing qualified, reliable, standardized processes, key to cost effectivity, is difficult with these variables introduced. In addition, panel sizes are variable among vendors. Laminates have reduced in cost with the ability to standardize on materials and equipment and maintain HVM equipment compatibility. With the variation in panel sizes, standardizing the equipment set has meant setting the LTCC substrates to standard sizes. This can result in poor panel efficiency from the LTCC substrates. Of course, dedicated optimized lines for ceramic processing are likely to reduce the costs associated with this aspect.

Ceramics can either be sawn or snapped. Obviously snapped solutions should be the most cost effective eliminating sawing and minimizing saw streets. However, processes used for ceramics often have the impact of singulation before it is time, resulting in yield loss. Sawing requires additional time in process and requires more frequent blade changeover than laminates.

4.2. Integrated Passive Devices (IPD)

Integrated passive devices (IPDs) are subcomponents that exclusively contain passive components. The IPDs play a crucial role in the packaging technology because the passive components often occupy more than 80% of the real estate in the board, while the assembly cost accounts for around 70% of a product assembly cost. The embedded-passive technology makes an overall board size smaller, leading to the higher throughput. It also helps improve the electrical performance because it eliminates soldering, which in turn improves system reliability while achieving a cost reduction and a faster time to market by removing surface-mounted devices (SMDs). Advantages such as lower cost, compactness, reliability, and higher performance make the IPD technology a suitable package solution for the systems as well as a key technology for the higher integration.

The IPD may contain all three types of passives (R, L and C, resistor, inductor, and capacitor, respectively in any combination. The elements can be connected to each other in order to form a certain network, matching or filter functions, or stand-alone elements to serve their function. The introduction of new materials like thin oxides or filled polymers as dielectrics as well (as the introduction of deep silicon vias) is extending the value range of capacitors into the microfarad realm. Besides standard redistribution wiring systems, it is also possible to form ground planes and transmission lines to create impedance-controlled RF-signal transmission.

IPD packaging can be categorized as either stand-alone chip scale package IPD devices or integrated IPD modules. Chip-scale IPD packages contain the entire IPD network in a single system in package (SiP) structure. This single package is designed to replace a surface mount passive component network. It is common to see these single packaged networks in ball grid arrays (BGAs), quad flat no leads (QFNs), and flip-chip packages. The area array packages help take full advantage of the size reduction achieved by using IPD technology.

Reference [36] presents an example of a wafer-level chip scale module package (WLCSMP). This category of module package is the advanced modular architecture that integrates mixed IC technologies with a wide variety of passive devices such as resistors, capacitors, inductors, filters, baluns, transceivers, receivers, and interconnects directly onto a

silicon substrate. The result is a set of high performance system level solutions that provide a significant reduction in die size and weight.

In order to reduce the board surface area and system cost associated with passive components, recent movements in the industry are focusing on alternative mounting methods. Alternative mounting include on-chip, multiple value discrete passive components (arrays) mounted onto boards or substrates, passives fabricated within the board (embedded), and combinations of all of the above. One emerging method is the array or network approach known as "integrated passive devices" or IPDs. Integrated passives are simply collections of passive devices made using semiconductor of thin-film methods, packaged as an integrated circuit (IC).

V. Solberg [37] presented the key advances and hurdles in implementation of passive and active technologies. The key findings are listed in the following.

- Embedded circuits are being produced successfully in very high volume worldwide.
- Embedding the semiconductor is where many companies may find a significant roadblock
  - Procurement of semiconductors in a wafer format
  - Outsourcing metallization and thinning
  - Confidence in semiconductor quality (KGD)
  - Sequential electrical testing during PCB Fab.
  - Testing embedded mixed function assemblies
- The PCB fabricator will be expected to perform board-level functional electrical testing.
- When outsourcing embedded component PC boards, the originating company will likely bring together the two primary disciplines; the circuit board fabrication specialist and the assembly service provider.
  - These partnerships must be willing to adjust their portion of the generated revenue against the overall process yield (includes the sharing of losses from fabrication process defects and damaged components).

4.3. Embedded Active

Recently, in addition to embedding passive components, attempts are being made to embed active chips. For the embedded active structure, thinned active chips are directly buried into a core or high-density interconnect layers rather than placed onto the surface. Currently, active chips can be embedded in many different ways within the categories of chip-first, chip-middle, and chip-last. Embedding is expected to reduce the parasitic effects of interconnects (reduced interconnect length) resulting in lower power dissipation, and providing better electromagnetic shielding. They also offer smaller and thinner package profiles.

In general, the chip-first technology has a number of challenges:

- The chip, once it is embedded, is subjected to a number of processing steps and can be affected due to the fabrication.
- Serial chip-to-build-up processes accumulate yield losses associated with each process.
- Defective chips cannot be easily reworked in current embedded package structure. Thus, this technology needs 100% known good die (KGDs).
- The interconnections in the chip-first approach, which are direct metallurgical contacts, can encounter fatigue failures due to thermal stress.
- Thermal management issues are also evident since the chip is totally embedded within polymer materials during the substrate or build-up layer processes.

L. Del Castillo, et al. [38] presented their evaluation on ultra-thin flexible microelectronics for use in applications such as conformal and wearable electronics by embedding less than 50-µm silicon die. As shown in Fig. 4-3, three techniques have been developed to fabricate ultra-thin, flexible electronics: (1) thinned die flip-chip bonded on polyimide or liquid crystal polymer (LCP) flex, (2) thinned die laminated into LCP films, and (3) thinned silicon die embedded in polyimide. The manufacturing methods and materials for each of these approaches is described in the following sections.

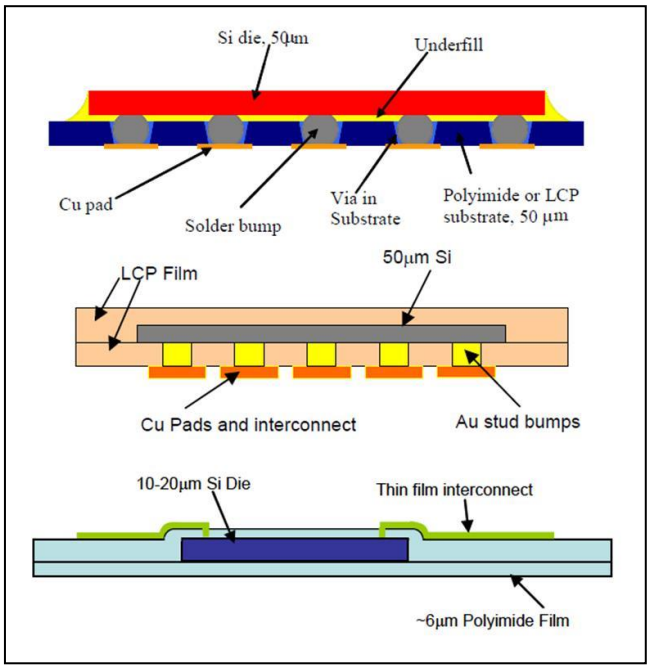


Fig. 4-3 Three techniques of thinning die: polyimide and LCP substrate with solder assembly (top); LCP substrate with thermal compression bond Au stud bump assembly (middle); thinned Si die embedded in polyimide with thin film interconnect (bottom) [38].

H. Hayashi et al. [39] disclosed a new embedded package configuration, wide strip fan-out package (WFOP), it is a face-down mounting (See Fig. 4-4), which uses a metal plate (stainless steel or copper) as the base plate of the redistributed interconnection layer. The dies are mounted on the metal plate, and the resin between the dies acts as a stress buffer and insulator for the interconnections. The advantages are a lower package warpage, precise fabrication process control, lower thermal resistance, and shielding of noises. The author showed reliability test results and multiple die stacking configuration for use in memory devices.

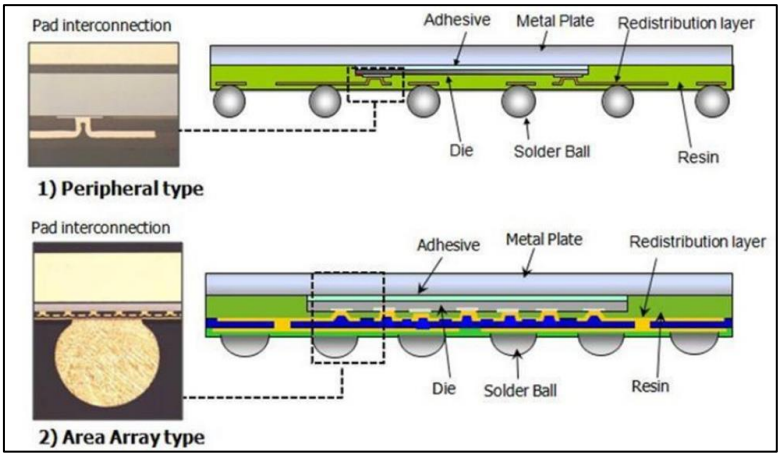


Fig. 4-4 A new embedded package, wide strip fan-out package (WFOP), which uses a metal plate like.

PCB based embedding technologies combine the advantages of standard printed circuit manufacturing with additional highly precise component assembly. Generally, two different approaches of component assembly are used: Face up, where the assembly of the semiconductor die is down with its contact pads up, comparable to a die for wire-bonding, or face down where the die is assembled with its contact pads down, like a flip chip. The face-up technology enables electrical and thermal contact using both conductive and non-conductive adhesives, solder, and low temperature sinter materials for the die-attachment. Because of its heat dissipation, this approach is widely used for various embedded active die including power metal oxide field effect transistors (power-MOSFETs), insulated gate bipolar (IGBTs), and diodes. Since the face-down technology is comparable to the conventional wire-bonding, it is already in high volume application. The process starts with embedding the die with placement of resin-coated copper (RCC) or prepreg with conductive adhesive and vacuum lamination followed with a microvia build for electrical connection to the embedded chip. Such substrates with embedded dies can be further processed like standard PCB inner layers. Fig 4-5 shows an example of a face down embedded component technology, a DC-DC converter. This package has one embedded die with three SMD components assembled on top of the PCB [40, 41].

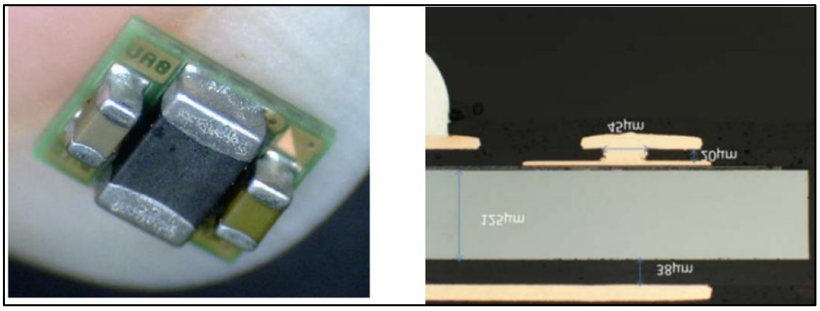


Fig. 4-5 Configuration of wafer level chip scale module package (WLCSMP).

J. Vardaman and K. Carpenter [42] presented the status of embedded devices and applications. It was stated that the key driver for the embedded active is demand for more thinness requirement, but the secondary advantages are for improved robustness and security. For embedded passive, the key driver is requirement for higher operating frequencies enabled by placing decoupling capacitance close to the processor. The technology requirements for embedded actives are thin-film, laminated or build-up with the first applications are for ultra-thin PoP for mobile products. The technology for embedded passive is primarily capacitors in build-up or laminate substrate. Application processors with embedded capacitors in high volume manufacturing (HVM) for mobile phone with future applications in high-end networking and communications.

5. Other Packaging Trends and Hierarchy and Materials

5.1. Moveable (MEMS) and Exposed (MOEM) Packaging

Microelectromechanical system (MEMS) are integrated micro devices or systems combining electrical, mechanical, fluidic, optical (MOEM), (and all physical domains) components fabricated using integrated circuit (IC) compatible batch-processing techniques and range in size from micrometers to millimeters. In the United States, the technology is known as MEMS, in Europe as microsystems technology (MST), and in Japan as Micromachines.

MEMS and Optical MEMS requires microfabrication of a silicon wafer. Silicon has been used as a mechanical substrate for more than 25 years. Two commonly used silicon microfabrication techniques exist: surface micromachining and bulk machining (see Fig. 5-1) [43-45].

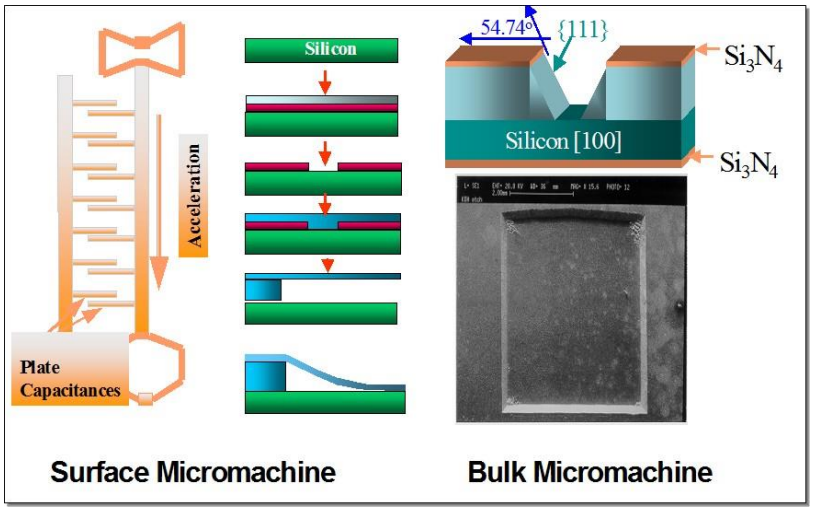


Fig. 5-1 Surface and bulk micromachining fabrication and structure

MEMS devices include microscopic machines such as valves, pumps, switches, and actuators. MEMS are unique in that they perform both mechanical and electrical functions,

and physically move. MEMS both harvest data and issue commands based on the data. A MEMS with a miniature tuning fork, for instance, can gather information about the direction of sound waves, which can prompt a command to shift the position of a microphone for better sound quality. Current technology mainly addresses millimeter (mm) to micrometer (μm) level MEMS devices.

MEMS are built similar to integrated circuits. They are fabricated on silicon wafers by patterning various layers of materials and releasing (under-etching). After release, these tiny structures are capable of motion. If the microstructure is a mirror, and the device can move and manage light, the device can be considered an optical MEMS, also known as a MOEMS.

Some of the MEMS technology has been around for years. Computer printer heads, automotive air bag actuators, brake sensors and engine heat sensors are examples of MEMS devices found today. Analog Devices' ADXL line of air-bag accelerometers and Texas Instruments' Digital Micromirror Device (DMD) display technology are commercial success stories. MEMS devices have traditionally been used to gather ambient data like temperature or pressure, but are expanding into more complex uses that involve optoelectronics and biotechnology. For example, MEMS devices can be used in new drug testing in the pharmaceutical industry, or in blood-screening sensors that can perform complete tests at bedside.

However, in recent years, need for MEMS/MOEMS packaging is further driven by consumer products including gaming and smartphone. Consumer products are price-sensitive and the market also needs quick turnaround times, smaller foot prints, and packages with a high degree of reusability and package standardization. Previous MEMS applications were custom made and application specific and generally tailored for high-reliability such as automotive industry. Transition from the automotive to the consumer market poses additional cost challenges and standardization challenges, especially the latest push for sensor fusion and internet of things (IoT).

This situation posed a challenge in transitioning. Furthermore, the automotive market was not price sensitive at that point, but long-term reliability was key. He added that the latest push is for sensor fusion and IoT applications, so there is an even greater need for lower costs and standardization.

In the IC industry, electronic packaging must provide reliable, dense interconnections to the multitude of high-frequency electrical signals. In contrast, MEMS packaging must account for a far more complex and diverse set of parameters. It must first protect the micromachined parts in broad ranging environments; it must also provide interconnects to electrical signals, and in some cases, access to and interaction with the external environment. Examples are as follows:

- The packaging of a pressure sensor must ensure that the sensing device is in intimate contact with the pressurized medium, yet protected from exposure to any harmful substances in this medium.
- Packaging of valves must provide access for electrical signals and fluid interconnects.

The MEMS packaging is largely borrowed from the IC industry in an effort to benefit from the existing mature technology. Designing packages, e.g. a micromachined sensor package, involves taking into account a number of important factors. Some of these are shared with the packaging of electronic ICs, but many are specific to the MEMS applications. Due to the variety of MEMS devices, it is not possible to specify a generic package. It is, however, possible to make some general comments. The package must be

designed to reduce internal/external electrical (or electromagnetic) interference, dissipate heat in the device, withstand high operating temperature and minimize CTE.

The package should also be designed to minimize stress on the device due to external loading, and it should be rugged enough to withstand the environment in which the device will be used. Connections to the package must also be capable of delivering the power required by the device. Connections out of the package must have minimal sources of signal disruption (e.g. stray capacitance). The package also has to have the appropriate fluid feed tubes /optical fibers, etc., attached to it, and aligned /attached to the device inside. Three categories of widely adopted packaging approaches in MEMS are: ceramic, plastic, and metal, each with its own merits and limitations are discussed below. Standard packages are

Metallic Packages: Metallic packages are attractive for MEMS because they are robust and easy to assemble, but they are being replaced by plastic or ceramic packages. Metal packages satisfy the low pin-count (input/output, I/O) requirements of most MEMS applications; they can be prototyped in small volumes with rather short turnaround periods and they are hermetic when sealed. For example, metal packaging is used for fluidic isolated pressure sensors that are intended for operating in industrial environments. The silicon sensor is immersed into an oil filled stainless-steel cavity that is sealed with a thin stainless diaphragm. The sensor measures pressure transmitted via the steel diaphragm and through the oil. The robust steel package offers hermetic protection of the sensing die and the wire-bonds against adverse environmental conditions.

Ceramic Packages: Ceramics are hard and brittle materials with high elastic moduli. A ceramic package often consists of a base or a header onto which one or many dice are attached by adhesives or solder. Wire-bonding is suitable for electrical interconnects. Flip-chip bonding to a pattern of metal contacts on the ceramic package works equally well. The final step after mounting the die on the base and providing suitable electrical interconnects involves capping and sealing the assembly with a lid, the shape and properties of which are determined by the final application.

Plastic Packages: Plastic packages, unlike their ceramic or metal counterparts, are not hermetic. Two approaches to fabrication plastic packages include post-molding and pre-molding. The plastic post-molded housing is molded after the die is attached to a lead frame. The process subjects the die and the wire-bonds to the harsh molding environments. In pre-molding, the die is attached to a lead frame over which plastic was previously molded.

However; the most popular standard package styles today includes SOIC and laminate LGA/FPBGA. The QFN and laminate LGA/FPBGA packages also could become standard platforms for sensor fusion and IoT applications and meet cost vs. performance objectives in the mobile industry. Though sensor fusion and IoT applications are primarily aimed at the consumer market, these package also have the potential to transition to the automotive market, which will benefit by having these standard platforms. Also, MEMS and other sensors in SiP packaging using FOWLP technologies is another methods for further reducing cost and form factor.

5.2. Optoelectronics Packaging

Fig. 5-2 shows the packaging and connectors trends for optoelectronics. Optical interconnects have been developed as the next generation packaging approach since the design of intra-chips interconnection has reached its capacity in GHz design. Engineers have been struggling to incrementally improve the interconnect density through the

optimization of silicon processes and materials. Even if the ultra-fine scale chip level interconnect is capable to meet Tera-Hz processing power, the designers will have to overcome the challenges in interconnect density required for the fan-out to system level. Industry has continued to build on the development of fiber optics, which has proved to be a reliable and high performance carrier as a long distance network. The idea of having optics as chip-to-chip interconnection is currently practicing, and is not far from the foreseeable future. Optical waveguides will form the basis for next generation high performance and high speed optoelectronics and micro opto-electromechanical system (MOEMS). There are four types of multimode waveguide designs available in the industry, namely,

- Free space optical interconnect
- Buried waveguide inside the printed circuit board (PCB)
- Optical layer on top of PCB
- Flex-foil based optical interconnects

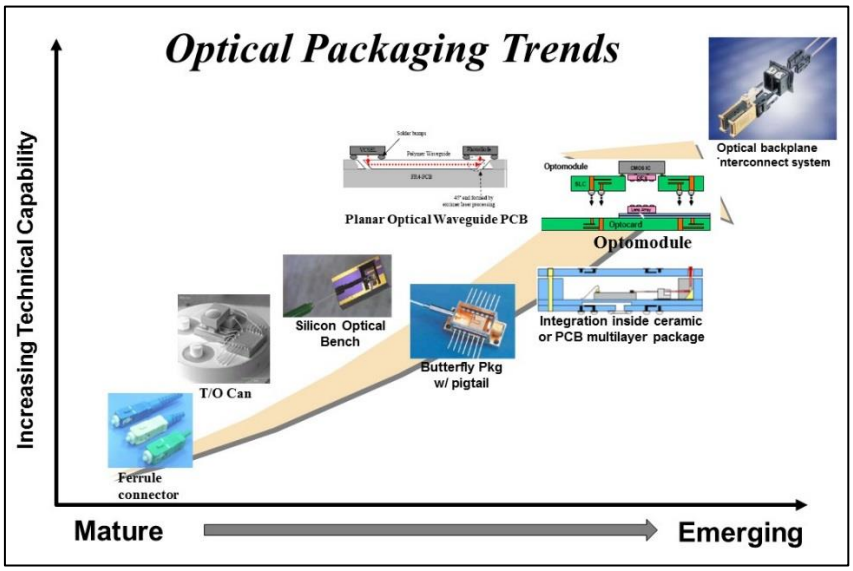


Fig. 5-2 Optical packaging trends from conventional to advanced packaging technologies.

5.2.1. Packages for Single Optical Components

Single optical components (lasers, photo diodes) are mainly used for simple electro-optical as well as opto-electrical conversion. Package types depend on device functionality and application standard. Interfaces are generally by pigtail, optical connector or free-space optical transmission. Examples are:

- TO-Package with pigtail or connector
- Butterfly-package with pigtail or connector
- Plastic-DIL (dual in line) with connector or free air interface
- SMD-Packages with connector or free air interface
- Specific metal packages (tray, lead frame) with pigtail
- MOEM new advanced packaging including LGA, PBGA, WLP, and QFN

Package type, pin number, size, assembly technology, etc. are determined by functionality, motherboard structure and cost. There is no difference between application for transmitter or receiver. The most popular and expensive package for high-reliability application is the TO-type. Metal cap with optical window, a metal can and assembly, mainly by soldering or welding, make the system hermetic, highly thermally conductive, electromagnetically protected and independent from environmental influences. The TO-can package can integrate lenses, filters, fiber retainers, etc., but their uses are limited for applications up to 10 Gbit/s (transmitter).

Increasing frequency and functionality make it necessary to introduce larger SMD packages. In this case, more space is available for components like Peltier elements and temperature control units for transmitters (Tx) or TIAs and shields for receivers (Rx). Systems are generally assembled on a lead frame structure and later over-molded with epoxy. This makes the technology more flexible and cost effective for mass production. In the future, SMD solutions will come to the fore. As discussed in MEMS?MOEM section, other more dense package technologies become available in order to accommodate consumer needs for lower cost and mass production.

In summary, feature requirements and integration for energy and band-width efficient photonic packaging, active and passive, are different from IC packaging. For example, hybrid integrated silicon photonic components require ultra-fine flip-chip interconnects for energy efficiency, single-mode optical interfaces (waveguide-to-waveguide or waveguide-to-fiber) require sub-micron alignment and placement accuracy, and PCBs may require embedded optical waveguides and couplers to facilitate optical ICs. It means that the photonics-based communication highways needs to be effectively integrated with their electronic systems requiring development of common photonics/electronics packaging interfaces.

5.2.2. 3D Packages for CMOS Imaging Sensors (CIS)

Packaging technology for CMOS imaging sensors (CIS) sensors used in most type digital cameras now advance to using 3D stack, stacking optical on processor. The CMOS sensors replaced CCD technology, the first imaging sensor for consumer digital cameras. The integration of chip technologies, micro optical components and packaging for building up a real system in a package (SIP) (for optoelectronic application) needs developments in many areas in order to achieve higher image quality for the CCD sensors. The main difference between CMOS and CCD sensors is that in a CMOS sensor, the charges are not passed along a column of pixels, but rather each pixel has its own readout unit. On top of this, unlike CCDs that output an analog signal that has to be converted to digital before the camera's image processor can interpret it, a CMOS sensor outputs a digital signal directly. CMOS sensors also have lower power consumption than CCDs, which makes them especially suited for video recording and cameras with live-view functions.

Another sensor was introduce in 2012, called back-side illuminated (BSI) CMOS sensor [46]. The main difference between the normal CMOS sensor and the BSI-CMOS sensor is that the former has its circuitry on top of the photosensitive layer, which means that the incoming light is partially blocked before it hits the pixels. BSI-CMOS sensors, which are used in many smart phone and compact cameras today, have the circuitry behind the photosensitive layer. Since their layout is technically inverted, it is as if a regular CMOS sensor were illuminated from behind–hence the designation 'back-side illuminated'.

This technology now advanced to 3D stack, stacking optical on processor. The color pixels require fewer metal interconnect layers and high voltage, lower temperatures

during processing and longer anneal times whereas the logic portions of the circuit are quite the opposite needing many more layers of interconnect and low voltage, higher processing temps and shorter anneal times. It therefore makes sense to fabricate these layers separately and stack them. Addition of memory to the stack is the next step in the development.

5.3. RF, Multi Packaging

Fig. 5-3 depicts radio frequency (RF) packaging technology trends. The need for analog/mixed-signal and RF content arises that usually is difficult to integrate. System on Chips (SoC) and System-in-Package (SIP) are key enabling technologies for digital and RF micro miniaturization and system integrations on silicon, ceramic and organic substrate platforms, offering diverse functionality in a single module. Embedded chip technology is being accepted for miniaturization of RF, base band and other mixed signal modules.

The size reduction of RF modules can be achieved by using embedded-passive technology. In addition, multi-layer substrates with high density interconnects are also critical in meeting size targets. Accordingly, the need for an extended supply of high-frequency packaging materials with high performance has become critical. Teflon and ceramic-based materials have been commonly used as high-frequency applications for many years

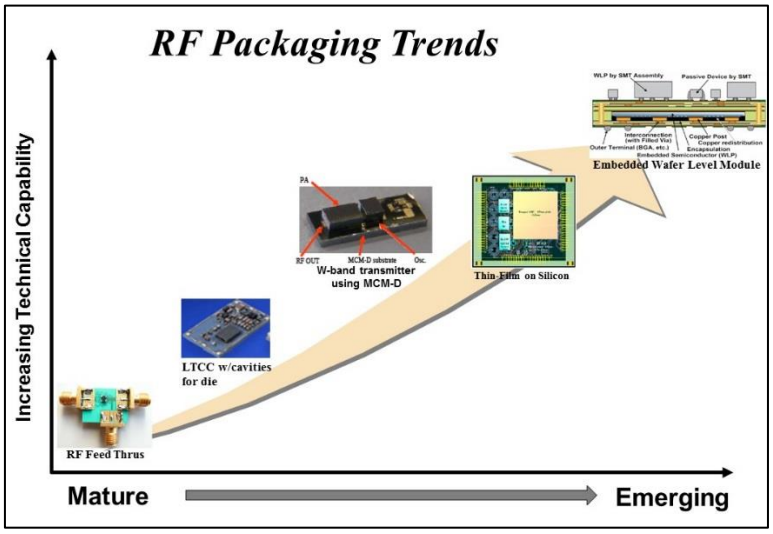


Fig. 5-3 RF packaging technology trends

As an example, for RF circuits the low temperature co-fired ceramic (LTCC) solution may provide the smallest size and also good cost effectivity. For the designer the ability to implement passives, layered shielding and transmission line structures in a high ε_r dielectric along with its die interconnectivity and routing capability makes LTCC an attractive solution set. Passives can be made with tolerances in the 3-5% range, multiple layers (14-20 are common) are available and the substrate is rugged when properly sized to the motherboard.

Variation in LTCC introduces potential variation in the electrical performance of RF circuits and may result in substrate binning, sub-lot testing, component matching and solder paste screen matching. The manufacturing and inventory logistics of such a solution may severely impact the cost of the solution. The two most costly manufacturing processes for ceramic are die protection and singulation. Die protection for ceramics is typically accomplished with a silicone glob-top followed by the application of a ceramic, plastic or metal cap to provide a handling and marking surface. The metal cap is usually soldered. Metal covers have the ability to provide shielding in a larger scale integration such as the transmit chain for a cellular phone.

Warpage of the substrate can occur making singulation difficult. An alternative solution to this approach is to leverage over molding utilized in laminates to ceramics. In this case the ceramic is overmolded beyond the edges of the substrate panel providing the die protection and utilizing a very cost effective array solution. If shielding is required this can be captured in the overmold. LTCC processing will evolve and design tools will progress such that this medium will gain more acceptance in RF SiP solutions for high levels of integration.

5.4. Hybrid/Multi-chip Packaging

Conventional leaded packages generally have larger footprints than the chips, as much as 4 to 10 times larger and are much thicker, 4x or more, than the die within. Conventional packaged parts not only make it difficult to meet the smaller footprints, but have high package parasitics and can be susceptible to EMI/EMS concerns. Multi-chip and hybrid technology can handle these requirements as they tend to be a system packaging solution rather that one or two different chips, such as most 3D packaging. Fig. 5-4 presents the multi-chip packaging technology trends.

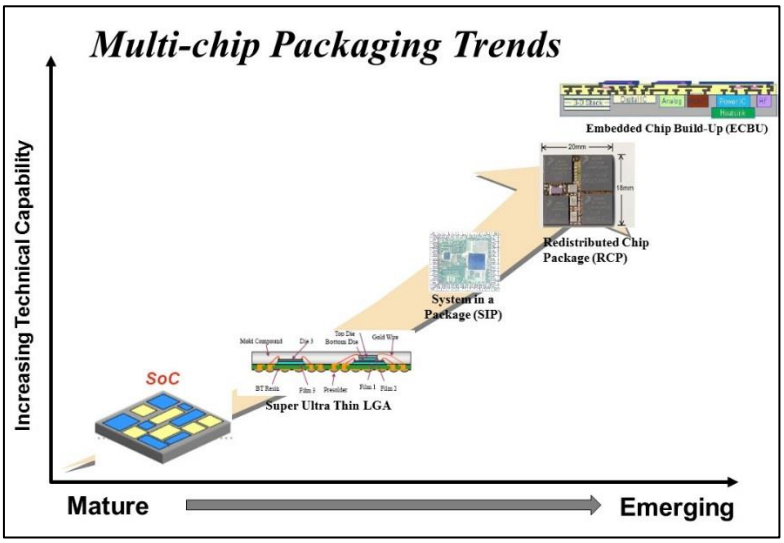


Fig. 5-4 Multi-chip packaging trends

For high-reliability application, hybrid DC/DC converters are power supplies that are fabricated with bare die as compared to using packaged parts. Elimination of the intermediate packages allows the size of the DC/DC Converter to be dramatically reduced. All parts are mounted on ceramic substrates which are well attached to the baseplate of the package. The DC-DC power converter hybrid is one of the most difficult hybrids to build as it consists not only of discrete resisters and capacitors and microcircuits, but also has larger components such as magnetics and inductors. The combination of these small and large components makes this technology very challenging to manufacture consistently.

5.5. Packaging Materials

Fig. 5-5 shows materials technology considered for conventional and advanced packaging technologies. New materials have been developed and are included in most roadmaps. Changes from Sn/Pb solder to no lead alloys to Cu pillars are being used in flip-chip (FC) technology. Whether it is flip-chip in package (FCIP) or flip-chip directly on a board (FCOB). As discussed earlier, wafer fabs are using new chip-level dielectric materials. One of these materials is Low-k dielectric. Assembly challenges for Low-k devices are primarily mechanical due to the weak dielectric material. Potential problems include cracked diffusion barriers, copper diffusion into low-k polymers and cracking of the low-k material. Low-k polymers tend to have high TCE and low thermal conductivity. These new materials force the choice of appropriate underfill materials to accommodate these stresses.

There has been increasing interest in the development of electronic circuits on flexible substrates to meet the growing demand for low-cost, large-area, flexible and lightweight devices, such as roll-up displays, e-papers, connectors, and keyboards. Organic materials have attracted a lot of attention for building large-area, mechanically-flexible electronic devices. These materials are widely pursued since they offer numerous advantages in terms of ease of processing, good compatibility with a variety of substrates, and great opportunity for structural modifications.

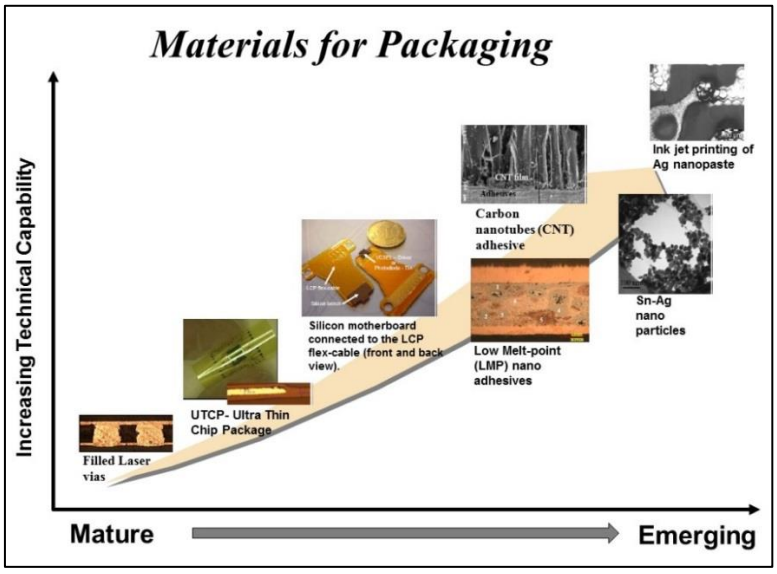


Fig. 5-5 Materials for packaging technologies

5.6. Packaging Interconnections and Hierarchy

For surface mount technology (SMT), packaging hierarchy defines different manufacturing and system levels. Definition of electronics elements and system level (e.g., defining interconnects between system levels) allows value chain participants to capture value and enable innovation. Furthermore, the acceptance of definitions allows value chain members to develop materials and technologies optimized for use within specific system levels. For example, the JISSO international council (JIC), a mix of membership from Asian, European, and North American members, was formed with the aim of promoting a strategic partnership among organizations interested in the total solution for electronics interconnecting, assembling, packaging, mounting, and integrating system design. Fig. 5-6 shows a recent proposal by JISSO with an added expansion on definition of packaging hierarchy [47, 48].

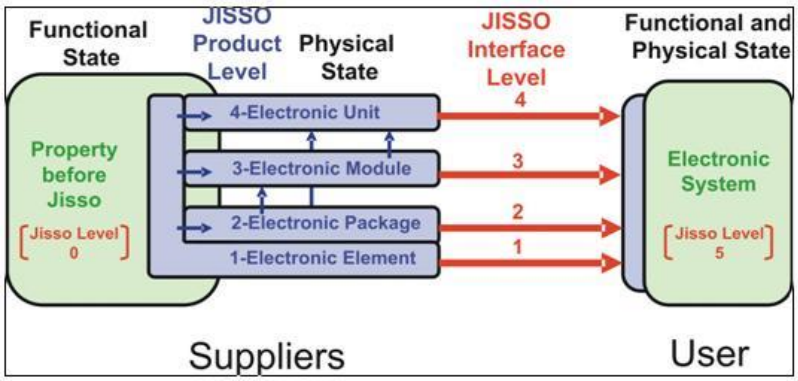


Fig. 5-6 SMT packaging hierarchy presented by JISSO.

The definition of interconnection hierarchy includes the following levels [47, 48].

Level 0 – Electronic Intellectual Element: The intellectual property of an item pertains to the idea or intelligence imported or described in a formal document (protocol, standards and/or specifications), design entity, or patent disclosure. The information may be in hard or soft copy and can include computer code or data format as a part of the descriptive analysis. The characteristics are described as to their physical, chemical, electrical, mechanical, electromechanical, environmental, and/or hazardous properties.

Level 1 –Electronic Element: Uncased bare die or discrete components (e.g., resistor, capacitor, diode, transistor, inductor, or fuse), with metallization or termination ready for mounting. This can be an IC or a discrete electrical, optical, or MEMS element. Individual elements cannot be further reduced without destroying their stated function.

Level 2 – Electronic Package: A container for an individual electronic element or elements that protects the contents and provides terminals for making connections to the rest of the circuit. The package outline is generally standardized or meets guideline standards. The package may function as electronic, optoelectronic, MEMS, or system in package (SiP), and may in the future include bio-electronic sensors.

Level 3 – Electronic Module: An electronic sub-assembly with functional blocks, which is comprised of individual electronic elements and/or component packages. An individual

module having an application-specific purpose including electronic (e.g., SiP), optoelectronic, or mechanical (MEMS). The module generally provides protection of its elements and packages, depending on the application to assure the required level of reliability. The module may be a company standard (catalog item) or custom (OEM-specific). Note: there will likely be some subdivisions of Level 2 and Level 3 descriptions to increase the granularity and clarity relative to what is included within each of these levels.

Level 4 – Electronic Unit: Any group of functional blocks that have been designed to provide a single or complex function needed by a system in order for the system to serve a specific purpose. The electronic unit may be comprised of electronic elements, component packages and/or application -specific modules. The function of the electronic unit may be electronic, optoelectronic, electromechanical, or mechanical or any combination thereof. The function may in the future include bio-electronic applications.

Level 5 – Electronic System: A completed, market-ready unit dedicated to combining and interconnecting functional blocks. The functional blocks are generally comprised of electronic units, but may also include electronic modules, electronic packages, or electronic elements. The electronic system product can include a housing, a backplane or a motherboard (into which the assemblies, modules, packages, or elements are inserted), and the cabling (electrical, optical, or mechanical) needed to interconnect the total functional block(s) into a configured system. The electronic system can vary in complexity from very simple to highly complex.

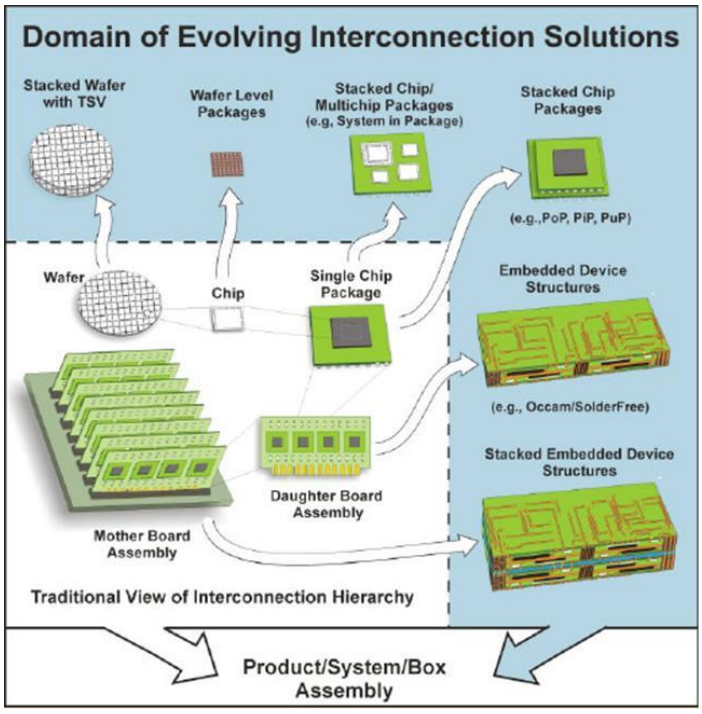


Fig. 5-7 Expansion of SMT packaging hierarchy with inclusion of new developments in packaging, including wafer levels and 3D stacks.

The interconnect hierarchy has evolved since the introduction of the transistor in 1960 [48]. Fig. 5-7 compares the traditional view of the hierarchy (lower left) to the emerging microelectronic technologies with growing ambiguity in interconnection level definition. In the early days, the divisions of levels for the various tasks involved in the creation of an electronic system were well defined. The semiconductor manufacturer created the integrated circuits (ICs); the IC chips were packaged for protection; a printed circuit facility built a substrate according to a design. Next, the package was assembled onto a board (using a soldering process) and used as "daughter card" for the next assembly of motherboard. The completed assembly would then be packaged in a suitable format, whether a computer, telephone switch, internet router, or any other product.

Now, there are new interconnections, such as a wafer-level packages and 3D stacks; some lack a clear category or definition. The blue area in the figure shows added new interconnections with lack of clear category; therefore, there is a need to find a way to embrace the emerging technologies that are already being deployed to create next generation products.

6. THERMAL CYCLE RELIABILITY OF PACKAGING ASSEMBLY

6.1. Conventional Reliability Methods

Reliability under thermal stress for package, PCB, and assembly depends on the reliability of constituent elements, e.g., the PCB and its global/local interfaces (attachments). As schematically shown in Fig. 6-1, three elements play key roles in defining reliability for a system, global, local, and interconnections. The characteristics of these three elements — package (e.g., die, substrate, solder joint, and underfill), PCB (e.g., polymer, copper (Cu), plated through hole, microvia), solder joints (e.g., via balls, columns) — together with the use conditions, the design life, and the acceptance failure probability for the electronic assembly determine the subsystem reliability.

In other words, reliability is the ability of a system (here microelectronics) to function as expected under the expected operating conditions for an expected time period without exceeding the expected failure levels. However, reliability is susceptible to early failure by infant mortality due to workmanship defect, lack of sound manufacturing, and use of a design without reliability consideration. Design for manufacturability (DfM), design for assembly (DfA), design for testability (DfT), and so on, are prerequisite to assure the reliability of the product. Only a design for reliability (DfR) can assure that a manufactured product with an acceptable quality will also be reliable in the product application. The elements of the system reliability are schematically shown in Fig. 6-1, and they are comprised of device/package/PCB and interconnections and also include consideration of design for reliability prior to assembly and subsequent manufacturing and quality assurance implementation.

In general, both statistical and probabilistic modeling approaches are considered in reliability methodology. Statistical approaches are employed after testing, whereas probabilistic predictive modeling is employed at the product design (DfR).

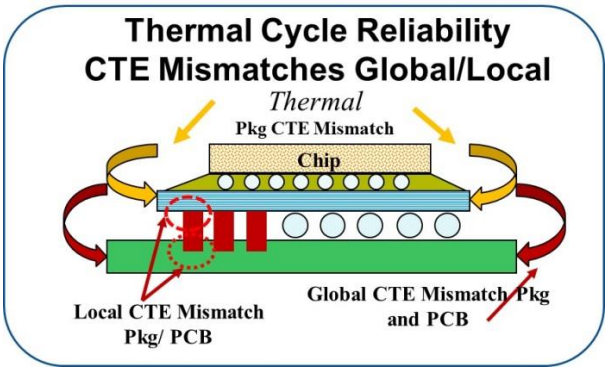


Fig. 6-1 Three key elements define reliability under thermal stress are due to global, local, and solder alloy coefficient of thermal (CTE) mismatches.

Mathematically, the reliability of an object at time t can be stated as [6]

$$R(t) = 1 - F(t)$$

where $R(t)$ is the reliability at time t (i.e., the proportion of parts still functioning), and $F(t)$ is the fraction of the parts or systems that have failed at time t. Time may be measured in calendar units or some other measure of service time such as on/off cycles or thermal or mechanical vibration cycles. The unit of time that makes sense depends on the failure mechanism. When several failure modes are present, it is often helpful to think in terms of several time scales.

A plot of the failure rate of a product as a function of time typically takes the shape of a "bathtub" curve (see Fig. 6-2). This curve illustrates the three phases that occur during the lifespan of a product from a reliability perspective. In the first, infant mortality phase, there is an initially high but rapidly declining failure rate caused by infant mortality. Infant mortality is typically caused by manufacturing defects that went undetected during inspection and testing and lead to rapid failure in service. Burn-in can be used to remove these units before shipment. The second phase, the normal operating life of the product, is characterized by a period of stable, relatively low failure rates.

During the operating life, failures occur apparently randomly, and the failure rate r is roughly constant with time. An exponential life distribution is often assumed to describe the behavior in this region. During the third phase, the wear-out period, the failure rate increases gradually due to wear-out phenomena until 100 percent of the units have failed. For some systems, the second steady-state region may not exist; for package, PCB PTHs/microvias, and solder joints; the wear-out region may extend over most of the life of the assembly.

Most wear-out phenomena can be characterized by cumulative failure distributions governed by either the Weibull or the log-normal distribution. Weibull distributions have been successfully used to describe solder-joint and PCB plated-through-hole fatigue distributions, while log-normal distributions are generally associated with electrochemical failure mechanisms. While these distributions may be quite narrow in some cases, their use should serve as a reminder that even with nominally identical samples, failures will be statistically distributed over time. A practical use of fitting a distribution to reliability data is to extrapolate to smaller failure rates or other environmental conditions.

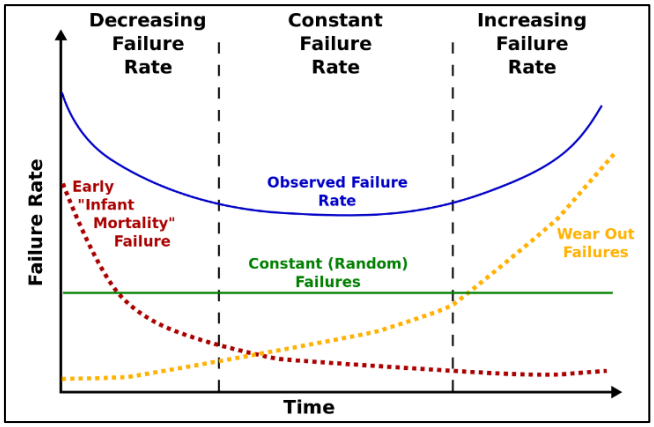


Fig. 6.2 Classic bathtub reliability curve showing the three stages during the life of a product from a reliability perspective: infant mortality, steady-state, and wear-out.

Numerous simulation approaches have been proposed to project failure distribution and reliability. For example, in 2000, John W. Evans, et al., presented a physics of failure based approach for virtual qualification of advanced area array assemblies, against solder fatigue failure [49]. Specifically, Monte-Carlo simulation to evaluate solder joint fatigue distribution, given material property variations and manufacturing capability. Simulation results were compared to data accumulated from two test environments and two BGA product types.

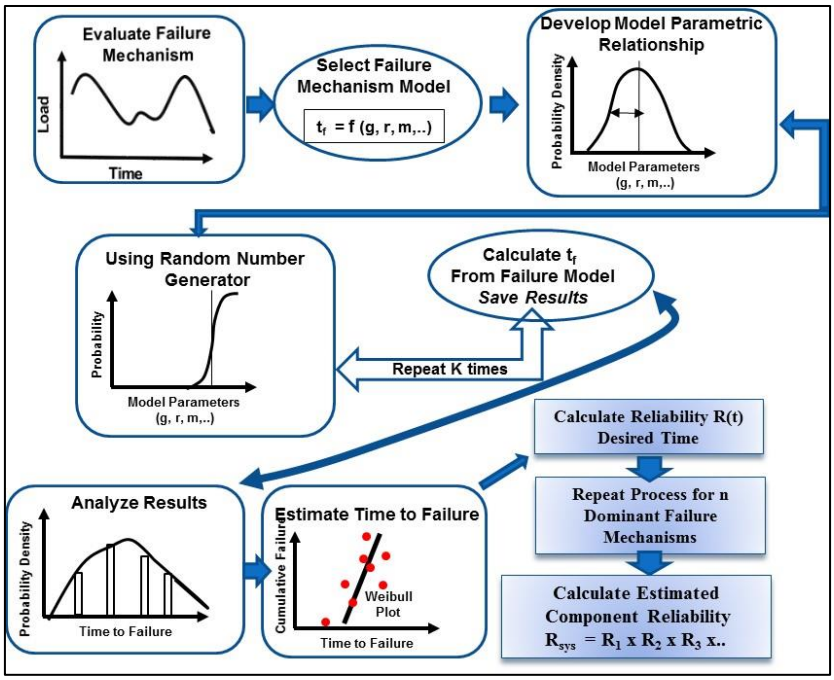


Fig. 6-3 Virtual qualification process by Monte Carlo simulation

For the thermal cycle to failure data in the range of 0C to 100°C, the simulation data were very representative of the actual test data. The 2-P (2-parameter) Weibull plots clearly showed the curvature in both the actual and simulated test data. When the 3-P Weibull plots were generated (see Fig. 6-4), the simulation and the actual test data were closely matched.

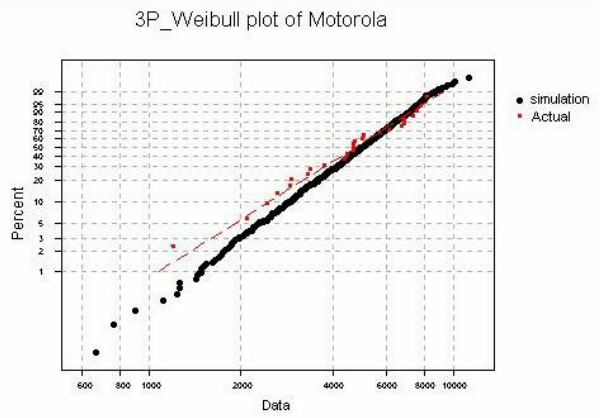


Fig. 6-4 3-P Weibull plots of simulation and actual test data for the 0/100C thermal cycle condition.

For the second thermal cycle test data in the range of –30°C to 100°C, simulations and actual data did not compare well. The 3-P Weibull shape parameter for the simulation and actual data were dramatically different. The difference explained by the fact that the solder joint reliability model used did not represent the process of failure for lower temperature. The –30°C to 100°C qualification temperature range exceeds the envelope of the model application.

The authors concluded that Monte Carlo simulation is a valuable tool for implementation into a virtual qualification test scheme for electronic devices and assemblies. It is compatible with proper physics of failure assessment, while providing advantages of properly treating uncertainty. In addition, much more information is available about the process of failure, from a Monte Carlo simulation.

In a recently published paper, February 2016, Hyunseok Oh, et al., agreed that among the analyses methods for solder joints, the conventional Monte Carlo simulation technique (random sampling) usually offers the most accurate results [50]. However, they conjecture that the computational cost becomes prohibitive for engineering problems with large computation requirement. They presented a table that compared the strength and weakness of four computational simulation methods including surface approximation technique that also reduces computational time. They proposed eigenvector dimension-reduction (EDR) simulation method to improve computational efficiency without accuracy penalty while reducing computational cost. As an example, the technique demonstrated to predict solder joint fatigue reliability of chip resistor assemblies. Two uncertainties were considered; one for solder joint height and the other one for chamber temperature. When key uncertainty parameters were defined, the simulation method was expand to project assembly reliability of solder joints under a field condition for a mobile device.

6.2. Prognostic Methodologies

Fig. 6-5 compares conventional reliability prediction approaches to prognostic methodologies that is used to predict remaining useful life (RUL) [51-57]. Conventional reliability methodologies focuses on analysis of failure data from the field with assumption of inherent constant failure rate. These methods tailor parameters such as quality, operating, and environmental conditions to reduce failures and improve reliability. On the other hand, prognostic methodologies predict the future performance of a package and assembly by assessing the extent of deviation or degradation of a system from its expected normal operating conditions. Prognostics emphasizes on predicting the time at which a system or a component will no longer perform its intended function. This lack of performance is most often a failure beyond which the system can no longer be used to meet desired performance. The predicted time then becomes the RUL, which is an important concept in decision making for contingency mitigation. The science of prognostics is based on the analysis of failure modes, detection of early signs of wear and aging, and fault conditions.

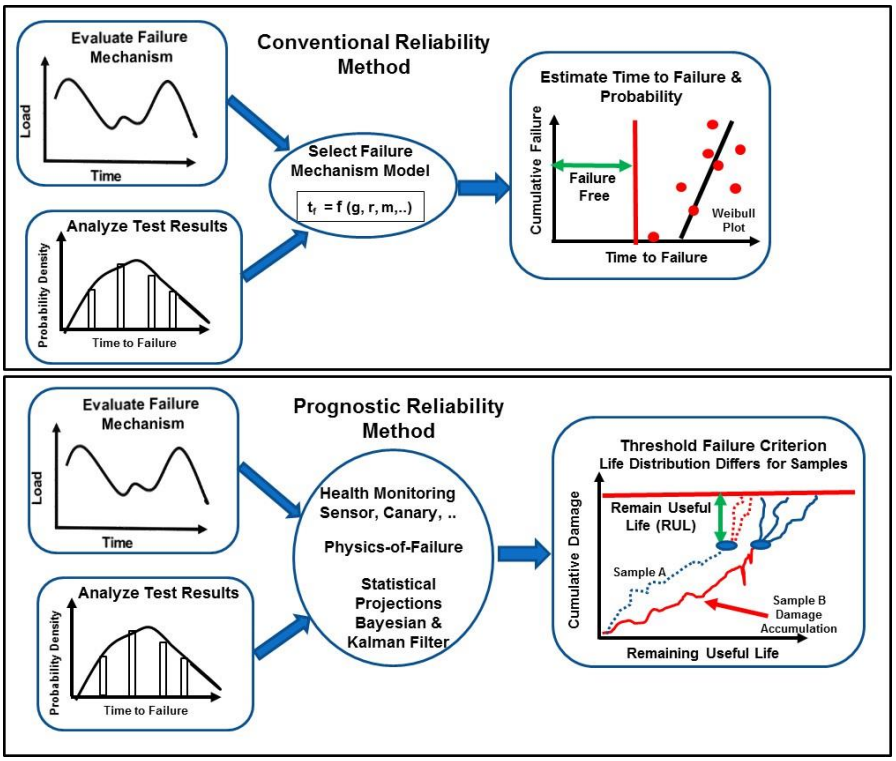


Fig. 6-5 Comparison of conventional reliability prediction methods to prognostic approaches that predict remaining useful life (RUL)

An effective prognostics solution is implemented when there is sound knowledge of the failure mechanisms that are likely to cause the degradations leading to eventual failures in the system. It is therefore necessary to have initial information on the possible

failures (including the site, mode, cause and mechanism) in a product. Such knowledge is important to identify the system parameters that are to be monitored. Potential uses for prognostics is in condition-based maintenance. The discipline that links studies of failure mechanisms to system lifecycle management is often referred to as prognostics and health management (PHM)— significant publications in microelectronics within the last decade. Other nomenclatures includes system (structural) health management (SHM).

Simply, PHM is the process of monitoring the health of a product and predicting the remaining useful life. The benefits of PHM include: (1) providing advance warning of failures; (2) minimizing unscheduled maintenance, extending maintenance cycles, and maintaining effectiveness through timely repair actions; (3) reducing the life cycle cost of equipment by decreasing inspection costs, downtime, and inventory; and (4) improving qualification and assisting in the design and logistical support of fielded and future systems. Technical approaches to building models in prognostics can be categorized into data-driven, physics-based, and hybrid approaches.

Data-driven approaches use information from previously collected data (training data) to identify the characteristics of the currently measured damage state and to predict the future trend. The data-driven method that does not use any particular physical model is powerful in predicting near-future behaviors, whereas the physics-based method has advantages in predicting long-term performance of the system by identifying model parameters. Since generally solder joint failure under thermal and mechanical cycling is a fatigue phenomenon with damage progression, the physics-based method is a more appropriate than data-driven approach. In the physics-based method, model parameter estimation has a great effect on evaluating the system's health status and predicting the RUL. So, the key differences between the two methods includes: (1) availability of a physical model and (2) use of training data to identify the characteristics of the damage state. Hybrid approaches combine the two to improve prediction for the performance.

Literature provides a wealth of papers on the PHM subject, but generally the simulation model proposed is specific and lack simplification needed for wider use. A recent paper on this topic addresses this weakness by proposing physics-based model using a three-step concept (TSC) for projecting reliability of microelectronics [58]. The first step involves the use of the classical statistical Bayes' formula, a diagnostics tool. It identifies, on the probabilistic basis, the faulty (malfunctioning) device(s) from the signals (''symptoms of faults''). Then, physics-of-failure-based Boltzmann–Arrhenius–Zhurkov's (BAZ) model was used to estimate the remaining useful life (RUL). If the RUL is not long-enough, restoration of the faulty device becomes necessary. The restored device is then put back into operation (testing), provided its failure-free probability of operation is found to be satisfactory. If the operational failure nonetheless occurs, the third, technical diagnostics step needed to update reliability. Statistical beta-distribution, in which the probability of failure is treated as a random variable, is suggested to be used at this step.

The data-driven methods are categorized into two key methods: (1) the artificial intelligence that includes neural network (ANN) and fuzzy logic and (2) the statistical methods that includes Gaussian process (GP) regression, least square regression, and hidden Markov model. In the following section, I present an ANN methodology that was developed to project cycles-to-failures for assemblies of BGA and CBGAs.

7. ARTIFICIAL NEURAL NETWORKS FOR CGA ASSEMBLY RELIABILITY PROJECTIONS

7.1. ANN Background

Artificial neural networks (ANN) — or simply neural networks — are information processing systems emulating some of the processing characteristics of the human brain [59]. Much like its biological counterpart, an artificial neural network consists of a large number of densely interconnected simple processing elements. This brain-like organization imparts to the neural network parallel processing and learning capabilities.

The above characteristics make the neural networks useful for tasks that are either impossible or very difficult to accomplish using traditional computer programs. These tasks include:

- Pattern recognition: recognition and separation of patterns contained in data
- Prediction: determination of a value of a variable from a set of given values
- Conceptualization: determination of conceptual relationships within data sets
- Filtering: smoothing a noisy signal
- Optimization: determination of the optimal values from a set of given values

All of the above functions are accomplished by simply altering the arrangement and number of processing elements. Most neural networks, like the human brain, require iterative feedback training. Training can be either supervised or unsupervised. In supervised training, the network is provided a set of input-correct output pairs to train on. Unsupervised training means only input data with some guidelines are given. In general, prediction requires supervised training, while classification, conceptualization, filtering, and optimization can employ unsupervised training.

Neural networks have two main components: the processing elements and the connections between them. The processing elements — sometimes called neurons, units, cells, or nodes — function as information processors; the connections function as information storage. Fig. 7-1 shows a diagram of a processing element with connections going in and out of it.

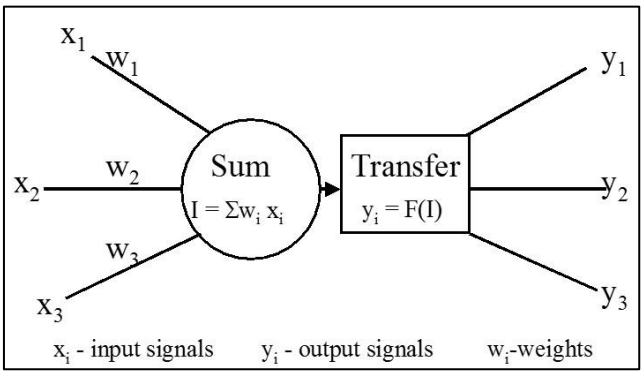


Fig. 7-1 Schematic of an ANN structure

Each processing element performs two distinct functions. First it calculates a weighted sum of the input signals, and then it applies a transfer function to this sum and outputs the result. Transfer functions are generally nonlinear since nonlinear functions are required to solve nonlinear problems. Nodes within a network are arranged in layers. The neural network

shown in Fig. 7-2 consists of an input layer, a hidden or processing layer, and an output layer. The initial data enters the network through the input layer. Most of the processing takes place in the hidden layer. If the complexity of a given problem is high, more hidden layers may be required. Finally, the output layer yields the desired information.

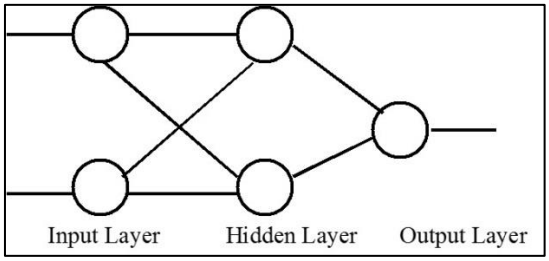


Fig. 7-2 Schematic of a simple ANN structure with a one hidden layer

7.2. Backpropagation

A number of neuromophic learning paradigms have been reported in the literature. The majority of these are supervised learning techniques including the error backpropagation (EBP) learning algorithm. The name "backpropagation" comes from the training method used during the learning process—back propagation of error. This training method is simply a gradient descent method that minimizes the total squared error of the output computed by the net. The very general nature of the backpropagation training method means that a backpropagation net can be used to solve problems in many areas.

In real world applications, EBP often suffers convergence problems. A new learning algorithm technique called cascade correlation (CC) has shown encouraging results. Both empirical and mathematical results has been validated [60] for a more general algorithm of cascade error projection (CEP), of which cascade correlation is a special case. CEP is a simple learning method using a one-layer perception approach followed by a deterministic calculation for another layer.

7.2.1. Cascade Error Projection (CEP)

Fig. 7-3 shows the CEP neural network architecture [60], which shaded squares and circles indicate frozen weights; a square indicates calculated weights and a circle indicates learned weights. The shaded circles or squares indicate either the learned or calculated weight set that is computed and frozen. A circle indicates that perceptron learning is applied to obtain the weight set, and a square indicates that the weight set is deterministically calculated. In the following a brief summary of mathematical approach for CEP is provided.

The energy function is defined as:

$$\sum_{p=1}^{P}\{F_h^p(n+1)-\frac{1}{m}\sum_{o=1}^{m}(t_o^p-o_o^p)f'^p_o\}^2$$

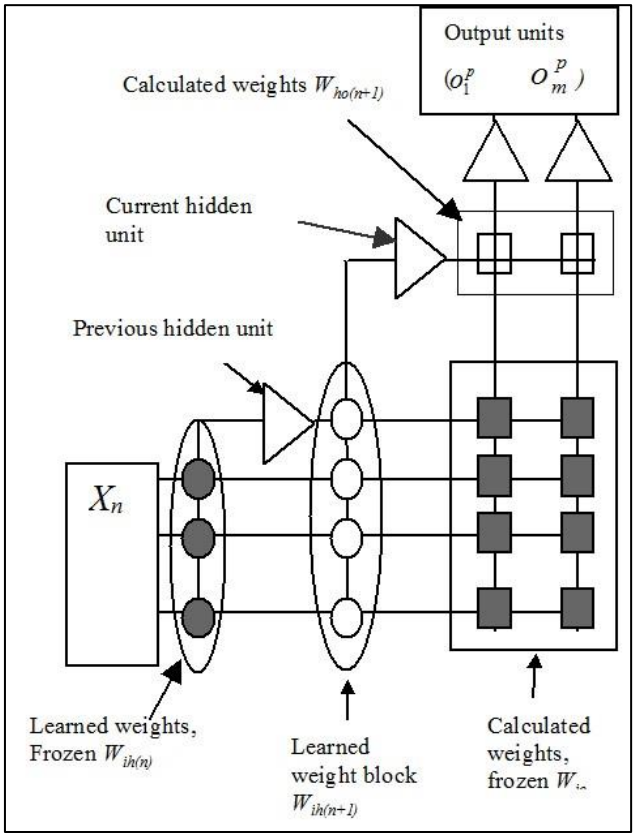


Fig. 7-3 The architecture of CEP includes inputs, hidden units, and output units

The weight update between the inputs (including previously added hidden units) and the newly added hidden unit is calculated as follows:

$$\Delta w_{ih}^p = -\frac{\partial \mathrm{E}^p}{\partial w_{ih}^p} \quad \text{(a)}$$

and the weight update between hidden unit $n+1$ and the output unit o is

$$w_{ho} = \frac{\sum_{p=1}^{P} \varepsilon_o^p f'^p_o \; f_h^p(n+1)}{\sum_{p=1}^{P} [f'^p_o \; f_h^p(n+1)]^2} \quad \text{(b) with } f(x) = \frac{1-e^{-x}}{1+e^{-x}}$$

m is the number of outputs, P is the number of training patterns.

Error $\varepsilon_o^p = t_o^p - o_o^p(n)$; where $o_o^p(n)$ is the output element o of the actual output $o(n)$ for training pattern p, *and* t_o^p is the target element $\boldsymbol{o}$ for training pattern p. n indicates the number of previously added hidden units.

$f'^{p}_{o}(n) = f'^{p}_{o}$ denotes the output transfer function derivative with respect to its input.
$f^{p}_{h}(n+1)$ denotes the transfer function of hidden unit $n+1$.

The CEP algorithm is processed in two steps:

- Single Perceptron learning which is governed by equation (a) to update the weight vector $W_{ih}(n+1)$
- When the single Perceptron learning is completed, the weight set $W_{ho}(n+1)$ can be obtained by the calculation governed by equation (b).

7.3. Artificial Neural Network (ANN) Approach

Neural networks are much more than gathering a set of raw data and feeding it directly to a modeling algorithm. Success requires a sequence of coordinated steps. The process of developing neural networks to predict reliability of advanced electronic follows the sequential steps of: (1) identification, (2) transformation, (3) model, (4) analysis, and (5) Prediction. These steps are further analyzed in the following sections.

7.3.1. Identification

Identification and characterization of the data are a critical step in the modeling process because the results are so dependent on the quality and selectivity of the input parameters. The first priority is to determine what data will be used to build the models ("training" data), and determine how well the chosen model works ("validation" data). When testing the effectivity of the models, it is extremely important to have an independent data set that contains examples that were not used to train the models, and that is why a portion of the data (randomly selected) is set aside for validation. This verifies the ability of the models to work well on new, unseen data, as they must when they are implemented for actual reliability prediction.

Once the data set has been identified, it is necessary to determine which of the data fields will be used for predictors (inputs) and which parameter will be predicted (output). The inputs are sometimes called independent variables, and the output the dependent variable since its value is driven by the values of the other fields. The format of the output variable will directly affect which modeling approach is used. New input variables can be created from existing variables to create more powerful modeling.

The raw data often are not ready to be modeled because of data inadequacies. Some of the common problems encountered with data for the ANN modeling are format, feature, null, data distribution, outliers, difference between validation and training data, etc. Most neural networks deal with numerical fields and data in text or other format need be translated in numerical values. For example, "yes" or "no" have to be changed to 1's and 0's. If needed, data distribution needs to be modified for different distributions within a data set or exclusion of outliers prior to their use in the data set.

7.3.2. Transformation

Properly representing and transforming data can make the difference between success and failure in the modeling process. There are several different approaches to coding and representing data so that certain characteristics are more obvious to the subsequent modeling algorithm. These include data coding, data sampling, feature extraction, etc. Symbolic data need to be converted to numeric, e.g., temperature (very cold, cold, room temperature, warm,

and hot) and many types of ratings (excellent, good, fair, poor). For these cases, an integer value can be simply assigned to the original symbolic values, such as excellent = 4, good = 3, and so forth.

7.3.3. Modeling

Once the data have been preprocessed and placed into the proper formats, they are ready to be mined for information. The neural networks models are trained to classify or estimate outputs. Several different mining schemes should be evaluated to determine which neural networks provide the best performance for the given type of data. The model step consists of defining neural networks for the selected problem type. This involves:

- Designating the inputs and the outputs to the model
- Identifying the training and validation sets
- Selecting the mining strategies, as well as the modeling parameters
- Executing the resulting model
- Analyzing the resulting models
- Applying the best mining strategy to subsequent data

7.3.4. Analysis

When analyzing the modeling results, it is very important that the performance of any model be determined with data that were not for training. Testing models on unseen data more closely represents the manner in which the model will be used in practice (i.e., on data that were not used for training) and is therefore a more realistic evaluation approach. After modeling, error statistics should be calculated to determine a comparison measure of how well each model is working. The error statistics are calculated by subtracting the model estimate from the actual value of the output to determine the error for each sample. Then, aggregate statistics can be calculated that describe how well the model performed on the data sets.

Errors calculation should include average absolute error, maximum absolute error, standard deviation, and coefficient of determination. For example, the overall absolute error provides an average of absolute error for each sample, a measure of the overall goodness of the model. Standard deviation measures variance of the error. The larger the variance, the less consistent the model is in overall ranges of values.

7.4. ANN Verification for BGA Reliability

As stated previously, the first step in an ANN modeling is how well the model works using an independent validation data set and then build the model based on training data. The CEP algorithm with 3-cascaded hidden layers was validated first using theoretical modeling of cycles-to-failure data gathered for BGA [61]. Three thousands (3,000) iterations for each neutron were utilized to minimize error associated with the model.

7.4.1. Backpropagation ANN Model for Reliability Projection of BGA

A Taguchi L27 design of experiment (DOE) was used to mode the effect of four key BGA variables, at 3 levels each that affect solder attachment reliability when subjected to thermal cycling [61]. The variables included the BGA pad diameter, ball diameter, weight

per solder joint, and applied displacement. No interaction between displacement and the other three variables was assumed; allowing use of fractional factorial reduced analysis time and cost. The shear deformation was assumed to be due to a 20-minute thermal cycle in the range of 0-100°C with 5 minutes ramps and dwells. Thermomechanical properties as well as surface tension for eutectic solder alloy, 63Sn/37Pb, were considered in finite element analysis. The inelastic energy required for empirical projection of solder joint fatigue life was calculated.

Fatigue life projections based on one method show that it is inversely proportional to the maximum inelastic energy density with an index of one; the index was two for the average energy rate of change per cycle. The Coffin-Manson relation has an index of approximately two. So, it became apparent that the fatigue life is inversely related to the inelastic energy to within a proportionality constant. Table 7-1 lists Taguchi runs, modeling results, and projection using Darveaux's model [62] adapted from Tables 1.2, and 5 of reference [61].

The table was sorted based on cycles-to-failure data from low-to-high to reveal the key variables. The assemblies with highest deformation level and the smallest ball diameter show the lowest cycles-to-failure. Those with the least deformation and the largest ball diameter show the highest cycles-to-failure. Weight and pad diameter in combination with ball diameter and deformation level cover the mid range failures.

Table 7-1 Reliability of PBGA assembly modeled using four variables (adapted from Reference 61)

Run	Pad Diameter microns	Ball Diameter microns	Weight per Solder Joint (mg)	Applied Displacement microns	Darveux
3	0.5	254	1016	12.5	47
11	2.55	254	635	12.5	62
19	5	254	254	12.5	72
2	0.5	254	635	8.75	116
10	2.55	254	254	8.75	135
21	5	254	1016	8.75	160
5	0.5	508	635	12.5	239
24	5	508	1016	12.5	288
13	2.55	508	254	12.5	376
4	0.5	508	254	8.75	564
1	0.5	254	254	5	634
7	0.5	762	254	12.5	642
15	2.55	508	1016	8.75	686
23	5	508	635	8.75	749
18	2.55	762	1016	12.5	759
26	5	762	635	12.5	961
9	0.5	762	1016	8.75	1088
12	2.55	254	1016	5	1305
17	2.55	762	635	8.75	1631
25	5	762	254	8.75	1919
6	0.5	508	1016	5	1927
20	5	254	635	5	1970
22	5	508	254	5	2338
14	2.55	508	635	5	2424
8	0.5	762	635	5	3461
27	5	762	1016	5	4165
16	2.55	762	254	5	4241

It was suggested that a model was required to quickly estimate fatigue life for any set of input parameters. A linear regression could be used for such a model. However, the disadvantage of a linear regression model is that the form of the model must be assumed *a priori*, and an inaccurate form of the regression model will lead to inaccuracies in the output. ANN was considered for projection since this modeling technique does not require the form of the data to be assumed *a priori*.

A backpropagation ANN technique was used for this purpose. Out of the 27 experiment runs, 18 were used for training the network and 9 were used for testing the network an additional 12 test units were used to further extensively validate the neural model. The least error in the ANN results occurred for Darveux's model based on the differences between projection and actual test data. However, higher error values obtained for the inverse estimate of maximum inelastic energy.

7.4.2. ANN CEP Training Data Error Compare to Literature

Prior to proceeding with the CEP ANN model, the error results from this model with 3-hidden layers and 3,000 iterations were compared to those presented previously employing a backpropagation model. Projections were made on BGA fatigue life. Fig. 7-4 shows a comparison between the target cycles-to-failure and actual projection based on CEP. The training of the CEP ANN model progressed smoothly which led naturally to the next step. The knowledge of network training data, then, was captured as nonlinear function of parameterized weight component and neural transfer function. As knowledge captured in training, we tested the network with the new set of data consisting of 12 input data (Table 4, Reference 61). Its prediction is shown in Fig. 7-5.

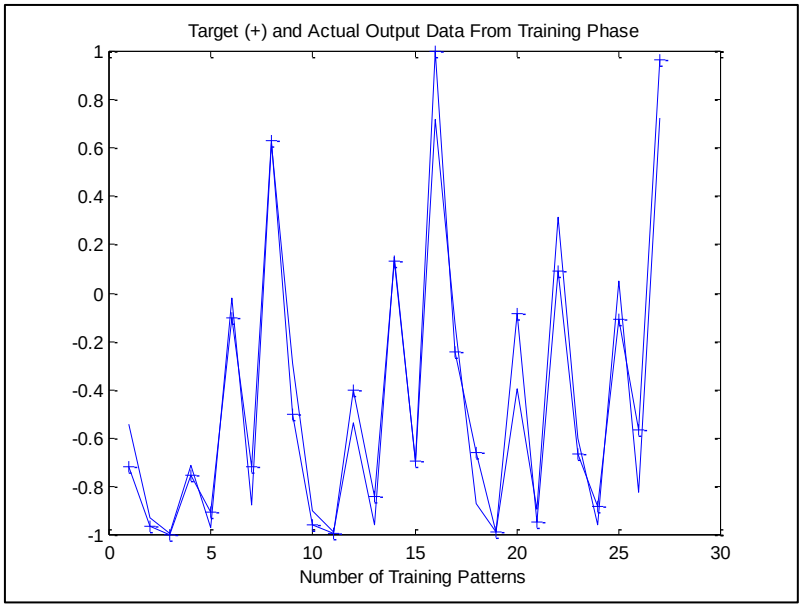


Fig. 7-4 The target (+) and actual learning data using CEP ANN modeling

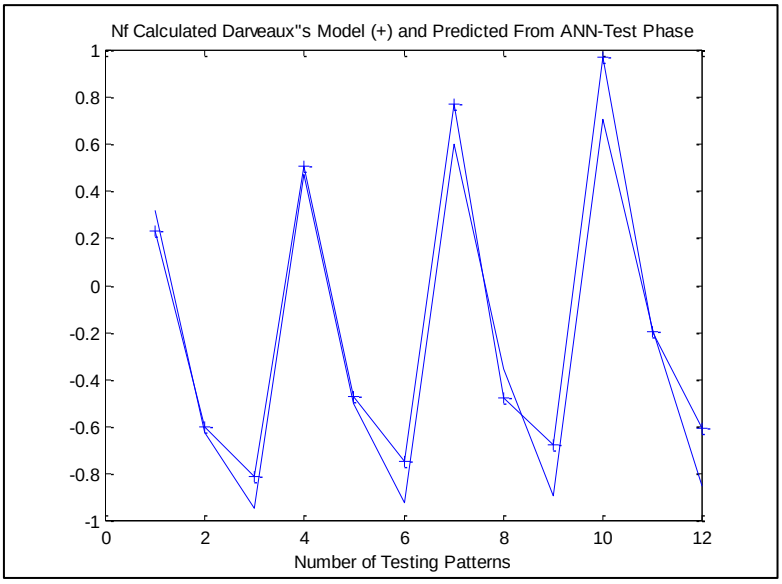


Fig. 7-5 Cycles-to-failure (+) and prediction using ANN CEP algorithm

To compare CEP ANN modeling projection against the Backpropagation technique presented in the literature, for both modeling efforts, the differences between calculated and prediction were calculated for the 12 data set. Results are shown in Fig. 7-6.

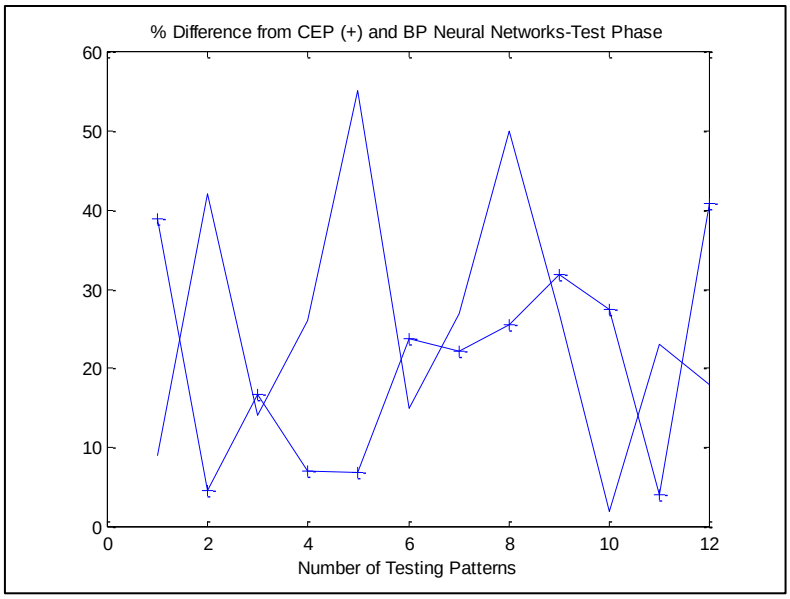


Fig. 7-6 The difference between calculated and prediction using either CEP (+) or Backpropagation ANNs

Again, it is apparent that the CEP algorithm provides a better prediction than the backpropagation ANN used in the literature for the given data set. Moreover, one of the key advantages of CEP is that it is not required to know the prior number of hidden units. This feature will save time for learning and therefore requires much less calculation time and simple calculation steps when compared to the Backpropagation ANN.

7.5. ANN CEP for CBGA Reliability

Subsequent to validation of CEP ANN using literature data for BGA life cycle, this technique was employed to project the cycles-to-failure data set for a ceramic BGA with 625 I/Os. Fig. 7-7 shows cycles to first failures for CBGA625 under four different thermal cycling conditions [63]. These plots were generated by ranking cycles-to-failures from low to high and then approximating the failure distribution percentiles using a median plotting position, $F_i = (i-0.3)/(n+0.4)$.

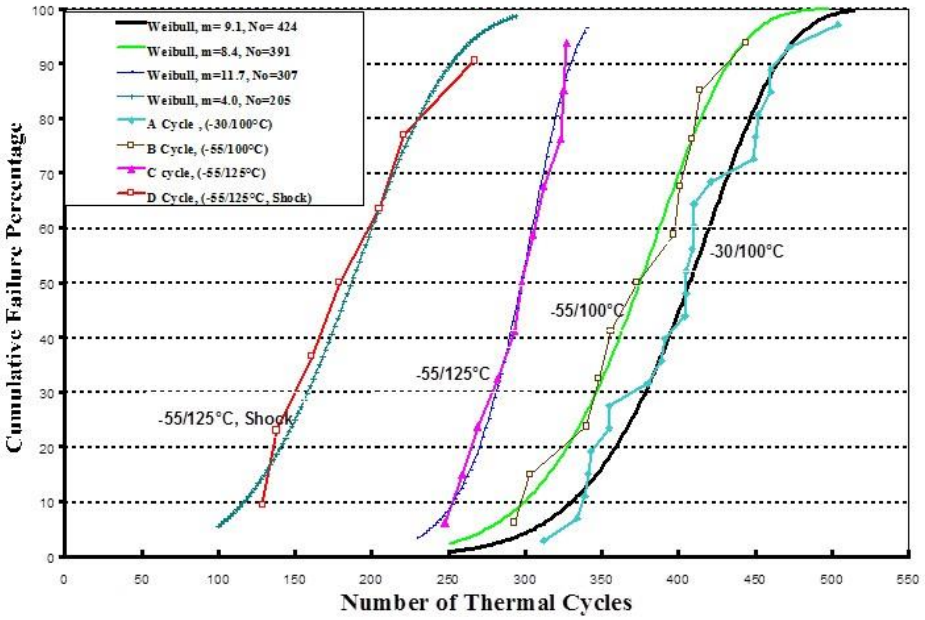


Fig. 7-7 Cycles-to-failure for CBGA 625 assemblies under different cycling conditions

The data set presented in Fig. 7-8 consists of 53 data points and each point included 3 elements: cumulative probability percentage, temperature cycle range (ΔT), and ramp rate (thermal cycle versus near thermal shock). The output was cycles-to-failure. Forty two (42) data points out of 53 were considered for training (input and output sets) and the remaining 12 data points used for testing. The top plots (see Fig. 7-8) show learning results with the green line being the target for training data set and the blue line as the network learned. The lower plots show unlearned data set (blue line) following the green line as the target data set. The error points from the two are marked by asterisk (*) indicating low error values and relatively constancy for the data set.

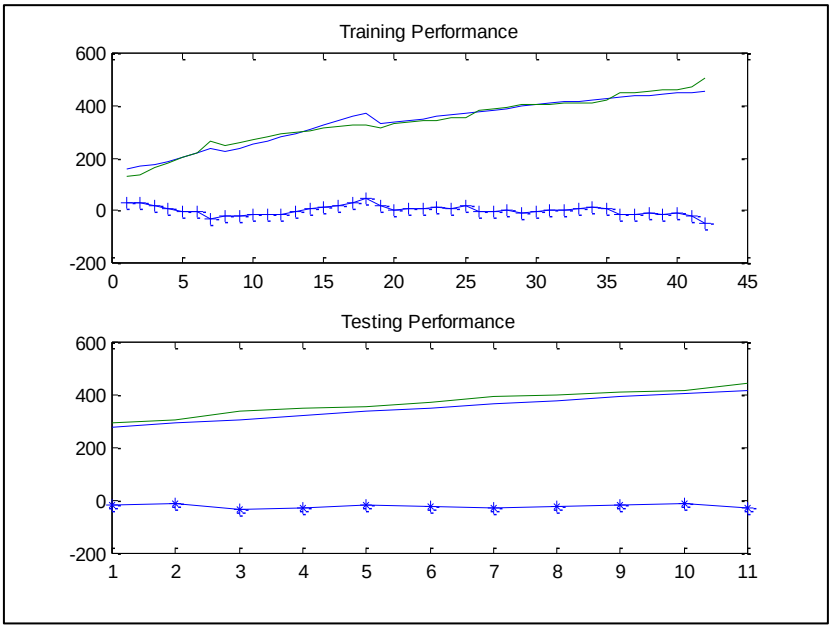


Fig. 7-8 Training and Testing Performance

Fig. 7-9 and 7-10 provide training and projection for data set for CBGA performed in the range of 0-100°C [64]. The figures include plots of the actual, projection, and error for the data set. Again, low errors in values indicate applicability of the CEP ANN model for projection.

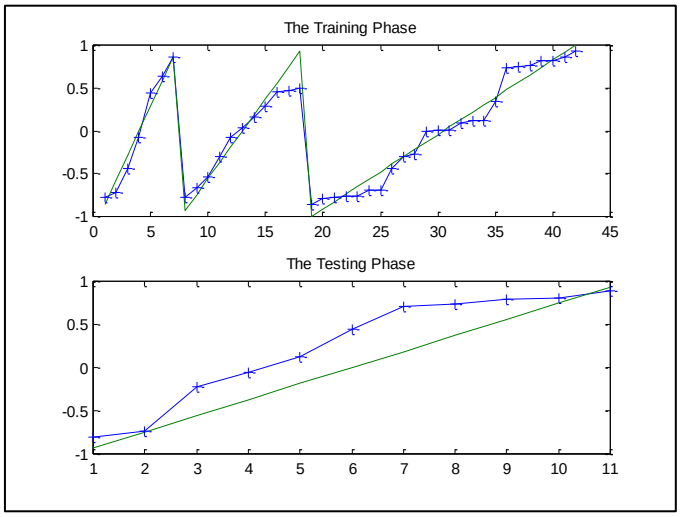


Fig. 7-9 Training and Testing Performance (0-100°C range)

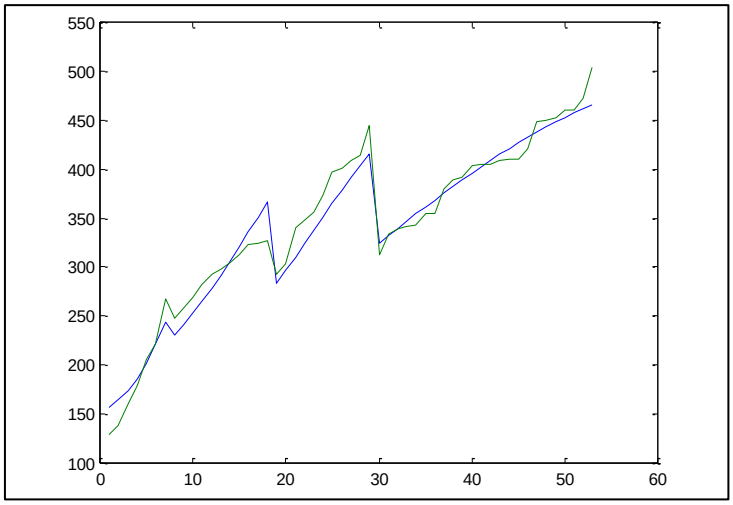


Fig. 7-10 Target (green) and actual data (blue)

7.5.1. Interpolation- CEP ANN and CTFs vs ΔT for CBGA

Fig. 7-11 shows cycles-to-failure projections at three probability levels versus temperature ranges. The full data set (53 data points) previously reported for training and testing of the network was considered in generating these plots. The temperature ranges varied between 0-100°C (ΔT = 100) to –55/125°C (ΔT = 180). No attempt was made at this stage of modeling to project data beyond the test boundary. Cumulative probability failures for 0.1, 0.5, and 0.9 were shown to represent a range of failure probability. Interpolation within the boundaries are well represented, and data trends are as expected.

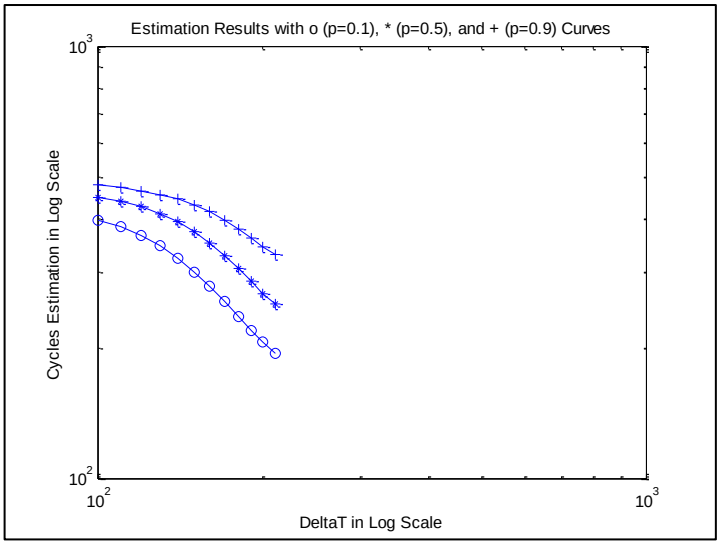


Fig. 7-11 Predictions of cycles-to-failures at 10% (o), 50%(*), and 90% (+).

7.5.2. Extrapolation- CEP ANN and CTFs vs ΔT for CBGA

Extrapolation of data beyond the provided thermal cycle regime is desirable. Extrapolation capability was tested using CEP ANN for projection. Fig. 7-12 shows cycles-to-failure for a lower ΔT is compared to plots shown in the previous figure. To improve the projection for lower ΔT, 8 CTF data points in the range of 0-100°C were added [64]. Fig. 7-13 provides more details, especially in the area of extrapolation. It is apparent that a reduction in cycles-to-failure leads to a very slow decrease rate. This is in contrast with the Coffin-Manson extrapolation projection. In addition, failures for the three levels of probability failures converged to a single point, possibly due to inaccuracy in extrapolation.

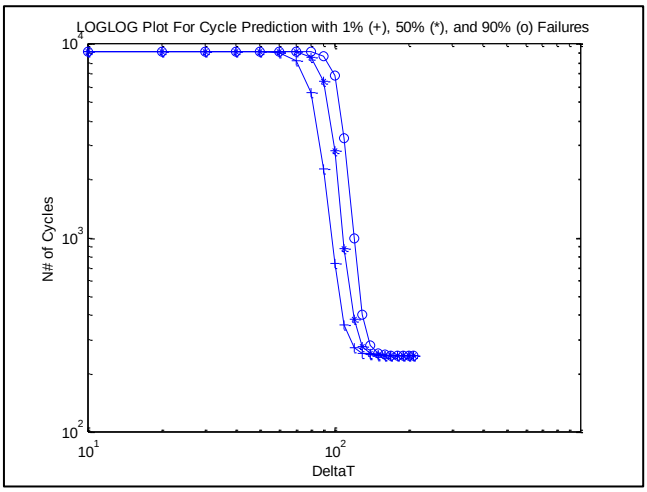


Fig. 7-12 Log-Log plot of projected cycles-to-failures versus temperature cycle range

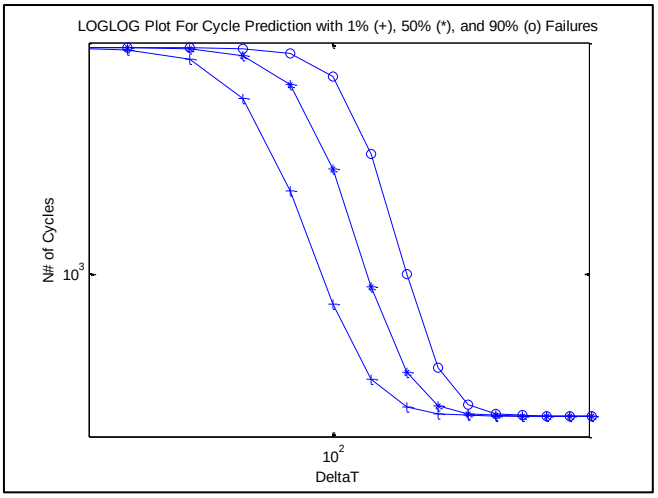


Fig. 7-13 Log-log plot of cycles-to-failure versus temperature range

8. SUMMARY

For five decades, the semiconductor industry has distinguished itself from other industries by continuously shrinking ICs enabling functional improvement—Moore's Law—and developing miniaturized electronics products at lower cost. The next shrinkage is packaging technology. Packaging shrinkage is enabled by using flip-chip ball grid array (FCBGA), through silicon via (TSV) interconnections, TSV-less interposers, and 3D TSV stacking technologies as well as packaging die at wafer level using fan-in/fan-out configurations. A few key points on packaging trends discussed in this paper are summarized below.

- Moore's Law has been kept alive since 2000s by various technical costly methods. At 90 nm, stain silicon was introduced, at 45 nm, new materials layered on the silicon, at 22 nm, tri-gate transistors invented, and at 14 nm, a new photolithograph process was developed to create finer feature requirements. It is unclear as how much further scaling is possible since at 2 nm, transistor would be just 10 atoms wide, and it is unlikely that they will operate reliability at such a small scale.
- The ITRS projects that by 2020–2025, system integration or "more than Moore" become the new option for miniaturization by utilizing the vertical dimension, i.e., a 3D approach. The iNEMI team predicts a moderate growth for QFP/LCC and chip-on-board (COB) whereas a significant growth both for QFN and WLP packaging technologies. Others project high-volume adoption of fan-out WLP, 2.5D/3D, and evolution and growth of fan-in WLP and flip chip. Fan-in and fan-out WLP act as complementary, rather than competing, technologies. The iNEMI projects a decline in conventional DIP leaded package as well wire-bonded die BGA with conventional pitch, whereas a moderate increase for wire-bonded die of finer pitch BGAs. Significant increases are projected for flip chip FPGA as well as stack packaging technologies.
- The iNEMI team also identified the new packaging technologies: (1) wafer level packaging (WLP) and bonding, (2) system in package (SiP), (3) printed electronics, (4) direct bonding interconnect, (5) new conductive and dielectric materials, and (6) 3D integration.
- The QFN packaging technologies show moderate growth. These are new categories of packages—leadless; which have no balls or columns for interconnection, they use only solder. IPC designate them as bottom-termination components (BTCs); other designated names in literature include dual-row/multi-row QFN (DRQFN/MRQFN), dual flat no-lead (DFN), and land grid array (LGA) packages.
- More than 1000 I/O ceramic CGAs are now offered by package suppliers for high-reliability applications. A new class of package – class Y- was added to the specification, MIL-PRF-38535, Revision K in order to cover high I/O CGA use. Key packaging trends for high-reliability applications identified as: (1) ceramic quad flat pack (CQFP) to area array packages, (2) CBGA to CCGA/CGA (>500 I/Os) and land grid array (LGA), (3) wire-bond to flip-chip die within a package, (4) hermetic to non-hermetic packages (>1000 I/Os), (5) high-lead solder columns to columns with Cu wrap , (6) Pb-Sn to Pb-free, including potential use of a Cu column, and (7) land grid with conductive interconnects rather than Pb-free solder
- For high density packaging, the migration to 3D using conventional interconnection method has become mainstream. Currently, 3D packaging consists of stacking of packaged devices, called package-on-package (PoP), stacking of die within a package

called package-in-package (PiP), or stacked wire-bonded die (primarily memory). The PoP packaging technologies were categorized in three styles: (1) PoP with center mold and flip chip, (2) PoP with partial cavity structure, and (3) through-mold via (TMV™).

- The 2.5D packaging technology had significant growth since it is considered to be an interim solution until challenges associated with the 3D TSV technology implementation are resolved. The 2.5D packaging (TVS-less)—active on passive-with TSV silicon interposer—implemented by an FPGA manufacturer (SLIT, silicon-less interconnect technology) transitioning finer pitch die with 28 nm technology to coarser 65 nm technology. Another high volume package supplier introduced the 2.5D EMIB technology that uses silicon bridges in a laminate to take advantage of higher functionality and lower cost. Other TVS-less interposers include: SLIM, silicon interposer-less integrated module, i-THOP, integrated thin-film high density organic package, and TSH, through silicon hole.
- Embedded components are defined as a passive/active discrete/devices that are placed or formed on inner layers of substrate/board. Embedded passives within board is near maturing whereas new classes of integrated passive devices within package are continue to emerge. Two different approaches of component assembly are used: face up and face down. The face-up technology, because of its better heat dissipation characteristic, is widely used for various embedded active including power-MOSFET, IGBT, and diodes.
- Printed electronic technology (PET) is complementary to silicon chip technology, which industry continues to find special applications for, with significant cost per area and throughput benefits. It is forecasted that the PET market will outpace silicon chip electronics because of its ubiquity.
- In recent years, MEMs/MOEMs packaging is driven by consumer products posing new lower cost requirement, larger volume implementation, and standardization approaches for applications. Previously, the technology was employed for automotive- and high-reliability applications, so, emphasis was placed on reliability. These technologies use both conventional packages such as TO and butterfly styles as well as advanced 3D stacking technologies such as BTCs.
- RF packaging trends were illustrated from mature to emerging technologies. For RF systems, micro-miniaturization and system integration on silicon, system on chip and system-in-package are key enabling technologies. The trends for multi-chip packaging technology were also illustrated showing that DC-DC converters in conventional hermetic packages are still in use in high-reliability applications. New miniaturized multi-chip package is emerging. New materials are needed for further microelectronics miniaturization. Changes in materials include RoHS implementation (tin-lead to Pb-free) with proliferation of alloys to Cu pillar for FC and low dielectric to new package underfill materials. The packaging technology trends were concluded with defining hierarchical ranking covering die, device, package, and system levels. The traditional hierarchy of packaging technologies is growing into ambiguity with emerging microelectronics including those with movable/sensing parts such as MEMs and MOEMs.
- Package, PCB, and assembly are the three key elements affecting reliability under thermal stresses. These elements with the use thermal conditions, the design life, and acceptance failure probability determine the subsystem reliability. Wear-out failure phenomena can be characterized by cumulative failure distributions using either the Weibull or the log-normal distribution.

- Monte-Carlo method was used to simulate solder joint fatigue distribution including material property variations and manufacturing capability. It was shown that risk projected based on 2- and 3-parameter Weibull distributions was different and needs to be considered, especially for high-performance applications. Also, it was shown that the risk based on log-normal distribution is less conservative than the risk from Weibull, i.e. log-normal projects higher cycles-to-failure.
- We compared conventional reliability prediction approaches to prognostic methodologies that predict remaining useful life (RUL). Conventional approaches focus on analysis of failure data from the field with assumption of inherent constant failure rate; whereas prognostics place emphasis on predicting the time at which a system or a component will no longer perform its intended function. The predicted time then becomes the remaining useful life (RUL), which is an important concept in decision making for contingency mitigation. The science of prognostics is based on the analysis of failure modes, detection of early signs of wear and aging, and fault conditions.
- The prognostic data-driven methods were categorized into two key methods: (1) the artificial intelligence including neural network (ANN) and fuzzy logic and (2) the statistical methods including Gaussian process (GP) regression, least square regression, and hidden Markov model. Test results for BGA was used to compare backpropagation ANN and the cascade error projection (CEP) ANN algorithm. CEP ANN showed better prediction than backpropagation ANN.
- CEP ANN method also employed to project the cycles-to-failure for a ceramic BGA with 625 balls. Training was based on four sets of thermal cycle test data covering thermal profiles of 0°/100°C, –35°/100°C, –55°/100°C, and –55°/125°C. Within ΔT test boundaries, ANN projections for cycles-to-failure were excellent; however, projections for cycles-to-failure were poor for outside of the test results' envelop.

9. Acronyms and Abbreviations

2D	two dimensional
2.5D	pseudo 3D with passive interposer
3D	three dimensional
ANN	artificial neural network
aQFN	advanced quad flat no-lead
ASIC	application-specific integrated circuit
BGA	ball grid array
BSI	back-side illuminate
BTC	bottom termination component
CBGA	ceramic ball-grid array
CCD	charge coupled device
CCGA	ceramic column grid array
CEP	cascade error projection
CIS	CMOS imaging sensor
CGA	column grid array
CMOS	complementary metal oxide semiconductor
COB	chip-on-board

COTS	commercial-off-the shelf
CPU	central processing unit
CQFP	ceramic quad flat pack
CSP	chip scale package
CTE	coefficient of thermal expansion
DIL	dual in line
DFN	dual flat no-lead (package)
DMD	digital micromirror devices
DOE	design of experiment
DRIE	deep reactive ion etching
DRQFN	dual-row quad flat no-lead
EMIB	embedded multi-die interconnect bridge
EDA	electronic design automation
EMS	electronics manufacturing services
ESL	equivalent series inductance
eWLB	embedded wafer level ball grid array
FCBGA	flip-chip ball grid array
FCOB	flip chip on board
FC	flip-chip
FCBGA	flip-chip ball grid array
FCIP	flip-chip in package
FCOB	flip chip on board
FLI	first level interconnect
FOWLP	fan-out wafer level package
FPBGA	fine pitch ball grid array
GPU	graphics processing unit
HBM	high bandwidth memory
HDTV	high definition television
HVM	high volume manufacturing
IC	integrated circuit
I/O	input/output
IoT	internet of things
IEEE	Institute of Electrical and Electronics Engineers
IGBT	insulated gate bipolar transistor [?]
iNEMI	international electronics manufacturing initiative
IPC	(association connecting electronics industries)
IPD	integrated passive devices
ITRS	International Technology Research Society
JIC	JISSO international council
JISSO	Japanese acronym for a total solution for interconnecting, assembling, packaging, mounting, and integrating system design
JPL	Jet Propulsion Laboratory
KGD	known good die
LCC	leadless chip carrier
LCP	liquid crystal polymer
LED	light emitting diode
LGA	land grid array

MBD	micro-bumped die
MCP	multi-chip package
MEMS	micro-electro-mechanical systems
MLF	micro lead frame
MOEM	micro-opto-mechanical systems
MOSFET	metal oxide field effect transistor
MPP	multi package on PCB
MRQFN	multi-row quad flat no-lead
MST	microsystems technology
MtM	more than Moore
NASA	National Aeronautics and Space Administration
NEPP	NASA Electronic Parts Program
ODM	original design manufacturer
OE-A	organic electronics association
OEM	original equipment manufacturer
OLED	organic light emitting diode
OPV	organic photovoltaic
OTFT	organic thin film transistor
PBGA	plastic ball grid array
PCB	printed circuit board
PE/OE	printed electronics/organic electronics
PET	printed electronics technology
PGA	pin grid array
PHM	prognostic health monitoring
PIDTP	package integrity demonstration test plan
PiP	package-in-package
PoP	package-on-package
PuP	package under package
PWB	printed wiring board
QFN	quad flat no-lead
QFP	quad flat pack
QML	qualified manufacturer list
R2R	roll to roll
RCC	resin-coated copper
RDL	redistribution layer
RF	radio frequency
RFID	radio frequency identification
RoHS	(European Union) restriction of hazardous substances
RUL	remaining useful life
SEM	scanning electron microscope
SIA	Semiconductor Industry Association
SiP	system in package
SMD	surface mount device
SMT	surface mount technology
SOC	small outline chip
SSI	stacked silicon interconnect
TFT	thin film transistor

TMV through mold via
TO transistor outline
TPV through-package via
TQFN thin quad flat no-lead
TSH through-silicon hole
TSOP thin small outline package
TSV through silicon via
TWG technology working groups
TV test vehicle
USON ultra-thin-small-outline
VDMA Verband Deutscher Maschinen und Anlagenbau (German engineering federation)
VQFN very thin quad flat no-lead
WCSP wafer level chip scale package
WFOP wide strip fan-out package
WLCSMP wafer-level chip scale module package
WLCSP wafer-level chip-scale packaging
WLP wafer level package

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REFERENCES

[1] *International Technology Roadmap for Semiconductors*, ITRS (web page), http://www.itrs.net/, accessed June, 2013.
[2] *International Electronics Manufacturing Initiatives* (web page), INEMI, http://www.inemi.org/2013-roadmap, accessed June, 2013.
[3] *IPC, Association Connecting Electronics Industry* (web page), http://www.ipc.org, accessed June, 2013.
[4] *OEA, Organic and Printed Electronics Association* (website), http://www.oe-a.org/en_GB/, accessed June, 2013.
[5] R. Ghaffarian, "Update on CGA Packages for Space Applications," *Microelectronics Reliability*, 2016.
[6] R. Ghaffarian, "Reliability of Printed Circuit Boards," Chapter 60 in *Printed Circuit Handbook*, 7th ed., editor-in-chief, Coombs, C. F., McGraw-Hill, New York, 2016.
[7] R. Ghaffarian, "Damage and Failures of CGA/BGA Assemblies under Thermal Cycling and Dynamic Loadings," In Proc. of the ASME 2013 International Mechanical Engineering Congress and Engineering. IMECE2013, November 15-21, San Diego, California.
[8] R. Ghaffarian, "Thermal Cycle and Vibration/Drop Reliability of Area Array Package Assemblies," Chapter 22 in *Structural Dynamics of Electronics and Photonic Systems*, eds. E. Suhir, E. Connally, and D. Steinberg Springer, 2011.

[9] R. Ghaffarian, "Thermal Cycle Reliability and Failure Mechanisms of CCGA and PBGA Assemblies with and without Corner Staking," *IEEE Transactions on Components and Packaging Technologies*, vol. 31, issue 2, June 2008.
[10] R. Ghaffarian, "Area Array Technology for High Reliability Applications," Chapter 16 in *Micro-and Opto-Electronic Materials and Structures: Physics, Mechanics, Design, Reliability, Packaging*, ed. E. Suhir, Springer, 2006.
[11] R. Ghaffarian, "BGA Assembly Reliability," Chapter 20 in *Area Array Packaging Handbook*, ed. K. Gilleo, McGraw-Hill, 2002.
[12] J. Fjelstad, R. Ghaffarian, and Y. G. Kim, *Chip Scale Packaging for Modern Electronics*, Electrochemical Publications, 2003
[13] S. Agarwal, "Class Y, a New Class of Space Microcircuits," *NASA EEE Parts Bulletin*, vol. 5, Issue 4, August/December 2013, (web page), https://sma.nasa.gov/documents/default-source/defaultFileLibrary/newsfeed-eee-partsbulletin-augdec2013.pdf?sfvrsn=0
[14] J.H. Lau, "Patent Issues of Fan-Out Wafer/Panel-Level Packaging," Chip Scale Review, Nov-Dec 2015
[15] "Amkor Technology, QFN (MLF) Package Design Kits for Agilent ADS," (web page), Amkor Technology, (web page) http://www.amkor.com/go/customer-center/qfn-mlf-package-design-kits-for-agilent-ads
[16] A. Tseng, M. Lin, B. Hu, J.W. Chen, J. M. Wan, S. Lee, Y.-S. Lai, "Advanced QFN Surface Mount Application Notes Development," In Proc. of the 12th Electronics Packaging Technology Conference (EPTC), 2010.
[17] C. Zwenger, L. Smith, and J.S. Kim, "Next Generation Package-on-Package (PoP) Platform with Through Mold Via (TMV™) Interconnection Technology," Originally published in the proceedings of the IMAPS Device Packaging Conference, Scottsdale, AZ, March 10–12, 2009 file:///C:/Users/rghaffar/Downloads/AmkorTMVPoPpaperIMAPSDPC2009.pdf, Accessed 11/5/14
[18] K. Saban, "Xilinx Stacked Silicon Interconnect Technology Delivers Breakthrough FPGA Capacity, Bandwidth, and Power," (web page), Xilinx, http://www.xilinx.com/support/documentation/white_papers/wp380_Stacked_Silicon_Interconnect_Technology.pdf, Accessed 11-5-14
[19] J. Casey, "System Scaling Technologies and Opportunities for Future IT Workloads and Systems," Solid State Technology Network, (web page) http://semimd.com/insights-from-leading-edge/2014/03/03/iftle-182-ieee-iss-2014-ibm-linx-imec-ihs-ibs/, accessed, Nov., 2014.
[20] R. Huemoeller, "Advances in Interposer Assembly," Solid State Technology (web page), http://electroiq.com/insights-from-leading-edge/2014/02/gatech-interposer-conf-amkor-globalfoundries/.
[21] C. G. Woychik, A. Agrawal, R. A. Zhang, R. Latorre, B. S. Lee, L. Mirkarimi, and S. Arkalgud, "Scalable Approaches For 2.5d IC Assembly", In Proc. of the Surface Mount Technology International Conference Proceedings, 2014.
[22] J. H. Lau, "3D IC Integration and Packaging," *McGraw Hill Professional*, 2015.
[23] J. H. Lau, C. Hsinchu, "3D IC Integration with a TSV/RDL Passive Interposer", In Proc. of the Surface Mount Technology International Conference, 2014.
[24] T. Mobley, S. Cardona, "2.5D and 3D Packaging Platform for Next Generation RF and Digital Modules Using Through Glass Vias (TGV) Technology," In Proc. of the IEEE Component and Technology Conference, 2014.
[25] A. Shorey, P. Cochet, A. Huffman, J. Keech, M. Lueck, S. Pollard, and K. Ruhmer, "Advancements in Fabrication of Glass Interposers," 2014.
[26] J. Tong, Y. Sato, S. Takahashi, N. Imajyo, A. F. Peterson, V. Sundaram, and R. Tummala, "High-Frequency Characterization of Through Package Vias Formed by Focused Electrical-Discharge in Thin Glass Interposers", In Proc. of the ECTC 2014.
[27] Intel news release, (web page), https://newsroom.intel.com/news-releases/intel-announces-new-packaging-and-test-technologies-for-foundry-customers/, accessed Mar, 2016
[28] K. Banerjee, S. Souri, P. Kapur, and K. Saraswat, "3-D les: A Novel Chip Design for Improving Deep-Submicrometer Interconnect Performance and Systems-on-Chip Integration," *IEEE Proceedings*, vol. 89, no. 5, 2001.
[29] A. Rahman and F. R. Reif, "Comparison of Key Performance Metrics in Two and Three Dimensional Integrated Circuits," In Proc. of the IEEE International Interconnect Technology Conference, pp. 18-20, 2000.
[30] S. Das, A. Chandrakasan, and R. Rei£, "Timing, Energy and Thermal Performance of Three Dimensional Integrated Circuits*,"* In Proc. of the Great Lakes Symposium on VLS, pp. 338–343, 2004.
[31] H. P. Hofstee, "Future Microprocessors and Off-chip SOP Interconnect," *IEEE Transactions Advanced Packaging*, vol. 27, no. 2, pp. 301–303, May 2004.

[32] A. Rahman, S. Das, A. Chandrakasan, and R. Rei£, "Wiring Requirement and Three-Dimensional Integration Technology for Field Programmable Gate Arrays," *IEEE Transactions VLSI*, vol. 11, no. 1, pp. 44–54, February 2003.
[33] J. Vardaman, "3-D Through-Silicon Vias Become a Reality," *Semiconductor International*, pp. 37–40, June 2007.
[34] P. E. Garrou, E. J. Vardaman, and P. D. Franzon, "Through Silicon Via Technology: The Ultimate Market for 3D Interconnect," *Tech Search International*, January 2008.
[35] F. Von Trapp, "Are There Still Gaps in 3D Readiness" (web page), *3DInCites*, (web page), http://www.3dincites.com/2014/08/gaps-in-3d-ic-readiness/, accessed November 14, 2014.
[36] IPD- Integrated Passive Devices- a Chip Scale Module Package Technology, (web page) http://www.statschippac.com/~/media/Files/Package%20Datasheets/CSMP.ashx, Accessed November 14, 2014.
[37] V. Solberg, "Embedded Passive Technology Materials, Design and Process," In Proc. of the Surface Mount Technology Association Proceedings, 2014.
[38] L. Del Catillo, A. Moussessian, M. Mojarradi, E. Kolawa, R. W. Johnson, and B. Blalock, "Advanced Embedded Active Assemblies for Extreme Space Applications," Jet Propulsion Laboratory, California Institute of Technology, Pasadena, CA, (web page), http://trs-new.jpl.nasa.gov/dspace/bitstream/2014/41385/1/09-0330.pdf.
[39] N. Hayashi, H. Mahicda, N. Shintani, N. Masuda, K. Hashimoto, A. Furuno, K. Yoshimitsu, Y. Kikuchi, and Y. Hiruta, "A New Embedded Structure Package For Next Generation, WFOTM (Wide Strip Fan-Out Package," Pan Pacific Symposium Proceedings, Surface Mount Technology Association, 2014, (web page), http://www.smta.org/
[40] L. Boettcher, S. Karaszkiewicz, D. Manessis and A. Ostmann, "Development of Embedded Power Electronics Modules for Automotive Applications," In Proc. of the Surface Mount Technology Association, 2012.
[41] H. Stahr and M. Beessley, "Embedded Components on the way to Industrialization," In Proc. of the Surface Mount Technology Association, 2011.
[42] J. Vardaman, K. Carpenter, "Embedded Components, Why Now?," Surface Mount Technology Association Proceedings, Luncheon speaker, 2014, (web page), http://www.smta.org/.
[43] R. Ramesham, R. Ghaffarian, "Challenges in interconnection and packaging of microelectromechanical systems (MEMS)," In Proc. of the 50th IEEE Electronic Components & Technology Conference, 2000, pp. 666-675.
[44] R. Ghaffarian, D.G. Sutton, P. Chafee, N. Marquez, A. K. Sharma, A. Teverovski, "Thermal and Mechanical Reliability of Five COTS MEMS Accelerometers," NASA Electronic Parts and Packaging Program, http://nepp. nasa. gov/eeelinks/February2002/Thermal_and_Mechanical_Reliability. Pdf, 2002 Feb.
[45] R. Ramesham, R. Ghaffarian, N. P. Kim, "Reliability issues of COTS MEMS for Aerospace Applications," In Proc. of the Symposium on Micromachining and Microfabrication, 1999, Aug. 18, pp. 83-88.
[46] Garrou, P., Insights From Leading Edge, Solid State Technology, (web page) http://electroiq.com/insights-from-leading-edge/, accessed Mar., 2016
[47] Jisso International Council, (web page), http://home.jeita.or.jp/jisso2/english/committee/index.html, accessed, Oct., 2015.
[48] J. Fjelstad, "The Electronic Interconnection Hierarchy," *Global SMT & Packaging*, (web page), http://www.globalsmt.net/smt/index.php?option=com_content&view=article&id=10890&Itemid=413, accessed June 29, 2013.
[49] J. W. Evans, J. Y. Evans, R. Ghaffarian, A. Mawer, K. Lee, C. Shin, "Simulation of Fatigue Distributions for Ball Grid Arrays by the Monte Carlo Method," *Microelectronics Reliability*, vol. 40, no. 7, pp. 1147-55, 2000.
[50] H. Oh, H. P. Wei, B. Han, and B. D. Youn, "Probabilistic Lifetime Prediction of Electronic Packages Using Advanced Uncertainty Propagation Analysis and Model Calibration," *IEEE Transactions on Components, Packaging And Manufacturing Technology*, vol. 6, no. 2, February 2016.
[51] M. Pecht, "Prognostics and Health Management of Electronics," *Wiley-Interscience, New York*, NY, 2008.
[52] S. Mathew, M. Osterman, and M. Pecht, "Considerations in implementing canary based prognostics", In Proc. of the IEEE Conference Prognostics and Health Management (PHM), June 2015, pp. 1-7. IEEE.
[53] C. Hendricks, E. George, M. Osterman, M. Pecht, "3 Physics-of-Failure (PoF) Methodology for Electronic," *Reliability Characterisation of Electrical and Electronic Systems*, pp. 24-27, 2014.

[54] P. Lall, R. Lowe, K. Goebel, K., "Prognostic Health Monitoring for a Micro-Coil Spring Interconnect Subjected To Drop Impacts," In Proc. of the IEEE Prognostics and Health Management (PHM) Conference, 2014, pp. 1-11.
[55] P. Lall, S. Deshpande, L. Nguyen, M. Murtuza, "Prognostic Indicators for Cu-Al Wirebond Degradation under Operation at Elevated Temperature and Combined Temperature Humidity," In Proc. of the IEEE Prognostics and Health Management (PHM) Conference, 2014, pp. 1-13.
[56] P. James, J. Hofmeister, B. Judkins, D. Goodman, "A Low-Power Sensor Design, SJ Monitor, for Monitoring 24x7 the Health of BGA Solder Joints," (web page) http://www.microsemi.com/document-portal/doc_view/131711-a-low-power-sensor-design-sj-monitor, Accessed 3/10/16
[57] D. An, N. H. Kim, J. H. Choi, "Practical Options For Selecting Data-Driven or Physics-Based Prognostics Algorithms with Reviews," *Reliability Engineering & System Safety*, vol. 133, pp. 223-36, 2015.
[58] E. Suhir, "Three-Step Concept (TSC) In Modeling Microelectronics Reliability (MR): Boltzmann–Arrhenius–Zhurkov (BAZ) Probabilistic Physics-Of-Failure Equation Sandwiched between Two Statistical Models," *Microelectronics Reliability*, vol. 54, pp. 2594-2603, 2014.
[59] S. Kartalopoulos, *Understanding Neural Networks and Fuzzy Logic*, IEEE Press, 1997
[60] T. A. Doug, A. R. Stubberud, "Convergence Analysis of Cascade Error Projection-An Efficient Learning Algorithm for Hardware Implementation," *International Journal of Neural Systems*, vol. 10, no. 3, pp. 199-210, June 2000.
[61] A. M. Deshpande, G. Subbarayan, D. Rose,"A System for First Order Reliability Estimation of Solder Joint Area Array Packages," *Transaction of the ASME*, vol. 122, pp. 6-13, 2000.
[62] R. Darveaux, K. Banerji, A. Mawer, and G. Dody, 1995. Reliability of plastic ball grid array assembly. Ball grid array technology, pp. 379-442.
[63] R. Ghaffarian, "Accelerated Thermal Cycling and Failure Mechanisms for BGA and CSP Assemblies," *J. Electron. Packag*, vol. 122, no. 4, pp. 335-340, 2000.
[64] CBGA Assembly and Rework, IBM User's Guideline (May 23, 2002)