FACTA UNIVERSITATIS
Series: **Electronics and Energetics** Vol. 27, N^o 2, June 2014, pp. 259 - 273
DOI: 10.2298/FUEE1402259N

PHYSICAL MODELING OF ELECTRICAL AND DIELECTRIC PROPERTIES OF HIGH-*k* Ta_2O_5 BASED MOS CAPACITORS ON SILICON

Nenad Novkovski

Institute of Physics, Faculty of Natural Sciences and Mathematics,
University "Ss. Cyril and Methodius", Arhimedova 3, 1000 Skopje, Macedonia

Abstract. *In this paper we present an integral physical model for describing electrical and dielectric properties of MOS structures containing dielectric stack composed of a high-k dielectric (with emphasize on pure and doped Ta_2O_5) and an interfacial silicon dioxide or silicon oxynitride layer. Based on the model, an equivalent circuit of the structure is proposed. Validity of the model was demonstrated for structures containing different metal gates (Al, Au, Pt, W, TiN, Mo) and different Ta_2O_5 based high-k dielectrics, grown of bare or nitrided silicon substrates.*
The model describes very well the I-V characteristics of the considered structures, as well as frequency dependence of the capacitance in accumulation. Stress-induced leakage currents are also effectively analyzed by the use of the model.

Key words: *high-k dielectrics, metal-insulator-silicon structures, conduction mechanisms in dielectrics, leakage currents*

1. INTRODUCTION

Further scaling of microelectronic devices required for new generations of integrated circuits is confronting multiple challenges, rather important one of them being the fabrication of ultrathin dielectric layers used particularly in MOSFETs and DRAMs. While decreasing the lateral size of devices, in order to obtain the required capacitance, a decrease of the equivalent oxide thickness is required. The above requirement can be met either by decreasing the physical thickness or by increasing the permittivity of the dielectric (gate oxide for MOSFETS, dielectric in MOS capacitors of DRAMs).

Doped, mixed and laminate high-permittivity (high-*k*) dielectric stacks attract progressively higher attention as a solution for further improvement of their electrical and dielectric properties [1]-[13]. It has been shown that Ta_2O_5, known as one of the most attractive dielectrics for the nanoscale dynamic random-access memories, can improve

Received February 5, 2014
Corresponding author: Nenad Novkovski
Institute of Physics, Faculty of Natural Sciences and Mathematics, University "Ss. Cyril and Methodius", Arhimedova 3, 1000 Skopje, Macedonia
(e-mail: nenad@iunona.pmf.ukim.edu.mk)

further by doping with convenient elements [14]. Detailed studies of the properties of tantalum pentoxide doped with Al, Ti and Hf and mixed with HfO_2 have been reported [15]-[30]. In addition, it has been shown that the nitridation of the Si substrate improves substantially electrical, dielectric and reliability properties of metal-high-*k*-Si structures [31].

In [32] we described in detail a comprehensive model for the I-V characteristics of metal-Ta_2O_5/SiO_2-Si structures. In this work we present integrally the generalization of the comprehensive model for MIS structures containing dielectric stack composed of a high-*k* dielectric (particularly pure and doped Ta_2O_5) and an interfacial silicon dioxide or silicon oxynitride layer and review the important results obtained with using specific cases of this model for various MOS structures of the considered type.

2. THEORETICAL MODEL

2.1. Band diagram

Band diagram of the considered structure in the case of Al gate is shown in fig. 1.

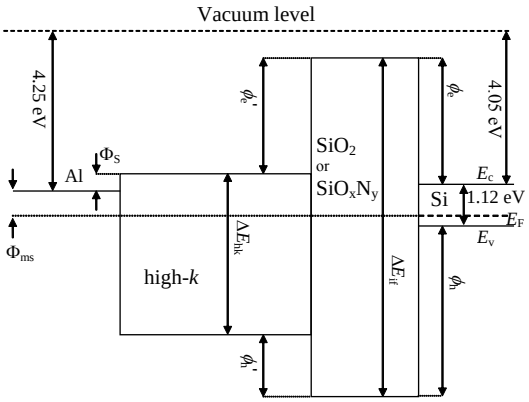

Fig. 1 Band diagram of the considered structure

In Fig. 1 ΔE_{hk} and ΔE_{if} are the bandgaps of the high-*k* and the interfacial layer, respectively. ϕ_e' and ϕ_h' are band offsets for electrons and holes, respectively, at the contact between the high-k and the interfacial layer, while ϕ_e and ϕ_h are band offsets for electrons and holes, respectively, at the contact between the interfacial layer and the silicon substrate. Φ_{ms} is the work function difference between the metal gate and Si, while Φ_S is the Shottky barrier height for electrons. In the case of Al gate, Ta_2O_5 high-*k* dielectric and SiO_2 interfacial layer the values are those summarized in Table 1. Work function difference, Φ_{ms}, depends on the Si substrate doping and is the same as in the case of the corresponding metal-SiO_2-Si structure. For p-type substrates it is around 0.5 eV.

Table 1 Values of bandgaps and band offsets for Al-Ta_2O_5/SiO_2-Si structures

ΔE_{hk} (eV)	ΔE_{if} (eV)	ϕ_e (eV)	ϕ_h (eV)	ϕ_e' (eV)	ϕ_h' (eV)	Φ_S (eV)
8.97	4.4	3.15	4.97	3.06	1.51	0.29

2.2. Conduction mechanisms

The conduction mechanisms that have to be considered in general case for the interfacial layer are:

- Hopping conduction, which is a result of the quantum diffusion of electrons between the localized states in the insulator, typical of disordered materials. This is a bulk-limited conduction mechanism, and hence it does not depend on the gate voltage polarity. Since the current density in this case is a linear function of the electric filed, we can consider it as a conductivity of ohmic type.
- The trap-assisted inelastic tunneling [33]-[34]. Electrons tunnel from the silicon to the traps in the SiO_2 layer. As the SiO_2 is an amorphous material with low trap density it is expected to observe this effect only in the films where the traps are created as a result of a stress, radiation or process induced damage. In the case of an SiO_xN_y interfacial layer significantly higher density of traps is to be expected. However, this density is still very low compared to typically high density materials.
- Direct tunneling (trough a trapezoidal barrier) and Fowler-Nordheim injection (trough a triangular barrier) into interfacial layer. Tunneling current can be created by the electrons or the holes from the Si substrate. The barrier for the tunneling of the holes is different from that for the electrons, thus a remarkable asymmetry can be observed between the opposite polarities.

A particular mechanism involving both SiO_xN_y and high-*k* is the tunneling through double barrier (through a trapezoidal barrier in SiO_2 and a triangular barrier in high-*k*).

The conduction mechanisms that have to be considered for the high-k dielectric are:

- Poole-Frenkel mechanism, which is bulk-limited, and hence independent on the gate bias polarity. Electrons are exited to the conduction band from the traps by field-enhanced thermal emission and they drift trough the layer. Because of the high defect density, they are easily trapped by other positively charged defects. New electrons are released from other traps, thus transporting the charge step by step from one surface of the film to the opposite (Fig. 2). When the gate is negative, electron needs first to enter the insulator from the metal gate. It is to be noted that they do not need to obtain enough energy to enter the conduction band, but just to move to a defect-related state in the vicinity of the metal surface. The activation energies of the defects responsible for the Poole-Frenkel emission in the Ta_2O_5 are 0.2 eV (type A, [35]) and 0.8 eV (type D, must probably the first ionization level of the double-donor oxygen vacancy, [36]). They are close to or lower than the metal-gate Fermi level (0.29 eV under the conduction band of Ta_2O_5. We estimated the tunneling probability from the Al-gate to the neighboring traps to be so high that extremely high current densities of order of 100 A/cm^2 can be attained for a voltage drop of only few mV.
- Shottky emission, which is an electrode-limited effect. Schottky conduction is excluded for gate positively biased, because the side of the high-*k* layer near the negative electrode is not in direct contact with a metal or semiconductor. For the gate negatively biased, the barrier is low (for Ta_2O_5 only 0.29 eV), and hence the Schottky emission is to be expected. However, it is not expected to be a current-limiting mechanism, because thus injected electrons are quickly trapped in the the high-*k* layer near the contact with the metal, continuing the transport by the Poole-

Frenkel emission from the traps. Namely, the pure Schottky effect occurs when electrons are injected from the metal in vacuum. The situation is similar when they are injected in a medium where they can almost freely traverse the distance from the injecting to the opposite electrode, as is the case with the ultra-thin SiO_2 or SiO_xN_y if the defect density is fairly low. For metals with higher absolute values of the work functions this issue requires further consideration. We observed a particular effect of charge trapping at the interface between the metal gate and the high-k dielectric for Au and Pt [37]-[39]. Although the Schottky emission from the metal to the high-*k* conduction band is practically impossible, an emission to the traps can substantially influence the leakage currents. For example, in the case of Ta_2O_5 and a Pt electrode, the Fermi level in the metal is about 0.6 eV lower than the trapping level of the D type defect. In that case the filling of the traps D type can occur by thermal emission from the metal, leading to a Schottky-like effect at low applied voltages, as it was observed on Au-Ta_2O_5-Pt-Si structures at Pt electrode negatively biased [40]. This issue requires deeper investigation in a separate study on metal-insulator-metal structures. One of the possible approaches to this problem will be to use the multi-step trap-assisted tunneling model, as it was done in [41] for the metal-Al_2O_3-Si structures.

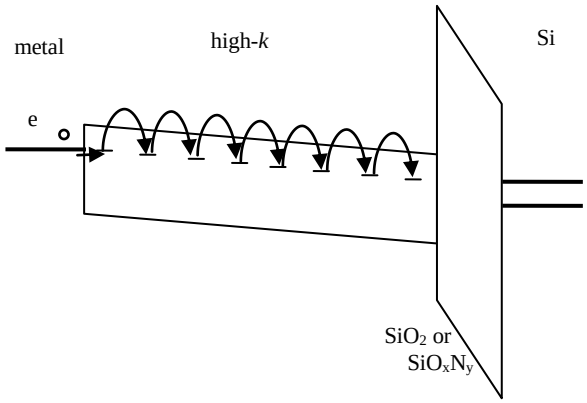

Fig. 2 Illustration of the Poole-Frenkel conduction mechanism

- The hoping conduction in the Ta_2O_5 layer is of much lower importance because the Poole-Frenkel mechanism gives already much higher conductivity in Ta_2O_5 then the hopping conductivity in SiO_2. Specifically, when Ta_2O_5 is polycrystalline, as is the case with the films studied here [42], the hopping conductivity is very weak, while the trap density (related to oxygen vacancies, grain boundaries etc.) becomes extremely high. Therefore, it is reasonable to neglect the hopping conductivity.

2.2. Differences between the cases of positive and negative gate

In the case of the gate positively biased, the electrons that tunnel through the SiO_2 barrier enter the Ta_2O_5 conduction band. They drift for a small distance, then they become trapped, but some new electrons are subsequently emitted from the traps and continue the transport, step by step, until entering the metal (Fig. 3).

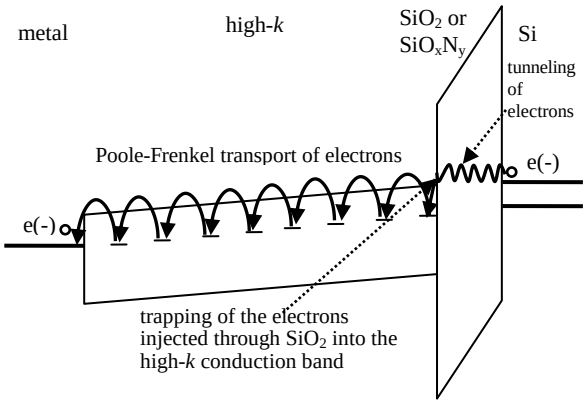

Fig. 3 Conduction mechanisms ate positive gate

In the case of the gate negatively biased, some electrons from the traps near the Ta_2O_5/SiO_2 interface can move to the localized states in the SiO_2 layer, then by quantum diffusion to contribute to the hopping conduction. Tunneling of electrons through the SiO_2 layer from the Ta_2O_5 layer and of holes from the Si substrate could occur. The usual assumption that the electron current gives the dominant contribution in this case is not valid, because the Fowler-Nordheim and direct tunneling are possible where an electron gas from the metal of semiconductor is in contact with an SiO_2 surface [43]. There, the dominant part of the electrons moving towards this surface are reflected, while a small part tunnels through the SiO_2 layer entering the opposite electrode (direct tunneling) or a part of it entering its conduction zone (Fowler-Nordheim tunneling). In the case of an insulator, the density of the electrons in the conduction zone is practically zero and the electron tunneling is practically impossible. Therefore only the holes from the substrate contribute to the tunneling current [44]. For enough high fields, the holes injected from the Si substrate enter the valence band of the Ta_2O_5 layer. Because of the high trap density, after passing a small distance, they recombine with the electrons on the traps. Special attention has to be devoted to the case of lower fields, where the holes can not tunnel to the valence band (Fig. 4). By other authors [45] an attempt was made to describe a similar situation by the double barrier tunneling.

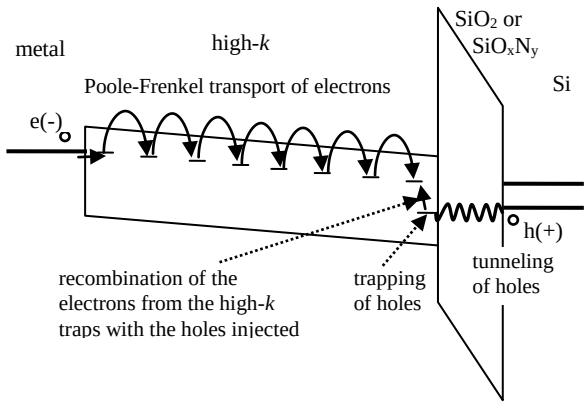

Fig. 4 Conduction mechanisms ate negative gate

Our estimations in connection with the proposed comprehensive model showed feeble agreement with the experimental results if a double barrier tunneling mechanism is invoked. The reason is that the dominant conduction mechanism for the Ta_2O_5 layer is the Poole-Frenkel and not the tunneling. Once the charge carriers enter the forbidden gap of the tantalum pentoxide, they become trapped after a short distance, because the defect related trap density there is extremely high. Tunneling is typical of the SiO_2 films and is observed in Si_3N_4 films with very high quality, where the defect density is low and the injected charge carriers can pass long distances (of order of 100 nm) with a small probability to be trapped. In some cases (SiO_2 thinner than 4 nm) even a ballistic transport is observed [46]. The most probable route of the electrons injected into the Ta_2O_5 forbidden gap is to be first trapped near the Ta_2O_5/SiO_xN_y interface and then to recombine with electrons from other traps or from the conduction band (Fig. 4). A similar situation can also appear in the case of low fields for the opposite gate polarity.

2.3. Construction of the model

The expressions for the current density due to the hopping conductivity in SiO_2 (J_{hc}) is described by the following expression:

$$J_{hc} = \sigma_{if} E_{if} \tag{1}$$

where σ_{if} is the temperature dependant hopping conductivity and E_{if} is the filed in the interfacial layer.

Direct tunneling current density through the interfacial layer (J_{td}) is given by the following expression:

$$J_{td} = \frac{q^2}{8\pi h\phi} E_{if}^2 \exp\left(-\frac{8\pi\sqrt{2m^* q\phi^3}}{3hE_{if}} \left(1 - \left(1 - \frac{d_{if}}{\phi} E_{if} \right)^{\frac{3}{2}} \right) \right) \tag{2}$$

and for the Fowler-Nordheim injection with (J_{FN})

$$J_{FN} = \frac{q^2}{8\pi h\phi} E_{if}^2 \exp\left(-\frac{8\pi\sqrt{2m^* q\phi^3}}{3hE_{if}} \right), \tag{3}$$

where q is the electron charge, h is the Planck's constant, m^* is the effective tunneling mass of charge carriers injected through the interfacial layer, d_{if} is the thickness of the interfacial layer, ϕ is the tunneling barrier height and E_{if} is the electric field in it.

The total current density flowing through the interfacial layer (J_{if}) is given by the following expression:

$$J_{if} = J_{hc} + \begin{cases} J_{td} & E_{if} \le \phi / d_{if} \\ J_{FN} & E_{if} \ge \phi / d_{if} \end{cases}, \tag{4}$$

and the voltage drop on the interfacial layer (E_{if}) is

$$V_{if} = d_{if} E_{if} . \tag{5}$$

The current density due to the Poole-Frenkel effect in the high-*k* layer (J_{PF}) is described by the following expression:

$$J_{PF} = \sigma_{hk}(0) E_{hk} \exp\left(\frac{1}{rkT} \sqrt{\frac{q^3}{\pi \varepsilon_0 K_T}} \sqrt{E_{hk}} \right), \tag{6}$$

where $\sigma_{hk}(0)$ is a temperature dependent defect related constant having dimensions of conductivity, r is the degree of compensation [47], k is the Boltzmann constant, ε_0 is the dielectric permittivity in vacuum, K_T is the optical frequency dielectric constant of the high-*k* dielectric and E_{hk} is the electric filed in it.

The voltage drop on the layer (V_{hk}) is given by:

$$V_{hk} = d_{hk} E_{hk}, \tag{7}$$

where d_{hk} is the thickness of the high-*k* dielectric layer.

The numerical procedure consists in simultaneous computation of the two following quantities: the oxide voltage:

$$V_{ox} = V_{hk} + V_{if} = d_{hk} E_{hk} + d_{if} E_{if} \tag{8}$$

and the current density in steady state (Kirchhoff's laws)

$$J = J_{PF} = J_{if}. \tag{9}$$

First the current density $J = J_{if}$ was determined for a given field E_{if} in the interfacial layer. Then the field in the high-*k* layer was computed as an inverse function of the current density $J_{hk} = J$. At the end, the oxide voltage was calculated with the use of the expression (8).

We intend to use minimum of fitting parameters. The defect density parameter for high-*k* layer was first chosen because it is dependent on the technological parameters and is difficult to be determined by independent methods. Silicon dioxide layer thickness was also treated as a fitting parameter in a restricted range (2 to 3 nm) close to the measured value, because the small variations in it cause substantial variations in the result. Later, these results were compared with independent measurements. The hoping conductivity was also treated as a fitting parameter, since there are no available data from independent experiments. Because the different mechanisms do not exclude each other, they are considered in a single form for the entire measurement region; as we discussed in [48], this approach is unavoidable in the case of nano-layered dielectrics where the effects of contributions of different conduction mechanisms can not be separated but standard methods a single assuming dominant conduction mechanism in a given voltage range.

In the case of Al-Ta_2O_5/SiO_2-Si structures following typical values can be taken from the literature: tunneling electron mass in ultrathin SiO_2, $m_e^* = 0.61\ m_e$ [49], where m_e denotes the mass of free electron; tunneling hole mass in SiO_2, $m_h^* = 0.51\ m_e$; optical frequency dielectric constant of Ta_2O_5, $K_T = n^2 = 2.1^2 = 4.4$; tunneling barrier height for of holes in SiO_2; $\phi_h = 4.70$ eV [49]; tunneling barrier height for of electrons in SiO_2, $\phi_e = 3.15$ eV [50]; and compensation factor, $r = 1$ (we consider the Poole-Frenkel effect without compensation).

Voltage on the stacked insulating layer (V_{ox}) can be calculated by using relations involving the flatband voltage (V_{fb}) and the voltage drop in the semiconductor (V_s):

$$V_{ox} = V_g - V_{fb} - V_s \,. \tag{10}$$

The value of the V_{fb} was determined with the standard method which is not described here. A low value of the fixed charge density in the SiO_2 was assumed, i.e. the ideal value of the flatband voltage (V_{fb}^{id}) was used. This assumption will be discussed later, though it can be simply treated as an approximation that holds for insulating films of high quality, where the oxide charge density is fairly low.

The voltage drop in Si (V_s) is connected with the electric field strength in the interfacial layer (E_{if}) by the following expression:

$$E_{if} = \pm \frac{\varepsilon_{Si}}{\varepsilon_{if}} \begin{cases} \sqrt{\dfrac{2kTp_0}{\varepsilon_{Si}} \left[\left(e^{-\frac{qV_s}{kT}} + \dfrac{qV_s}{kT} - 1 \right) + \dfrac{n_i^2}{p_0^2} \left(e^{\frac{qV_s}{kT}} - \dfrac{qV_s}{kT} - 1 \right) \right]} & \mathrm{p-type\,Si} \\ \sqrt{\dfrac{2kTn_0}{\varepsilon_{Si}} \left[\dfrac{n_i^2}{n_0^2} \left(e^{-\frac{qV_s}{kT}} + \dfrac{qV_s}{kT} - 1 \right) + \left(e^{\frac{qV_s}{kT}} - \dfrac{qV_s}{kT} - 1 \right) \right]} & \mathrm{n-type\,Si} \end{cases} . \tag{11}$$

where ε_{Si} is the relative permittivity of Silicon, ε_{if} is the relative permittivity of the interfacial layer, n_0 is the density of electrons in n-type silicon, p_0 is the majority carrier density in p-type silicon and n_i is the intrinsic carrier density in silicon.

In strong inversion (positive gate for p-type substrate, negative gate for n-type substrate) the leakage current density reaches an almost saturated value of the order of magnitude 1 mA/cm^2. This saturation is due to the exhaustion of the minority carriers in the substrate, due to the minority carrier extraction from the substrate (electrons for p-type and holes for n-type). Namely, the maximum tunneling current density of the electrons from the substrate is limited by the thermal generation rate of electrons in the inversion region of Si, similarly to the case of the diode reverse current. The values observed in our experiment are comparable to the values obtained for p-n Si diode reverse currents for the voltages between 1 V and 10 V.

2.3. Equivalent circuit

Combining above described model with the standard description of MIS structures [51], a complete equivalent circuit of the considered structure can be constructed (Fig. 5). Diode (D) that is shown at the left end of the figure accounts for the effect of exhaustion of minority carrier in strong accumulation, as described above. Diode orientation shown in the figure corresponds to an n-type substrate; for the case of p-type Si substrate the orientation is reversed.

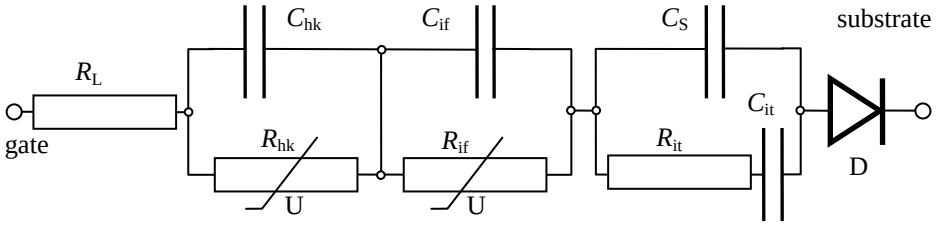

Fig. 5 Equivalent circuit of the considered structure

Meanings of the symbols for physical quantities in Fig. 5 are as follows:
R_L – serial resistance,
R_{hk} – voltage dependent resistance of the high-*k* layer,
R_{if} – voltage dependent resistance of the interfacial layer,
R_{it} – interface traps resistance,
C_{hk} – capacitance of the high-*k* layer,
C_{if} – capacitance of the interfacial layer and
C_{it} – interface traps capacitance.

Capacitances of the layers of the dielectric stack are given by following expressions:

$$C_{hk} = \varepsilon_{hk}\varepsilon_0 \frac{A}{d_{hk}} \tag{12}$$

and

$$C_{if} = \varepsilon_{if}\varepsilon_0 \frac{A}{d_{if}}, \tag{13}$$

where ε_{hk} is the the relative permittivity of high-*k* layer and A is the electrode area of the capacitor.

R_L, R_{it}, C_{if} and C_{it} are to be extracted from the *C-G-V* curves at various frequencies, while R_{hk} and R_{if} from *I-V* curves while using here described model. R_{hk} and R_{if} are both voltage dependent.

3. RESULTS

3.1. I-V curves

First we discuss the values of the parameters obtained from the fitting of the theoretical to the experimental curve that can be obtained by independent methods. This is the case with the interfacial layer thickness (d_{if}) and the band offsets (ϕ_e and ϕ_h) at the contact between Si and SiO_2. For ϕ_e and ϕ_h values close to the literature data, 3.15 eV and 4.70 eV, respectively, have been obtained [44]. In [44], fitted value d_{if} = 2.8 nm was obtained, close to the value of 2.6 nm measured by transmission electron microscopy.

Some of the results obtained from applying the model on the experimental results for *I-V* curves different for Al-high-*k*/SiO_xN_y-Si structures are displayed in Table 2. Several

important features of the structures are clearly identified by the values of the important parameters.

Table 2 Values of fitting parameters for Al-high-k/SiOxNy-Si structures

r.f. sputtered Ta_2O_5 on bare Si at substrate temperature 493 K (unpublished data)						
annealed	d_{if} (nm)	d_{hk} (nm)	ϕ_e (eV)	ϕ_h (eV)	σ_{hc} ($\Omega^{-1}cm^{-1}$)	$\sigma_{hk}(0)$ ($\Omega^{-1}cm^{-1}$)
not	2.90	27	2.50	3.30	1×10^{-16}	3.95×10^{-17}
at 893 K	2.95	27	3.05	3.40	1×10^{-16}	3.95×10^{-15}
at 1193 K	2.97	26	3.15	4.70	1×10^{-16}	1.98×10^{-12}
Ta_2O_5 obtained by thermal oxidation of Ta in pure O_2 at 873 K on bare Si [44]						
gate	d_{if} (nm)	d_{hk} (nm)	ϕ_e (eV)	ϕ_h (eV)	σ_{hc} ($\Omega^{-1}cm^{-1}$)	$\sigma_{hk}(0)$ ($\Omega^{-1}cm^{-1}$)
Al	2.78	47	3.15	4.70	8.1×10^{-17}	8.2×10^{-11}
Au	2.72	47	3.15	4.70	8.1×10^{-17}	6.6×10^{-14}
W	2.80	47	3.15	4.70	8.1×10^{-17}	1.7×10^{-13}
r.f sputtered Ta_2O_5 at 493 K on Si nitrided in nitrous oxide at temperatures T_{on} [52]						
T_{on} (K)	d_{if} (nm)	d_{hk} (nm)	ϕ_e (eV)	ϕ_h (eV)	σ_{hc} ($\Omega^{-1}cm^{-1}$)	$\sigma_{hk}(0)$ ($\Omega^{-1}cm^{-1}$)
973	2.65	17.3	2.92 eV	3.35 eV	4×10^{-15}	3.3×10^{-8}
1073	2.70	17.3	2.85 eV	3.50 eV	1×10^{-15}	3.3×10^{-8}
1123	2.80	17.2	2.80 eV	3.50 eV	3×10^{-15}	3.3×10^{-8}
r.f sputtered Ta_2O_5 at 493 K on Si nitrided in ammonia at temperatures T_{on} [52]						
T_{on} (K)	d_{if} (nm)	d_{hk} (nm)	ϕ_e (eV)	ϕ_h (eV)	σ_{hc} ($\Omega^{-1}cm^{-1}$)	$\sigma_{hk}(0)$ ($\Omega^{-1}cm^{-1}$)
973	2.70	17.3	2.60 eV	3.30 eV	1×10^{-15}	3.3×10^{-8}
1073	2.80	17.2	2.85 eV	3.25 eV	1×10^{-15}	3.3×10^{-8}
Ta_2O_5 obtained by thermal oxidation of Ta in pure O_2 at 873 K on bare Si [53]						
gate	d_{if} (nm)	d_{hk} (nm)	ϕ_e (eV)	ϕ_h (eV)	σ_{hc} ($\Omega^{-1}cm^{-1}$)	$\sigma_{hk}(0)$ ($\Omega^{-1}cm^{-1}$)
Al	1.84	8.1	3.15	4.4	1×10^{-15}	2×10^{-9}
W	2.04	8.0	3.15	4.7	2×10^{-15}	8×10^{-11}
Au	2.05	8.0	3.15	4.7	5×10^{-16}	8×10^{-11}
metal-Hf:Ta_2O_5/SiO_xN_y-Si structures (work in progress)						
gate	d_{if} (nm)	d_{hk} (nm)	ϕ_e (eV)	ϕ_h (eV)	σ_{hc} ($\Omega^{-1}cm^{-1}$)	$\sigma_{hk}(0)$ ($\Omega^{-1}cm^{-1}$)
Ag	2.56	5.44	2.6	4.2	2×10^{-16}	2×10^{-16}
W	2.24	5.76	2.6	4.2	7×10^{-15}	2×10^{-14}
TiN	2.10	5.90	2.6	4.2	1.2×10^{-12}	1×10^{-11}

First, as is seen from data for r.f. sputtered Ta_2O_5 on bare Si at substrate temperature 493 K, unannealed films posses high defect density, as manifested by a high value of the parameter $\sigma_{hk}(0)$; annealing substantially reduces density of these defects. Annealing also increases the band offsets, thus substantially reducing leakage currents. This is attributed to the improvement of stoichiometry of the interfacial silicon oxide.

Second, for Ta_2O_5 obtained by thermal oxidation of Ta in pure O_2 at 873 K on bare Si it is obtained that band offsets are those for SiO_2, indicating that thermally grown films posses an SiO_2-like interfacial layer. The parameter depending on the deffect density in the high-*k* layer, $\sigma_{hk}(0)$, is about two order of magnitude higher for reactive Al gate than for the nonreactive Au, W and TiN gates, indicating that deposition of the reactive gate creates high amount of defects in the high-*k* layer. Thickness of the layer is practically independent on the gate material for films as thick as 50 nm [44], and weakly dependent

on the gate material in the case of films as thin as 10 nm or thinner (nanosized dielectric) [53]. Low-field conductivity (σ_{hc}) for films as thick as 50 nm is independent on the gate material [44], while for nanosized films it is somehow reduced in the case of reactive Al gate [53]. Therefore, we conclude that the reactive gate in the case of nanosized high-*k* dielectrics affects also interfacial layer.

Third, it is seen that substrate nitridation reduces band offsets [52]. With this effect alone, the nitridation would degrade leakage properties of the dielectric films. Nevertheless, there is a more important beneficial effect of nitridation consisting in an increase of the relative permittivity of the interfacial layer and substantial decrease of the equivalent thickness with nitridation. As a result, leakage currents for same equivalent thicknesses are lower for films grown on nitrided substrates than for the films grown on bare substrates. Detailed analysis of electrical and dielectric properties of different MOS structures containing high-*k* dielectric grown on nitrided Si substrate have been reported in several works [31],[52],[62].

The model is also applicable to the structures containing Ta_2O_5 with different metals (one example is given in the last section of the Table. 2). In addition, in [54] we have shown that the model described in this work is also applicable to the case of HfO_2 high-k dielectrics, by fitting the experimental *I-V* curves obtained by other authors [55]. It is expected the same or slightly modified model to be applicable on various similar structures. Recently, an analysis of leakage properties of Al-Ta_2O_5/SiO_xN_y-Si structures based on a derived model has been published by other authors [56].

3.2. Effective capacitance

Standard methods for characterization of MOS structures include measurement of *C-V* and *G-V* (or *R-V*) curves in parallel mode (i.e., C_p-*V* and *G-V* or R_p-*V*) [51]. An alternative approach is to use *C-V* and *R-V* curves obtained in serial mode (C_s-*V* and R_s-*V*). Our extensive experience with metal/high-*k*/Si structures suggests that better results are obtained when using serial mode in characterization of capacitance properties of the considered structures. This approach has been supported by additional studies of the AC capacitance and resistance measurements at various frequencies [57],[58]. Based on the model described here an equivalent circuit (simplified equivalent circuit of that shown in Fig. 5) for the capacitance in accumulation has been constructed and applied to describe experimental results for measured capacitances and resistances as a function of the signal frequency, both in parallel and serial mode [57]. Impedance of the considered equivalent circuit (Z) is given with the following expression:

$$Z = \frac{R_{hk}}{1+(2\pi f C_{hk} R_{hk})^2} + \frac{R_{if}}{1+(2\pi f C_{if} R_{if})^2} + R_L + \frac{1}{i2\pi f}\left(\frac{1/C_{hk}}{1+1/(2\pi f C_{hk} R_{hk})^2} + \frac{1/C_{if}}{1+1/(2\pi f C_{if} R_{if})^2}\right), \quad (14)$$

where f is the measurement signal frequency. For measurements in serial mode (at given gate voltage V in accumulation), corresponding effective serial capacitance (C_s) and resistance (R_s) are frequency dependent and given with following expressions:

$$C_s(f)=\left(\frac{1/C_{hk}}{1+1/(2\pi fC_{hk}R_{hk}(V))^2}+\frac{1/C_{if}}{1+1/(2\pi fC_{if}R_{if}(V))^2}\right)^{-1} \quad (15)$$

and

$$R_s(f)=\frac{R_{hk}}{1+(2\pi fC_{hk}R_{hk}(V))^2}+\frac{R_{if}}{1+(2\pi fC_{if}R_{if}(V))^2}+R_L\,. \quad (16)$$

In [57] excellent fits to the experimental results for Al-Ta_2O_5/SiO_2 structures have been obtained when using expressions (15) and (16). Detailed analysis for the *C-V*, *R-V* and *C-V* curves for metal(Al,W,Au)-Ta_2O_5/SiO_2 structures, both in parallel and serial mode, have been reported in [51]. All the results obtained are consistent with the model described in this work.

3.3. Stress-induced leakage currents

In addition to the description of the leakage currents of fresh structures, this model has been successfully applied to the description of the stress-induced leakage currents. We dominantly studied the case of constant current stress. We have shown that *I-V* characteristics of stressed Al-Ta_2O_5/SiO_2 structures can be very well described by our model [59]. Increase of the leakage currents with the stress has been attributed to the degradation of the interfacial layer by creation of high density of defects in a part of it. This part can be degraded to the point where it can be regarded as a conductive material where conduction occurs through percolation paths [59]-[61].

4. CONCLUSIONS

Comprehensive physical model for describing electrical and dielectric properties of MOS capacitors containing high-*k*/(SiO_2,SiO_xN_y) dielectric stack has been described in details. Corresponding equivalent circuit has been constructed and displayed. The proposed model describes very well MOS structures containing Ta_2O_5 based dielectric layers, both obtained with different technological procedures and with different doping. It has been also shown that the model can be used for other high-*k* dielectrics such as HfO_2. Based on the model, degradation of the dielectric properties of the high-*k* dielectric layer induced by a reactive metal gate, such as Al, can be clearly distinguished from other effects. The model is applicable on fresh as well on high-field/current stressed samples, thus allowing analyzing the stress-induced leakage currents at medium fields. Finer details of the effect of various technological processes on the electrical and dielectric properties of the considered structures can be extracted using the model.

Acknowledgement: *This work was supported by Macedonian Ministry of Education and Sciences under Contract 13-3573.*

REFERENCES

[1] J. Zhang, Z. Li, H. Zhou, C. Ye and H. Wang, "Electrical, optical and micro-structural properties of ultra-thin HfTiON films", *Applied Surface Science*, in press, http://dx.doi.org/10.1016/j.apsusc.2013.12.064.

[2] C.Ye, C. Zhan, J. Zhang, H. Wang, T. Deng and S. Tang, "Influence of rapid thermal annealing temperature on structure and electrical properties of high permittivity HfTiO thin film used in MOSFET", *Microelectronics Reliability* **54**, 2014, pp. 388–392. (anneling)

[3] S. Chen, Zh. Liu, L. Feng, X. Che and X. Zhao, "The dielectric properties enhancement due to Yb incorporation into HfO_2", *Appl. Phys. Lett.* **103** 2013, pp. 132902 (*4 pages*).

[4] G.Lee, B.-K. Lai, C. Phatak, R. S. Katiyar and O. Auciello, "Interface-controlled high dielectric constant Al_2O_3/TiO_x nanolaminates with low loss and low leakage current density for new generation nanodevices", *J. Appl. Phys.* **114**, 2013, pp. 027001 (*5 pages*).

[5] M. Ali Khaskheli, P. Wu, R. Chand, X. Li, H. Wang, Sh. Zhang, S. Chen and Yili Pei, "Structural and dielectric properties of Ti and Er co-doped HfO_2 gate dielectrics grown by RF sputtering", *Applied Surface Science* **266**, 2013, pp. 355–359

[6] B. Toomey, K. Cherkaoui, S. Monaghan, V. Djara, É. O'Connor, D. O'Connell, L. Oberbeck, E. Tois, T. Blomberg, S.B. Newcomb and P.K. Hurley, "The structural andelectrical characterization of a $HfErO_x$ dielectric for MIM capacitor DRAM applications", *Microelectronic Engineering* **94**, 2012, pp. 7–10

[7] Z. Essa, C. Gaumer, A. Pakfar, M. Gros-Jean, M. Juhel, F. Panciera, P. Boulenc, C. Tavernier and F. Cristiano, "Evaluation and modeling of lanthanum diffusion in $TiN/La_2O_3/HfSiON/SiO_2/Si$ high-k stacks", *Appl. Phys. Lett.* **101** 2012, pp. 182901 (*5 pages*).

[8] T. Usui, S. A. Mollinger, A. T. Iancu, R. M. Reis and F. B. Prinz, "High aspect ratio and high breakdown strength metal-oxide capacitors", *Appl. Phys. Lett.* **101** 2012, pp. 033905 (*4 pages*).

[9] W.Yang, Q.-Q. Sun, R.-C. Fang, L. Chen, P. Zhou, S.-J. Ding and D.W. Zhang, "The thermal stability of atomic layer deposited $HfLaO_x$: Material and electrical characterization", *Current Applied Physics* **12**, 2012, pp. 1445–1447

[10] T. Yu, C. Jin, X. Yang, Y. Dong, H. Zhang, L. Zhuge, X. Wu and Z. Wu, "The structure and electrical properties of HfTaON high-k films prepared by DIBSD", *Applied Surface Science* **258**, 2012, pp. 2953– 2958

[11] X. Zhang, H. Tu, Y. Guo, H. Zhao, M. Yang, F. Wei, Y. Xiong, Z. Yang, J. Du and W. Wang, "Atomic configuration of the interface between epitaxial Gd doped HfO_2 high-*k* thin films and Ge (001) substrates", *J. Appl. Phys.* **111**, 2012, pp. 014102 (*4 pages*)

[12] L. Ning, F. Yang, C. Duan, Y. Zhang, Jun Liang and Z. Cui, "Structural properties and 4f→5d absorptions in Ce-doped $LuAlO_3$: a first-principles study", *J. Phys.: Condens. Matter* **24**, 2012, pp. 055502 (*10 pages*)

[13] L. Kornblum, B. Meyler, C. Cytermann, S. Yofis, J. Salzman and M. Eizenberg, "Investigation of the band offsets caused by thin Al_2O_3 layers in HfO_2 based Si metal oxide semiconductor devices", *Appl. Phys. Lett.* **100**, 2012, pp. 062907 (*3 pages*)

[14] K.M.A. Salam, H. Fukuda and S. Nomera, "Effects of additive elements on improvement of the dielectric properties of Ta_2O_5 films formed by metalorganic decomposition", J. Appl. Phys. 93, 2003, pp. 1169–1175.

[15] E. Atanassova, N. Novkovski, D. Spassov, A. Paskaleva and A. Skeparovski, "Time-dependent-dielectric-breakdown characteristics of Hf-doped Ta_2O_5/SiO_2 stack", *Microelectron. Reliab.* **54**, 2014, pp. 381–387.

[16] E. Atanassova, N. Stojadinovic, D. Spassov, I. Manic and A. Paskaleva, "Time-dependent dielectric breakdown in pure and lightly Al-doped Ta_2O_5 stacks", *Semicond. Sci. Technol.* **28**, 2013, pp. 055006–055006-9

[17] E. Atanassova, D. Spassov, N. Novkovski, and A. Paskaleva, "Constant current stress of lightly Al-doped Ta_2O_5", *Materials Science in Semiconductor Processing* **15**, 2012, pp. 98–107.

[18] Y. Karmakova, A. Paskaleva and E. Atanassova, "Interfacial layers in Ta_2O_5 based stacks and constituent depth profiles by spectroscopic ellipsometry", *Appl. Surf. Sci.* **258**, 2012, pp. 4507–4512.

[19] E. Atanassova, A. Paskaleva and D. Spassov, "Doped Ta_2O_5 and mixed HfO_2–Ta_2O_5 films for dynamic memories applications at the nanoscale", *Microelectron. Reliab.* **52**, 2011, pp. 642–650.

[20] A. Paskaleva, M. Ťapajna, E. Dobročka, K. Hušeková, E. Atanassova and K. Fröhlich, "Structural and dielectric properties of Ru-based gate/Hf-doped Ta_2O_5 stacks", *Appl. Surf. Sci.* **257**, 2011, pp. 7876–7880.

[21] A. Skeparovski, N. Novkovski, E. Atanassova, A. Paskaleva and V. K. Lazarov, "Effect of Al gate on the electrical behaviour of Al doped Ta_2O_5 stacks", *J. Phys. D: Appl. Phys.* **44**, 2011, pp. 235103–235103-10.

[22] I. Manić, E. Atanassova, N. Stojadinović, D. Spassov and A. Paskaleva, "Hf-doped Ta_2O_5 stacks under constant voltage stress", *Microelectron. Eng.* **88**, 2011, pp. 305–313.

[23] D. Spassov, E. Atanassova and A. Paskaleva, "Lightly Al-doped Ta_2O_5: Electrical properties and mechanisms of conductivity", *Microelectron. Reliab.* **51**, 2011, pp. 2102–2109.

[24] N. Novkovski and E. Atanassova, "Charge trapping during constant current stress in Hf-doped Ta_2O_5 films sputtered on nitrided Si", *Thin Solid Films* **519**, 2011, pp. 2262–2267.
[25] E. Atanassova, N. Novkovski, A. Paskaleva and D. Spassov, "Constant current stress-induced leakage current in mixed HfO_2– Ta_2O_5 stacks", *Microelectron. Reliab.* **50**, 2010, pp. 794–800.
[26] A. Paskaleva and E. Atanassova, "Evidence for a conduction through shallow traps in Hf-doped Ta_2O_5", *Mat. Sci. Semicond. Proc.* **13**, 2010, pp. 349–355.
[27] E. Atanassova, M. Georgieva, D. Spassov and A. Paskaleva, "High-*k* HfO_2–Ta_2O_5 mixed layers: Electrical characteristics and mechanisms of conductivity", *Microelectron. Eng.* **87**, 2010, pp. 668–676.
[28] D. Spassov, E. Atanassova, N. Novkovski, "Electrical behaviour of Ti-doped Ta_2O_5 on N_2O and NH_3 nitrided Si", *Semicond. Sci. Technol.* **24**, 2009, pp. 075024–075024-10.
[29] A. Skeparovski, N. Novkovski, E. Atanassova, D. Spassov and A. Paskaleva, "Temperature dependence of leakage currents in Ti doped Ta_2O_5 films on nitrided silicon", *J. Phys. D: Appl. Phys.* **42**, 2009, pp. 095302–095302-8.
[30] A. Paskaleva, E. Atanassova and N. Novkovski, "Constant current stress of Ti-doped Ta_2O_5 on nitrided Si", *J. Phys. D: Appl. Phys.* **42**, 2009, pp. 025105–025105-8.
[31] N. Novkovski, "Analysis of the improvement of Al-Ta_2O_5/SiO_2-Si structures reliability by Si substrate plasma nitridation in N_2O", *Thin Solid Films* **517**, 2009, 4394–4401.
[32] N. Novkovski and E. Atanassova, "A comprehensive model for the *I-V* characteristics of metal-Ta_2O_5/SiO_2-Si structures", *Appl. Phys. A* **83**, 2006, pp. 435–445.
[33] E. Rosenbaum and L. F. Register, "Mechanism of stress-induced leakage current in MOS capacitors", *IEEE Trans. Electron Dev.* **44**, 1997, pp. 317–323.
[34] M. Houssa, M. Tuominen, M. Naili, V. Afanas'ev, A. Stesmans, S. Haukka and M. M. Heyns, "Trap-assisted tunneling in high permittivity gate dielectric stacks", *J. Appl. Phys.* **87**, 2000, pp. 8615–8620.
[35] W. S. Lau, L. Zhong, Allen Lee, C. H. See, Taejoon Han, N. P. Sandler and T. C. Chong, "Detection of defect states responsible for leakage current in ultrathin tantalum pentoxide (Ta_2O_5) films by zero-bias thermally stimulated current spectroscopy", *Appl. Phys. Lett.* **71**, 1997, pp. 500–502.
[36] W. S. Lau, L. L. Leong, T. Han and N. P. Sandler, "Detection of oxygen vacancy defect states in capacitors with ultrathin Ta_2O_5 films by zero-bias thermally stimulated current spectroscopy", *Appl. Phys. Lett.* **83**, 2003, pp. 2835–2837.
[37] N. Novkovski, A. Skeparovski and E. Atanassova, "Charge trapping effect at the contact between a high-work-function metal and Ta_2O_5 high-*k* dielectric", *J. Phys. D: Appl. Phys.* **41**, 2008, pp. 105302–105302-4.
[38] L. Stojanovska-Georgievska, N. Novkovski and E. Atanassova, "Charge trapping at Pt/high-*k* dielectric (Ta_2O_5) interface", *Physica B: Condensed Matter* **406**, pp. 3348-3353 (2011).
[39] L.S. Georgievska, N. Novkovski and E. Atanassova, "Charge Trapping at Low Injection Currents in (TiN, Mo, Pt)/Ta_2O_5:Hf/SiO_2/Si Structures", 2012 28th International Conference on Microelectronics, Proceedings, MIEL2012, pp. 331-334
[40] F.-C. Chiu, J.-J. Wang, J. Y. Lee and S. C. Wu, "Leakage currents in amorphous Ta_2O_5 thin films", *J. Appl. Phys.* **81**, 1997, pp. 6911-6915.
[41] O. Blank, H. Reisinger, R. Stengl, M. Gutsche, F. Wiest, V. Capodieci, J. Schulze and I. Eisele, "A model for multistep trap-assisted tunneling in thin high-k dielectrics", *J. Appl. Phys.* **97**, 2005, pp. 044107–044107-7.
[42] E. Atanassova, D. Spassov, A. Paskaleva, J. Koprinarova and M. Gueorguieva, "Influence of oxidation temperature on the microstructure and electrical properties of Ta_2O_5 on Si", *Microel. J.* **33**, 2002, pp. 907–920.
[43] M. Lenzlinger and E. H. Snow, "Fowler-Nordheim Tunneling into Thermally Grown SiO_2", *J. Appl. Phys.* **40**, 1969, pp. 278-283.
[44] N. Novkovski and E. Atanassova, "Injection of holes from the silicon substrate in Ta_2O_5 films grown on silicon", *Appl. Phys. Lett.* **85**, 2004, pp. 3142-3144.
[45] C. Chaneliere, J. L. Autran and R.A.B. Devine, "Conduction mechanisms in Ta_2O_5/SiO_2 and Ta_2O_5/Si_3N_4 stacked structures on Si", *J. Appl. Phys.* **86**, 1999, pp. 480–486.
[46] M. V. Fischetti and D. J. DiMaria, "Hot electrons in SiO_2: Ballistic to steady-state transport", *Solid-St. Electron.* **31**, 1988, pp. 629–636.
[47] J. R. Yeargan and H. L. Taylor, "The Poole-Frenkel Effect with Compensation Present", *J. Appl. Phys.* **39**, 1968, pp. 5600–5604.
[48] N. Novkovski, "Limitations in the methods of determination of conduction mechanisms in high-permittivity dielectric nano-layers", *Physica B: Condensed Matter*. **398**, 2007, pp. 28–32.

[49] K. N. Yang, H. T. Huang, M. C. Chang, C. M. Chu, Y. S. Chen, M. J. Chen, Y. M. Lin, M. C. Yu, S. M. Yang, D. C. H. Yu and M. S. Liang, "A physical model for hole direct tunneling current in p^+ poly-gate pMOSFETs with ultrathin gate oxides", *IEEE Trans. Electron Dev.* **47**, 2000, pp. 2161-2166.

[50] N. Yang, W.K. Henson, J.R. Hauser and J. Wortman, "Modeling study of ultrathin gate oxides using direct tunneling current and capacitance-voltage measurements in MOS devices", *IEEE Trans. Electron Dev.* **46**, 1999, pp. 1464-1471.

[51] D. K. Shroder, *Semiconductor material and device characterization*. Hobokeen, New Jersey: John Wiley& Sons, 2006, Chapter 9, pp. 347–350.

[52] N. Novkovski, A. Paskaleva and E. Atanassova, "Dielectric properties of rf sputtered Ta_2O_5 on rapid theramlly nitrided Si", *Semicond. Sci. Technol.* **20,** 2005, pp. 233–238.

[53] N. Novkovski, "Conduction and charge analysis of metal (Al, W and Au)-Ta_2O_5/SiO_2-Si structures", *Semicond. Sci. Technol.* **21**, 2006, pp. 945–951.

[54] Aleksandar Skeparovski and Nenad Novkovski, "On the nature of the high-k dielectrics leakage current reduction by postdeposition annealing", *J. Optoelectron. Adv. Mat.* **9**, 2007, pp. 897–901.

[55] W. J. Zhu, T.-P. Ma, T. Tamagawa, J. Kim and Y. Di, "Current transport in metal/hafnium oxide/silicon structure" *IEEE Electron Device Lett.* **23**, 2002, pp. 97–99.

[56] S. Huang, "Oxygen Annealing Effects on Transport and Charging Characteristics of Al-Ta_2O_5/SiO_xN_y-Si Structure", *IEEE Trans. Electron. Dev.* **60**, 2013, pp. 2741–2746.

[57] N. Novkovski, and E. Atanassova, "Frequency dependence of the effective series capacitance of metal-Ta_2O_5/SiO_2-Si structures", *Semicond. Sci. Technol.* **22**, 2007, pp. 533–536.

[58] N. Novkovski and E. Atanassova, "Peculiarities of capacitance measurements of nanosized high-*k* dielectrics: case of Ta_2O_5", *J. Optoelectron. Adv. Mat.-Symposia* **1**, 2009, pp. 398–403.

[59] N. Novkovski and E. Atanassova, "Origin of the stress-induced leakage currents in Al-Ta_2O_5/SiO_2-Si structures", *Appl. Phys. Lett.* **86**, 2005, pp. 1521041–52104-3.

[60] N. Novkovski, E. Atanassova and A. Paskaleva, "Stress-induced leakage currents of the RF sputtered Ta_2O_5 on N-implanted silicon", *Appl. Surf. Sci.* **253**, 2007, pp. 4396–4403.

[61] N. Novkovski, E. Atanassova and A. Paskaleva, "Model Based Analysis of Electrical and Wear-out Characteristics of Ultra-thin Ta_2O_5/SiO_xN_y Stacks on Si", Proc. 26nd international conference on microelectronics, 10-14 May, 2008, Vol. 2, pp. 533–536.

[62] N. Novkovski and E. Atanassova, "Dielectric properties of Ta_2O_5 films grown on silicon substrates plasma nitrided in N_2O", *Appl. Phys. A* **81**, 2005, pp. 1191–1195.