FACTA UNIVERSITATIS
Series: **Electronics and Energetics** Vol. 30, N^o 3, September 2017, pp. 383 - 390
DOI: 10.2298/FUEE1703383V

EXPLORATION TOWARDS ELECTROSTATIC INTEGRITY FOR SIGE ON INSULATOR (SG-OI) ON JUNCTIONLESS CHANNEL TRANSISTOR (JLCT)

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Abstract. *In view of reduced electric field and avoiding source drain engineering, the work exploresstrain effect in junctionless channel transistor. To achieve scaled I_{OFF} and maintain $I_{ON,}$ here the device SG-OI JLCT is proposed. The study discusses higher switching action with mole fraction x = 0.25. The dependency of ϕ_M and the N_D is responsible for maintaining constant current for overall analysis.*

Key words: *SG-OI JLCT, SOI JLT, Drift Diffusion carrier mobility, ON-OFF Currents.*

1. INTRODUCTION

The interpretation of the Si based semiconductor industries started in 1959 and is still continuing in following Moore's law. Scaling technology contributed different leakage currents in conventional metal oxide semiconductor (MOS) Field Effect Transistor (FET) which internally affects the device performance. This gives a challenging notation to device engineers. A brief description of various leakage currents is given in [1] describing the issues at scaled channel length. In order to overcome these issues various challenges are addressed such as high-κ gate oxide engineering, spacers engineering and new materials and structural design etc. are reported [2], [3], and therefore process technology device structures have been invented. The new design architectures such as silicon on insulator (SOI) [4], double gate MOSFET (DGMOSFET) [5], [6], tri gate MOSFET (TMOSFET) [7], gate all around (GAA-MOSFET) [8], Fin-FET [9], [10] etc., are briefly described.

Apart from this, a new device structure has been identified such as Lilienfeld's first transistor architecture [11], and followed with various structural design approach as a tri-gate architecture with no doping gradients is given in [12]. Accordingly, a vertical gate stack SOI and bulk planar Junctionless transistor are reported in [13]–[15].

Received September 29, 2016; received in revised form January 23, 2017
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Junctionless nanowire (JN) transistor are uniform with heavy doping profile of 10^{19} to 10^{20} cm^{-3} with in a Si device layer, the JN is usually a ON resistor which do not require any metallurgical junctions across the channel edges. Depending on the type of transistor N^+ or P^+ is doped along S/D channel regions. This approach is well simplified and fabricated with standard CMOS technology [16], [17]. The physics behind the architecture is given for LG < 20-nm. For N-type MOSFET, due to N+ doping concentration, a high electric field is generated along the vertical direction, which makes the channel fully depleted below VTH with VGS = 0 V, and above VTH field drops to zero. Therefore due to its specific merits JLT along with different structures are preferable for scaling short channel effects.

The paper proposes a SiGe on Insulator (SG-OI) [18]–[21] using junction-less channel Transistor. N_D is taken as SiGe to evaluate the performance of the device with respect to I_{OFF}. The parameters listed in Table 1 are used to investigate electrostatic integrity of the device. The obtained results are verified with SOI-JLT and conventional MOSFET. Fig 2 shows that our simulation model is in well agreement with [13].

With the inherent features of the JLT, a $Si_{1-0.25}Ge_{0.25}$ mole fraction (x) material is taken along S/D and channel regions with uniformly high N_D. The conduction mechanism of JLT shows the difference in ϕ_M - ϕ_S (JLT conducts above 5 eV work function) leads to the positive shift in V_{TH} and bands becomes flat at $V_{FB,}$ which then takes a path for the conduction at positive V_{GS}. The channel depletes completely at zero V_{GS}. At high N_D mobility degrades perpendicularly to channel and with low electric field enhances mobility.

Along with introduction, section II discusses the device structure and physics behind the device that carried out simulations, and activated models for the simulations. Section III describes the study of electrostatic integrity of SG-OI JLCT. Section IV deals with conclusion and remarks of the proposed device.

2. SILICON GERMANIUM ON INSULATOR JUNCTION-LESS CHANNEL TRANSISTOR (SG-OI JLCT)

The schematic diagram of SG-OI JLCT is shown in Fig.1. The architecture is carried out with no metallurgical junction in lateral direction, hence named JLCT. According to the features and specifications listed in table 1 the device has been designed, and the parameter specifications are taken from [4], [13], [14].

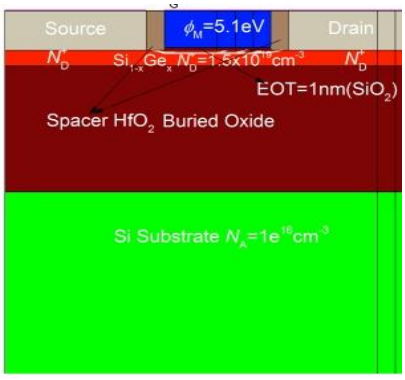

Fig. 1 Cross sectional view of SG-OI JLCT

Junctionless transistors are the devices with no doping gradients across source channel and drain edges. Usually, the device layer is doped with high doping density. The gate metal is taken at high work function ϕ_M of 5.1 eV. For isolation purpose a SiO_2 is considered. The spacers are provided with high-κ HfO_2 [22], [23]. A fully depleted SiGe layer is grown epitaxial on an insulator (FD SG-OI JLCT) forming a conducting path across the device layer. The strain induce effect occur when a SiGe layer is grown epitaxial on a thin silicon substrate. [24], [25] a simple identification of the device performance is represented by considering a relaxed SiGe layer, with the change in the molefraction value. The model used for the simulation is default drift-diffusion carrier transport mobility model. The mobility model is then dependent on the doping concentration with high field saturation carrier densities and transverse field dependence. As SiGe is compound material, a mole fraction dependent effective intrinsic density band gap narrowing model for SiGe is used for the device. The structure assumes to be abrupt and taken at room temperature. In order to solve this, a self-consistent Drift-Diffusion equation is used. Due to its high N_D across lateral direction and OldSlotboom band gap narrowing model and Schottky-Read-Hall mechanism is accounted. The model calculates the intrinsic carriers for silicon material. It then improves the carrier mobility under high field saturation. The overall simulations are carried out using Sentaurus TCAD 2D Simulator [26], [27].

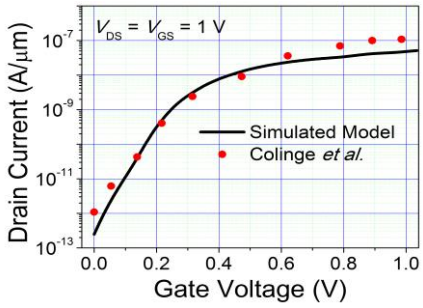

Fig. 2 Comparison of $I_{D,LIN}$ with respect to V_{GS} plot for SG-OI JLCT at V_{DS} = 1 V and [13] with simulation L_G = 20-nm, ϕ_M = 5.1 eV, N_D = 1.5e19 cm^{-3}

Table 1 Parameter required for simulation [28][], [13].

Parameters	SG-OI JLCT	Conventional MOSFET
SiGe layer (T_{Si}) for SG-OI JLCT	5-nm	5-nm
Donor doping (N_D)	1.5x10^{19} cm^{-3}	10^{18} cm^{-3}
EOT of gate dielectric (T_{OX})	1-nm	1-nm
Gate work Function (ϕ_M)	5.1 eV	4.6 eV
Well doping (N_A)	5x10^{18} cm^{-3}	10^{15} cm^{-3}
Drain Supply Voltage (V_{DD})	0.05 V, 1 V	0.05 V, 1 V
Channel length (L_G)	20-nm	20-nm

3. RESULTS AND DISCUSSIONS

The section deals with the results and discussions that carryout for the simulations with the parameter values of V_{DS} = 0.05 V for $I_{D,LIN}$ and V_{DS} = 1 V for $I_{D,SAT}$ with V_{GS} = 1 V. Basically the paper deals with the electrostatic integrity (EI) parameter which usually has short channel effects and DIBL given in equation 2 and 3. This induces a qualitative control on the channel through the gate. In short channel devices the channel is predominated by gate with affecting electric field lines from source to drain. As the approach is fully depleted, SG-OI EI is shown in equation 1, most of the electric field lines propagate through box to channel which can reduce SCE. Further this has an inconvenience of increasing junction capacitance and body effect [30]. Firstly from Fig. 4 our model is well suitable for reducing I_{OFF} at 10^{-13} (A) and I_{ON} is maintained 10^{-06} (A) which is then compared with [13]. A comparative analysis is shown for conventional MOSFET, SOI JLT and a SG-OI JLCT. The main intention behind the analysis is to scale $I_{OFF,}$ the challenges for scaling I_{OFF} is [28], (1) having a thin channel region, (2) considering High κ spacers, which improves the I_{OFF} and (3) temperature doping dependent channel is considered.

$$EI = \left[1 + \frac{t_{Si}^2}{L_{el}^2}\right] \frac{t_{ox}}{L_{el}} \frac{t_{Si} + \lambda t_{BOX}}{L_{el}} \tag{1}$$

$$DIBL = 0.80 \frac{\varepsilon_{Si}}{\varepsilon_{ox}} EIV_{DS} \tag{2}$$

$$SCE = 0.64 \frac{\varepsilon_{Si}}{\varepsilon_{ox}} EIV_{bi} \tag{3}$$

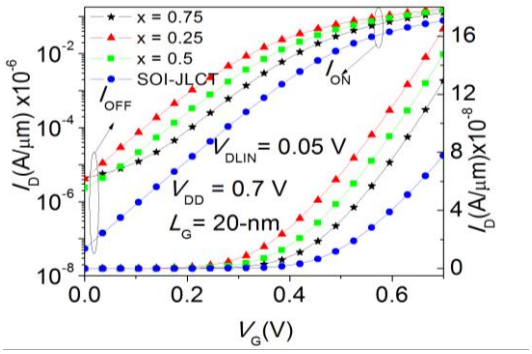

Fig. 3 Comparative Analysis of $I_{D,LIN}$ with respect to V_{GS} is shown for SOI JLCT and SG-OI JLCT. With ϕ_M = 5.1 eV, N_D = 1.5e19 cm^{-3} and L_G = 20-nm

Fig. 3 Comparison of $I_{D,LIN}$ with respect to V_{GS} is shown for SOI JLCT and SG-OI JLCT. I_{ON} is improved in case of SG-OI JLCT and I_{OFF} shows better improvement in SOI JLCT. This shows that at x = 0.25 the values are similar to those given in [13]. As the SiGe is a compound material, there is possibility of a varying band gap from 0.6 to 1.1 eV. This variation of bandgap is obtained due to tuning the molefraction value (x = 0.25, x = 0.5, and x= 0.75). The composition of Si is high in content; therefore the device

acquires the Si material characteristics though the channel is maintained to be SiGe material. However, the band gap value of Si is 1.1 eV, but for SiGe at x = 0.25 the bandgap value is almost near to 1.1 eV. If the molefraction x = 0.75 the bandgap value is near to 0.6 eV, hence the channel acts according to the Ge material properties shown in Fig. 4. [31] Provide Ge MOSFET advancement in electrical performance which represents the switching activity and the mobility enhancement to that of an Si MOSFET [32]. Fig. 5 shows the DIBL as a function of I_{ON} is represented for both SG-OI JLCT and SOI JLCT. At x = 0.25 I_{ON} is improved in case of SG-OI JLCT but DIBL remain equal for both the devices and at x = 0.75 I_{ON} found to be less and DIBL is very high which is not considerable. In order to improve I_{ON} and DIBL for x = 0.75 a proper tuning of ND and work-function is suggested.

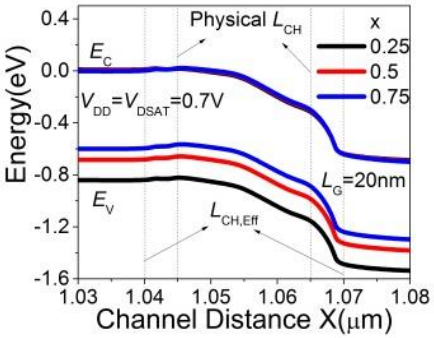

Fig. 4 Energy with respect to Distance "X" along the channel for SG-OI JLCT is shown. For $Si_{1-x}Ge_x$ channel (x = 0.25, 0.5, 0.75), V_{DSAT} = 0.7 V and T_{Si} = 5 nm is given.

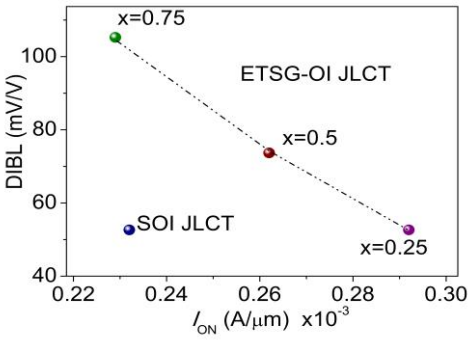

Fig. 5 DIBL with respect to *I*ON for both SG-OI JLCT and SOI JLCT is shown. *V*D,LIN = 0.05 V, *V*D,SATm = 1 V and x = 0.25, 5, 0.75

Fig 6 investigates the impact of ϕ_M on I_{ON} and I_{OFF}, as JLT works ϕ_M > 5 eV the performance of the device is shown accordingly. It is clear that at ϕ_M > 5.2 eV I_{ON} and I_{OFF} start degrading. Though the device takes the Si material properties, the concentration of the Ge at SiGe channel will affect the electric field at low V_{TH}. Hence results in I_{OFF} improvement. [14] JLT as Si channel has ϕ_M = 5.5 eV. In the proposed work, Fig. 3 compares $I_{D,LIN}$ function of V_{GS} plotted with x = 0.25 for SG-OI JLCT. As the value of x increases a

drastic degradation of device performance takes place, as shown in Fig. 7 with respect to I_{ON}/I_{OFF} ratio.

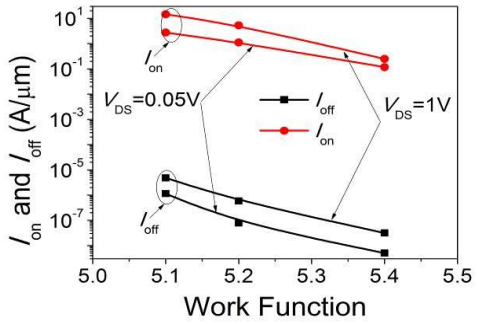

Fig. 6 Impact of metal work function ϕ_M on I_{ON} and I_{OFF} of the SG-OI JLCT with x = 0.25, N_D = 1.5e19 cm^{-3}, EOT = 1-nm with L_G = 20-nm

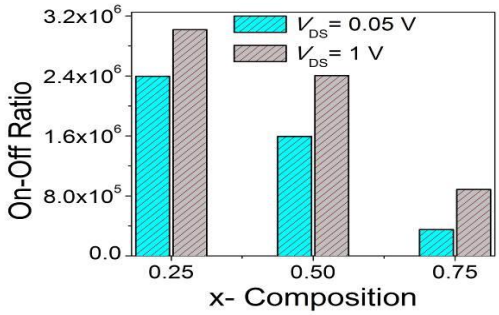

Fig. 7 I_{ON}/I_{OFF} of the SG-OI JLCT with different x composition (x = 0.25, 0.5, 0.75), ϕ_M = 5.1 eV, N_D = 1.5e19 cm^{-3}, EOT = 1-nm with L_G = 20-nm

4. CONCLUSION

The paper investigates an improvement in I_{OFF} current and maintaining I_{ON} at 10^{-6} Amp's. A conduction mechanism of SG-OI JLCT with the concept of relaxed SiGe on insulator is explained. The $I_{D,LIN}$ and $I_{D,SAT}$ values at x = 0.25, ϕ_M = 5.1eV is considered to estimate the I_{OFF}. Therefore from the above results SG-OI JLCT performs better at x = 0.25 by activating the drift-diffusion carrier mobility and SRH mechanism for high field saturation mobility model using sentaurus TCAD 2D simulator. And study towards electrostatic integrity can then be evaluated.

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