FACTA UNIVERSITATIS
Series: **Electronics and Energetics** Vol. 28, N^{o} 2, June 2015, pp. 223 - 236
DOI: 10.2298/FUEE1502223M

OSCILLATION-BASED TESTING METHOD FOR DETECTING SWITCH FAULTS IN HIGH-Q SC BIQUAD FILTERS

Miljana Milić, Vančo Litovski

Faculty of Electronic Engineering, University of Niš, Serbia

Abstract. *Testing switched capacitor circuits is a challenge due to the diversity of the possible faults. A special problem encountered is the synthesis of the test signal that will control and make the fault-effect observable at the test point. The oscillation based method which was adopted for testing in these proceedings resolves that important issue in its nature. Here we discuss the properties of the method and the conditions to be fulfilled in order to implement it in the right way. To achieve that, we have resolved the problem of synthesis of the positive feed-back circuit and the choice of a proper model of the operational amplifier. In that way, a realistic foundation to the testing process was generated. A second order notch cell was chosen as a case-study. Fault dictionaries were developed related to the catastrophic faults of the switches used within the cell. The results reported here are a continuation of our previous work and are complimentary to some other already published.*

Key words: *OBT method, SC filters, switch faults, fault dictionary*.

1. INTRODUCTION

The synthesis of test signal is one of the essential problems in analog circuits testing. Choices among many possibilities have to be made. First, one should select an analog test domain [1]. Testing can be done by analyzing DC signals [2, 3, 4], signals in the frequency domain [5, 6, 7], as well as the signals in the time domain [8]. It is often necessary to use test signals from several domains simultaneously. If we use DC signals, then we search for fault effects related to the nonlinearities and quiescent conditions. A number of methods consider the time domain test signals selection [9, 10, 11]. In the frequency domain, one has to determine the most appropriate spectrum of the testing signal in order to achieve maximal fault effects. In the time domain one searches for one or more signal waveforms that will enable the fastest and the cheapest testing, in order to optimize the production and decrease the price of the product.

A technique that does not require solving such problems since it needs no test signal is the Oscillation-Based Test (OBT), [12]. To implement this powerful method one has to create a feed-back during testing. By measuring the frequency of the created oscillator and by comparing that with the fault-free frequency, one can detect defective circuits.

Received May 16, 2014; received in revised form January 19, 2015
Corresponding author: Miljana Milić
Faculty of Electronic Engineering, University of Niš, Aleksandra Medevedeva 14, 18000 Niš, Serbia
(e-mail: miljana.milic@elfak.ni.ac.rs)

Structural testing is a concept where test signals that detect one or more faults are created. To detect all most possible faults we need many tests. In OBT all possible defects are targeted with only one measurement since they all affect the oscillation frequency. Here comes the major difference in oscillator design. Regular oscillators are created to be insensitive to the presence of parameter variations. On the other hand, OBT oscillators and their oscillation frequency should be as much sensitive to parameter variations as possible. Unfortunately, the OBT technique cannot be automated, since each analog circuit is unique. That is the biggest difficulty in implementing the method.

Unlike other testing approaches where numerous and most appropriate testing points have to be selected, observed, and captured signals processed, [13], the number of OBT test points is one, i.e. the oscillator's output. Nevertheless, the problem of measurement is not solved, since one has to decide which parameters of the response should be measured and extracted.

There are also other problems related to OBT implementation. First, bringing the oscillations into a stable state can slow down the testing process. Second, in rare situations observing just one testing point (for example, the output voltage), cannot show the fault effect, so additional measurements are needed, such as IDDQ [14, 15]; additional voltage waveforms [16]; or even mixing domains, including physical redesign of the original circuit to create access points for measurement [17]. Problems of needed test (measurement) points and most appropriate quantities of observation for determining the state of the circuit should be solved [18, 19].

The oscillation based testing (OBT) method [12, 20, 21] has been drawing our attention for a relatively long period. The main reason for that was the fundamental discrepancy between the theoretical developments reported by the original authors and the practical implementation of the method. Namely, as elaborated in [22, 23, 24] the original method is based on the presumption that the operational amplifiers (OA) (or active amplifying elements) within the circuit under test (CUT) perform ideally as if the frequency is equal to zero. In practice, that is not the case. In fact, at the oscillation frequency the modulus and the phase of the gain of the operational amplifier(s) are so degraded that it makes the theoretically developed expressions not only impractical but also misleading. Both the oscillation frequency of the fault-free (FF) and faulty circuits (FC) obtained by the closed form expression derived based on the original method are far from the real ones. Later implementations of the OBT concept [25, 26, 27, 28, 29, 30] suffer from the same drawback. Namely, if one generates a fault dictionary using closed form formulae (or even by simulation) based on use of ideal model of the operational amplifier, and then verifies the results by (repeated) simulation based on the same models, one does not notice the fundamental problem: the gain and the phase distortions of the operational amplifier are not negligible and the fault dictionaries are far of the realistic ones.

It is worth mentioning that, admittedly, the need to include the operational amplifier's phase shift in the evaluation of the oscillation frequency for implementation of the OBT method to continuous time analog filter was mentioned earlier in the literature [31]. The idea was, however, implemented in the frequency domain and led to conclusions quite different than the ones we reported in [22]. We find the implementation of the OBT method for continuous time filters reported in [32] to be the proper one. There, of course, due to the complexity of the CUT the developments in the frequency domain were, simply, not feasible.

Based on those considerations we concluded that a different, not analytical, approach to the extraction of these two quantities based on realistic (dynamic) models of the operational amplifiers and time (not frequency) domain simulation is to be implemented. Of course, that introduces an additional problem related to the overall time needed to get the fault dictionary (for as many faults as needed) since one needs to extract the oscillation frequency from a time domain signal which in turn has to reach a steady-state.

The problems introduced in practical implementation of the OBT, however, are broadly compensated by the sole fact that OBT resolves the main problem in the test generation per se. Namely in general, and especially for analog circuits, the synthesis of the testing signal is a problem above all. OBT needs no test signal and, if testable, it exposes any fault present in the circuit. That enables simple implementation of the structural concept [33] to the test signal generation by which only selected faults (being the most probable) in the system are targeted.

The OBT method was implemented to several types of circuits (as listed in all references above) among which to switched capacitor (SC) filters [34, 35, 36, 37, 38]. The problem of the non-idealities was considered in [37] where, due to the difference between the conclusion obtained from the z-domain and from time domain, much attention was paid to the time domain simulation for generation of the fault dictionaries. There, a simple CMOS transconductance amplifier was implemented in the schematic of the SC filter and a conclusion was drawn that the difference between the time and frequency domain analysis is to be attributed to the feed-back circuit. We believe that a purely resistive model of the transistors within the op-amp was used. It is well known, however, [39] that the op-amp implemented in SC circuits has to fulfill stringent requirements not only in the frequency domain (including the nominal gain and the cut-off frequency) but also in the DC domain (low offset), and in transient domain (high slew-rate). In addition, low noise requirements are usually imposed. For example, in [40] the authors recommend the LT1055 op-amp which, in fact, has a JFET at the input in order to reduce the noise. This is why, we think, the main circuit, not the feed-back, is imposing the need to have a much better model of the operational amplifier. That was illustrated in more detail in [22].

Considering the OBT method, a very important and powerful one, and having in mind the need for a more realistic implementation, we started to resolve the corresponding issues of implementation of OBT to the testing of SC filter cells, one by one. The nature of the faults in SC circuits was studied in [41]. Namely, within a circuit one may encounter parametric and catastrophic faults. Parametric faults here are related only to the capacitance values. Catastrophic faults may belong to the following categories: faults related to the connection lines, faults related to the capacitors, faults related to the switches (transistors), and faults related to the operational amplifiers. To generate a fault dictionary, however, one has to resolve the synthesis of the oscillator and the fault insertion method first.

We first attacked the problem of synthesis of the feed-back loop that enables oscillation. The success was demonstrated on the simplest situation that is fault dictionary creation for parametric or soft faults. [42]. Large changes were attributed to all capacitance values. Introduction of catastrophic faults into a circuit that has active elements and feed-back loops is a challenging task since the fault may have several very dramatic consequences. Firstly, a catastrophic fault may change the quiescent working conditions of the active elements, eventually bringing them in saturation or in cut-off. That fundamentally changes the circuit behavior and makes the simulation settings much more complicated. One is not to forget that the simulation of an oscillator is a specific

problem related to the conflict between the requirements for a stable numerical integration rule and simulation of an unstable electronic circuit. On the other side, a catastrophic fault may break the existing or establish a new feed-back loop that, again, leads to a totally new circuit with unknown properties and behavior. For that reason, when speaking of catastrophic faults, we first considered the capacitors in an SC notch cell [43]. After getting good results and after considerable experience was accumulated we are here attacking the second element type of the SC filters, the switches. The results reported here are complimentary to the ones reported in [43] (which are not repeated here) and we consider the present and the report given in [43] as completion of a single task. To our knowledge the fault dictionaries reported here are the first and unique base for testing a notch SC cell.

The paper is structured in the following way. In the next section the analysis and design of the high Q SC notch cell is described. Then, in section 4, the OBT is discussed and application described. There follow, in paragraph 5, the main results being related to the method of creation of the fault dictionary and the dictionary itself. Here the discussion of the results is given too.

2. HIGH Q SC NOTCH FILTER

A switched capacitor (SC) is an integrated electronic element used in discrete time signal processing systems. The main idea is to use capacitors and switches to emulate the drawbacks of integrated resistors which have pure accuracy and temperature dependence properties. In that way discrete time systems are obtained from continuous time originals. The circuits so obtained use non-overlapping signals to control the switches, often termed Break before Make switching, so that all switches are open for a very short time during the switching transitions. Filters implemented with these elements are termed 'switched-capacitor filters'. The switching frequency may be used to control the response of the filters since the equivalent resistances are directly dependent on it.

From the implementation point of view the SC filters are in between the analog and the digital ones. Namely, while the signals are sampled they are not quantized so that their advantage over digital filters is the potential to achieve a high dynamic range. In the same time the need for analog-to-digital (AD) and digital-to-analog (DA) conversion as well as digital signal processing (DSP) hardware is avoided. The analog output signal is simply restored by a low-pass filter. On the other side, besides the potential to be integrated in silicon which is not the case for the continuous time RC active filters, unlike continuous time filters (which have to be constructed with resistors, capacitors and sometimes inductors whose values are accurately known), switched capacitor filters depend only on the ratios between capacitances and the switching frequency.

For all these reasons SC filters are an important class of integrated circuits and testing of SC filters is an important issue in electronic design.

The physical realization of the SC filters is very frequently performed by cascading second-order cells. That concept will be followed here, too. A topology of a universal second order SC filter cell is depicted in Fig. 1 [44, 45]. This is a well known Fleischer-Laker active SC filter [46]. By proper choice of the parameter values of the cell one may produce all four variants needed for complete filter design: low-pass (LP), band-pass (BP), band-stop (notch), and high-pass (HP). In these proceedings (as we did in our previous

research related to the OBT method) the notch cell will be elaborated mostly because it may be stated as the most complex one. Namely, it has to suppress part of the frequency band and has two pass-bands. In addition, when creating filters with transmission zeroes at the axis of real angular frequencies, this cell is used as many times as the number of transmission zeroes is (which usually is n/2-1, n being the order of the filter). Practically only one additional cell of the type LP, BP or HP is enough to complete the filter realization. Finally, it is not to forget that the use of a universal topology drastically simplifies the layout design since it allows for 'programming' the layout on the chip.

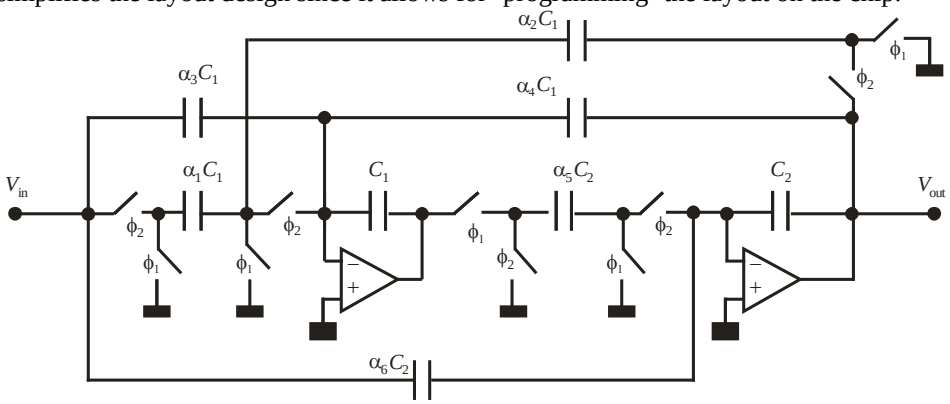

Fig. 1 High Q SC Notch filter cell

The transfer function of the cell T(s), obtained under presumption that the operational amplifiers have infinite gain (not frequency dependent) is given by

$$T(s) = \frac{V_{out}(s)}{V_{in}(s)} = -\frac{K_2 s^2 + K_1 s + K_0}{s^2 + \frac{\omega_0}{Q} s + \omega_0^2}. \tag{1}$$

The element values of Fig. 1 may be related to the coefficients of (1) in the following way [44]:

$$\alpha_1 = K_0 T / \omega_0 \tag{2}$$

$$\alpha_2 = |\alpha_5| = \omega_0 T \tag{3}$$

$$\alpha_3 = K_1 / \omega_0 \tag{4}$$

$$\alpha_4 = 1/Q \tag{5}$$

$$\alpha_6 = K_2, \tag{6}$$

where K_0, K_1, K_2 are constants determining the position of the passband on the frequency axis, e.g. low-pass, band-pass, etc., while ω_0 – notch frequency, Q – quality factor, and T – non-overlapping clock period, are design parameters.

In the specific case of a notch transfer function one should choose $K_0 = (3 \cdot \omega_0)^2$, and $K_1=0$, $K_2=9$. In the above expressions T stands for the sampling period and $\omega_0 = 2\pi f_0$, is equal to the modulus of the pole of the cell which is, in the same time, equal to the notch frequency.

The cell is usually designed using (1). To do that we choose as an example for this study the following: f_0=1 kHz, Q=10, T=10 μs (the frequency of the two-phase, non-overlapping switching is 100 kHz), and capacitances C_1=C_2=20 pF. The selected value of Q, which is recognized as quality factor of the cell, is considered large, hence the name of the cell. After substitution of these values in (2)-(6) we obtain: ω_0=6283.18 rad/s, α_1=0.063, α_2=0.063, α_3=0, α_4=0.1, α_5=0.063, and α_6=1.

The amplitude- and phase-frequency response of this filter cell, produced under the presumption of use of infinite gain operational amplifiers, is depicted in Fig. 2. Note the usual SPICE [47] presentation of the phase which is presented as if the phasor is jumping for 180 degrees.

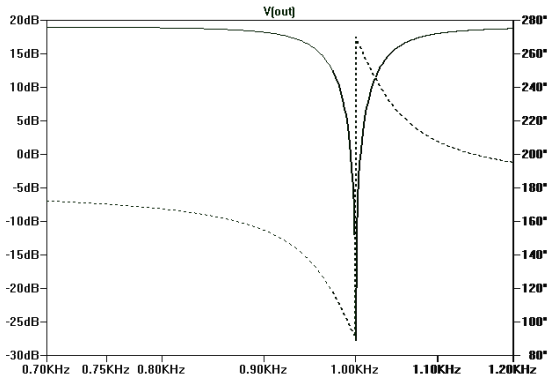

Fig. 2 Amplitude (full line) and phase (doted) frequency response of the "ideal" filter

3. BASIC CONCEPTS OF THE OBT

Under testing, within these proceedings, we will understand the creation of a fault dictionary. It is a look-up table containing the effect of every fault conceived in advance. By using it we practically implement the simulation before test approach [33]. The information stored in it tells the test engineer whether the selected fault is testable from both points of view: controllability and observability. The main problem hidden behind this table is the selection of a test signal that will activate and propagate the fault effect to the output in the shortest time (to reduce the overall testing in mass volume production). This problem is especially difficult to solve for analog circuits [48] since three domains are to be taken into account: DC, frequency and the time domain.

There exists, however, a technique that needs no test signal. It is known as the OBT [12, 20, 21]. The basic idea behind this powerful method is to create a redundant feed-back loop that is to be activated during testing only. By measurement of the output signal of the FC and by comparison with the response of the FF circuit, one may conclude whether there are defects in the circuit or not. The simplicity of the method is deeper since usually only one testing point is needed (the output) and frequently only one quantity is to be observed: the oscillation frequency. When the FF circuit is set to oscillate, the FC may be revealed either by absence of oscillation or by a different value of the frequency of the signal measured at the output.

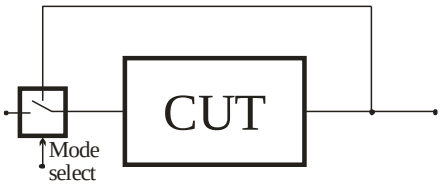

Fig. 3 Simplified OBT

For the implementation of this method it is assumed that the system is so structured that an external controlling signal is capable of (1) isolating a part of it (being the CUT) and (2) introducing positive feed-back that will make it oscillate. Fig. 3 represents the local arrangement. As can be seen a switch is introduced that, under control of the 'mode select' signal, when activated, simultaneously isolates the CUT from the rest of the circuit and positive connects the feed-back branch. This concept allows for implementation of the design for testability (DFT) concept of integrated circuits (IC) design which is depicted in Fig. 4 in its simplified version [22, 43]. The development of the schematic proposed here is based on [49]. It is reminiscent of the one published in [50] where more details concerning the digital circuitry may be found.

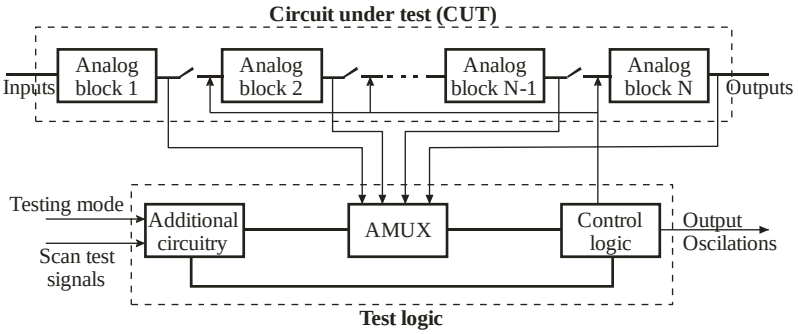

Fig. 4 OBT at the system level

In this configuration additional digital control logic is provided in order to set the system in testing mode and to allow for the analog CUTs to be isolated and tested one by one. Since no test signal is needed, in testing mode, only the output of the cells is to be connected to the system output. Note that every analog block is to be designed with a structure as depicted in Fig. 3.

When first reported the OBT method was based on two fundamental presumptions: the active elements are ideal with infinite gain and consequently the system is linear. Neither of these presumptions is valid. Namely, the operational amplifiers which are necessary for implementation have real properties such as, among many others, finite and frequency dependent modulus of the gain and a phase shift that is different from zero and also frequency dependent. Ignoring these properties leads to wrong expressions for calculation of the oscillation frequency and consequently wrong values for the outcome. Unfortunately, the fact is that if the simplest, more realistic model of the OA was to be implemented (single pole roll-off) there would not be possible to get a closed form expressions due to the complexity of the node equations of the system. In fact, nonlinear expressions are obtained.

On the other side, there are no linear active circuits as such. Furthermore, one is to be aware that if one designs an oscillator, one must draw the working point of the active element into saturation in order to limit the rise of the amplitude being forced by the positive feed-back. So, in part of the period, the circuit must be nonlinear. How long the active element will stay in saturation will depend on the quality of the feed-back loop, i.e. on the value of the modulus of the loop-gain. Again, we come to the conclusion that no closed form expressions may be derived for calculation of the oscillation frequency. Here we will allow ourselves to make a small digression. The fact that there are nonlinearities within the feed-back loop does not disqualify the OBT method as such. On the contrary! The abundance of harmonics in the output signal may be effectively used as additional information (besides the oscillation frequency) for both testing and diagnostic purposes [23, 24]. The use of harmonic analysis of the output signal (that may be done of-line) may drastically reduce the additional efforts, redesigns, and silicon area needed in order to get the supply current as additional information for testing what was done in [51].

To summarize, if the simulation with proper models of the active elements is presumed instead of closed form expressions, and if the problem of the additional circuitry needed to create positive feed-back loop is resolved, the OBT method becomes a powerful means for testing and diagnosis of not only analog but also mixed-signal systems [20, 23, 24].

4. SIMULATIONS AND TESTING

The creation of the fault dictionary goes as follows. A list of faults is assembled first. It is normally shorter than the list of all possible faults for several reasons, one of them being the tractability of the testing process, while another is lower probability of occurrence of some specific faults. In these proceedings, as explained in the introduction we will consider the faults related to all transistors used as switches. Two types of faults will be taken into account: stuck-at-open and stuck-at-closed. For the circuit of Fig. 1 where 10 switches are used, one is to create a fault dictionary with 21 rows, the first one being allocated for the FF circuit. In the next step a fault is to be inserted in the circuit [52]. In our case we have to model an open-circuit (stuck-at-open fault) and a short-circuit. In the former case we use two variants. In the first we consider the open to be an infinite resistance (ideal open), while in the second we choose a more realistic model: the open has finite resistance of 1MΩ (representing the leakage between the source and the drain). Similarly, for the modeling of the stuck-at-short we use a real short-circuit, i.e. zero ohms (ideal short) or the more realistic 0.01Ω (representing a physical short circuit). Note, to ensure numerical accuracy one is to use a relatively small span of the resistance values between the open and the closed case. In SPICE one uses 1 GΩ and 1 Ω as defaults. What we use is more realistic and less parted. Accordingly, in the sequel we will present two fault dictionaries, one for ideal and the other for more realistic models of the faults. Based on these, we will conclude whether we can rely on the ideal switch models or not.

To get the oscillation frequency of the FF circuit it has to be extended by a positive feed-back loop. Having in mind the value of the gain of the notch cell alone, we concluded that additional gain is to be added to the loop for the oscillations to be enabled. Furthermore, the additional gain is to be positive and small enough to avoid excessive harmonic distortions. In fact, additional gain of 6 dB was added to the loop-gain. The resulting configuration is depicted in Fig. 5 where the schematic is copied from the schematic input to the SPICE simulator.

Before proceeding to simulation we had to solve two additional issues. The first one is related to the choice of the integration rule for the differential equation solver within the simulator. Namely, if one is to simulate an electronic circuit, one usually asks for an integration rule (or derivative approximation formula) that is stable and if possible A-stable. That however, as shown in [53], may lead to a signal with a decaying amplitude which eventually vanishes due to the stability requirement imposed. For that reason, for simulation of oscillator circuits, the so called trapezoidal integration rule [53] is to be implemented.

Finally, a realistic model of the operational amplifier is to be chosen and implemented. Since no model (schematic neither) is normally given with the design kits delivered together with the technology file for IC design for the academic licenses we use, we were forced to use a model that is built in the simulator. That was the model of the LTC6078 [54] op-amp whose schematic is built into the LTspice simulator [47]. We published the schematic and the parameters of the model in [22].

All conditions set, after the simulation of the FF circuit, we obtained oscillation with frequency f_{osc}= 960 Hz. The fast Fourier transform (FFT) analysis results for the obtained output signal is shown in Fig. 6. That is the information from which the oscillation frequency was extracted.

In order to get the fault dictionary, as can be seen, for every fault we have to simulate the oscillator and to perform FFT. Here all together we needed 41 simulations and FFT analyses. The results are given in Table I and Table II. The first one uses ideal models of the faulty switches, while the second one uses more realistic models of the faulty switches.

The test dictionaries expressed by Table I and Table II contain the following data for the FF and for every FC: 1. Oscillation frequency; 2. deviation (in percentage) of the oscillation frequency from the FF circuit; 3. and 4. The amplitude and the phase of the first harmonic; 5. The DC value of the output; and 6. The THD of the output signal.

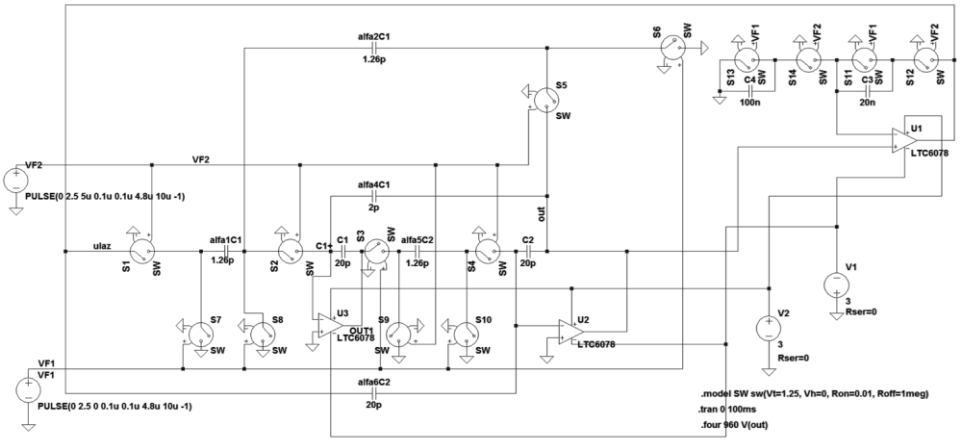

Fig. 5 LTspice schematic of the Notch filter

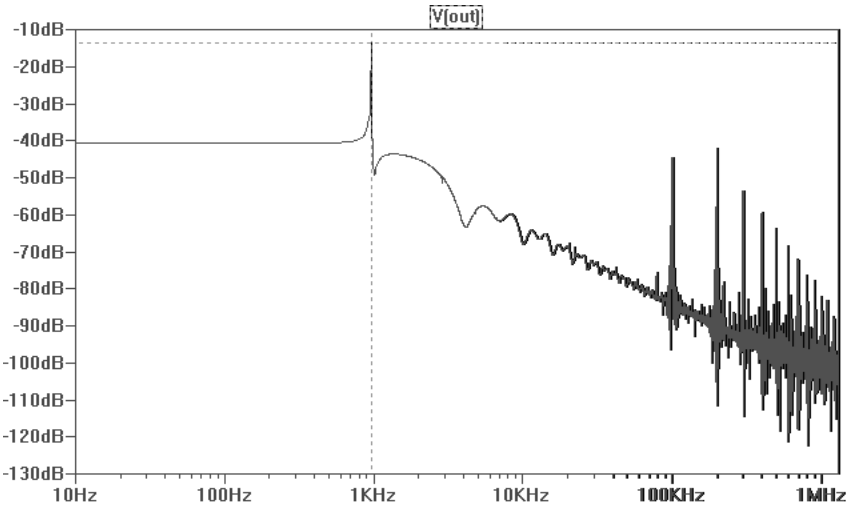

Fig. 6 FFT of the OBT oscillator output signal

We note, at the beginning, the difference between the notch and the oscillation frequency of the FF. For the idealized case it is 1 kHz, while for the case when realistic models of the op-amps are implemented it becomes 960 Hz. These, if ideal operational amplifiers were to be implemented, would be equal. One is not to forget that 1 kHz is a very low frequency and this effect is to be expected to have much more severe consequences if the working frequency of the circuit is to be risen. We also expect that a higher gain in the additional circuit will be needed if oscillations at higher frequencies are to be created.

As can be seen from the f_{osc} column for both tables, oscillations are not established in all FCs. In cases where no oscillations are established, one simply concludes that the fault is testable. When however, the oscillations are established in the FC, we may distinguish three situations. In the first one, such as the cases S1-open, S5-open, and S7-short, in Table I, there is clear difference in the oscillation frequency. That is enough to conclude that the fault is testable. In the second case, we may have oscillation with frequency near to the one of the FF but with a clearly different value of the amplitude of the first harmonic. This is practically always the case in Table I and Table II.

There is one case in Table II which deserves some additional attention. Namely, when S2-short is present, if not satisfied, in order to get an absolutely firm conclusion about the presence of the fault, one may take into account not only the frequency (difference is 8.3%) and the amplitude of the first harmonic (difference is 29%), but the harmonic distortions, too. In all other cases there is no practical need for the use of the phase shift, the DC values and the distortions as an information about the testability of the circuit.

There is a special situation where no sinusoidal oscillations are observed at the output. These are marked by 100k in the oscillation frequency column. Instead, as a consequence of clock feed-trough, trapezoidal waveform, having the frequency of the clock, is obtained at the output. Note that since such signal is far above the passband of the low-pass filter used at the output of the SC cell, if one wants to diagnose this effect, one is to measure directly at the SC output. In the opposite, the filter will suppress this fault effect.

Table 1 Simulation with ideal switch model – Fault dictionary

Defect	fosc [Hz]	δfosc [%]	Ampl. 1st. har. [mV]	Phase 1st. har. [deg]	DC val. [mV]	THD [%]	comments
FF	960	-	266.6	-125.45	-0.218	0.353	
S1 - open	360	62.5	139.6	-40.12	-0.073	1.161	
S1 - short	100k	>500	0.216	80.62	-2999.87	209.071	no sin. osc.
S2 - open	100k	>500	0.023	-117.67	-2999.91	171.753	no sin. osc.
S2 - short	1040	8.3	374.1	45.05	-1.147	0.914	
S3 - open	100k	>500	0.091	-93.06	-2999.53	266.543	no sin. osc.
S3 - short		100			0.		no oscillations
S4 - open	100k	>500	0.018	-92.74	-2999.91	270.629	no sin. osc.
S4 - short	100k	>500	59.52	-6.31	398.077	45.526	no sin. osc.
S5 - open	890	7.3	3.259	74.36	0.003	2.918	
S5 - short	100k	>500	43.05	71.75	-16.101	109.583	no sin. osc.
S6 - open	890	7.3	20.76	81.64	-0.036	1.339	
S6 - short	100k	>500	45.95	68.30	18.849	107.222	no sin. osc.
S7 - open		100			0.		no oscillations
S7 - short	310	67.7	476.3	105.40	-12.934	134.391	
S8 - open	100k	>500	0.033	-90.37	-2999.91	281.203	no sin. osc.
S8 - short	100k	>500	0.051	-91.73	-2999.9	284.390	no sin. osc.
S9 - open	100k	>500	0.092	-93.11	-2999.51	266.616	no sin. osc.
S9 - short	100k	>500	0.155	-91.80	-2999.75	210.601	no sin. osc.
S10 - open	100k	>500	0.008	-71.64	-2999.91	384.349	no sin. osc.
S10 - short	100k	>500	0.430	-97.77	-2170.95	263.349	no sin. osc.

Table 2 Simulation with real switch model – Fault dictionary

Defect	fosc [Hz]	δfosc [%]	Ampl. 1st. har. [mV]	Phase 1st. har. [deg]	DC val. [mV]	THD [%]	comments
FF	960	-	266.6	-125.45	-0.218	0.353	
S1 - open	727.3	24.2	52.67	-152.95	-0.195	0.541	
S1 - short	100k	>500	0.291	82.61	-2999.84	221.73	no sin. osc.
S2 - open	670	30.2	6.073	7.47	0.078	1.386	
S2 - short	1028	7.1	374	133.07	1.966	1.754	
S3 - open	680	29.2	305.3	101.60	-0.509	0.29	
S3 - short		100			0		no oscillations
S4 - open	680	29.2	109.7	-166.00	-0.399	0.300	
S4 - short	100k	>500	59.65	-6.35	398.039	45.352	no sin. osc.
S5 - open	930	3.1	120.2	47.64	-0.105	0.857	
S5 - short	100k	>500	43.16	71.59	-16.221	109.513	no sin. osc.
S6 - open	930	3.1	95.39	45.16	-0.070	0.872	
S6 - short	100k	>500	45.84	68.44	18.737	107.305	no sin. osc.
S7 - open	733	23.6	0.019	1.00	-0.007	4.535	
S7 - short	310	67.7	478.5	107.40	-12.276	133.594	
S8 - open	670	30.2	79.09	-158.37	-0.421	0.554	
S8 - short	100k	>500	0.042	-91.93	-2999.9	273.155	no sin. osc.
S9 - open	680	29.2	318.3	22.08	-0.370	1.067	
S9 - short	100k	>500	0.513	-92.00	-2998.75	227.005	no sin. osc.
S10 - open	680	29.2	258.1	-165.77	-0.063	1.139	
S10 - short	100k	>500	0.421	-97.95	-2171.09	263.529	no sin. osc.

By comparison of Table I and Table II we may get a notion on the quality of the model of the switch used. The main difference between Table I and Table II is in the number of feed-trough fault effects. In addition, as can be seen for the case S7-open, the change of the circuit functionality due to the ideal model, leads to a wrong conclusion about the fault effects, while both models cover the fault. The realistic fault model is mostly suppressing this effect and this is why we do recommend it for this application. Note its simplicity.

By inspection of Table I and Table II we may conclude that there are no untestable faults. The fault effects being different, all faults may be recognized at the output of the cell making OBT a successful concept for testing this kind of cells while using an extremely simple additional circuitry for the synthesis of the oscillator circuit.

We want to stress here again that only one testing point was used and only one measurement is undertaken - the output voltage waveform was measured. The additional processing (FFT) is unavoidable in order to get the oscillation frequency so that the numbers depicted in Table I and Table II are obtained with no additional cost and effort.

5. CONCLUSION

Implementation of the OBT is a challenging issue. It comes from the fact that the method was originally proposed based on presumptions that the active elements exhibit ideal performances. That is not the case. In this proceeding we demonstrate the proper implementation of OBT for the case of a second-order notch cell. This cell may be considered as the best representative (among other second order cells) for the task we undertook, since it is the most complicated and is the most frequently used one. It was synthesized to be implemented as an integrated circuit with switched capacitors. Since the number and the nature of the possible faults if large we are attacking the problem in several phases, one of them being reported here. Only catastrophic faults of the switches were modeled and corresponding fault dictionary was created. It was shown that full coverage of the selected faults may be achieved if proper modeling of the operational amplifiers is used and proper feed-back circuit is synthesized. The results reported here are parts of a project run for a longer period in which we started with continuous time analog filter cells and we are here ending with switched capacitor filter cell.

Acknowledgement. *This research was partly funded by The Ministry of Education and Science of Republic of Serbia under contract No. TR32004.*

REFERENCES

[1] M. Soma, "Automatic test generation algorithms for analogue circuits", IEE Proc. Circuit, Devices and Systems, Vol. 143, No. 6, December 1996, pp. 366-373.

[2] C. Dufaza and H. Ihs, "A BIST-DFT technique for DC test of analog modules", *Journal of Electronic Testing- Theory and Applications*, Vol. 9, No. 1-2, 1996, pp. 117-133.

[3] M. Marlett and J. Abraham, "DC-IATP: An iterative analog circuit test generation program for generating DC single pattern tests", International Test Conference, 1988, pp. 839-845.

[4] L. Milor and V. Viswanathan, "Detection of catastrophic faults in analog integrated circuits", *IEEE Transactions on Computer Aided Design*, Vol. 8, 1989, pp 114-130.

[5] M. Slamani and B. Kaminska, "Multifrequency analysis of faults in analog circuits", *IEEE Design & Test of Computers*, Vol. 12, No. 2, 1995, pp. 70-80.

[6] C. Wang, Y. Yun, H. Liang, J. He, M. Chan, "Multi-frequency Test for analog circuits," Electron Devices and Solid-State Circuits (EDSSC), IEEE International Conference, June 2013, pp. 1, 2, 3-5.
[7] S. Huynh, S. Kim, M. Soma and J. Zhang, "Automatic Analog Test Signal Generation Using Multifrequency Analysis", I*EEE Transactions on Circuits and Systems—II: Analog and digital signal processing*, Vol. 46, No. 5, May 1999, 565-576.
[8] B. Burdiek, "Generation of optimum test stimuli for nonlinear analog circuits using nonlinear programming and time-domain sensitivities," Proc. of Design, Automation and Test in Europe, Conference and Exhibition, 2001, pp. 603-608.
[9] Z. Guo and J. Savir, "algorithm-based fault detection of analog linear time-invariant circuits", Proc. of IEEE Instrumentation and measurement technology conference, Budapest, Hungary, May 2001, pp. 49-54.
[10] S. Cherubal and A. Chatterjee, "Parametric fault diagnosis for analog system using functional mapping", Proc. of IEEE DATE, Nice, France, 1999, pp. 195-200.
[11] V. Prasannamoorthy and N. Devarajan, "Time domain technique for fault diagnosis of analog circuits with flexible accuracy algorithm", *Eur. Journal of Scientific Research*, Vol. 51, No. 2, 2011, pp. 211-221.
[12] K. Arabi and B. Kaminska, "Oscillation-test strategy for analog and mixed-signal integrated circuits", Proc. of the 14th IEEE VLSI Test Symposium (VTS'96), Princeton, New Jersey, April/may 1996, pp. 476-482.
[13] A. Halder and A. Chatterjee, "Automated test generation and test point selection for specification test of analog circuits," Proc. of 5th International Symposium on Quality Electronic Design, 2004, pp. 401-406.
[14] G. Hu, H. Wang, M. Hu and S. Yang, "Oscillation test strategy for analog filters by monitoring output voltage and supply current" *Thinghua Science and Technology*, Vol. 12, No. S1, 2007, pp. 78-82.
[15] P. Alli, *Testing A CMOS Operational Amplifier Circuit Using A Combination Of Oscillation And Iddq Test Methods*, M.Sc. Thesis, Louisiana State University, USA, 2004.
[16] M. Wong and K. Ko, "Fault diagnostic improvement method for OTM-based testing", Proc. of 17th IEEE Instrumentation and Measurement Technology Conf., 2000, Baltimore, MD, USA, pp. 1118 – 1123.
[17] S. Yellampalli, A. Srivastava, and V. Pulendra, "A Combined Oscillation, Power Supply Current and IDDQ Testing Methodology for Fault Detection in Floating Gate Input CMOS Operational Amplifier", Proc. of the 48th Midwest Symp. on Circuits and Systems, Covington, KY, Aug. 2005, pp. 503 - 506.
[18] Prasad, V.C.; Babu, N.S.C., "Selection of test nodes for analog fault diagnosis in dictionary approach", *IEEE Transactions on Instrumentation and Measurement*, Vol. 49, No. 6, Dec. 2000, pp. 1289-1297.
[19] C. Yang, S. Tian, and B. Long, "Application of Heuristic Graph Search to Test-Point Selection for Analog Fault Dictionary Techniques", *IEEE Trans. on Instrumentation and Measurement*, Vol. 58, No. 7, 2009, pp. 2145-2158.
[20] K. Arabi and B. Kaminska, "Efficient and accurate testing of analog-to-digital converters using oscillation-test method", Proc. of the European Design and Test Conference (ED&TC 97), Paris, France, March 1997, pp. 384-352.
[21] K. Arabi and B. Kaminska, "Oscillation-test methodology for low-cost testing of active filters", *IEEE Trans. on Instrumentation and Measurements*, Vol. 48, No. 4, August 1999, pp 798-806.
[22] M. Milić, M. Stošović and V. Litovski, "Oscillation based analog testing – a case study", In Proceedings of the 34th International Conference on Information and Communication Technology, Electronics and Microelectronics MIPRO 2011, Opatija, Croatia, 2011, vol. 1, pp. 118-123.
[23] M. Stošović, M. Milić and V. Litovski, "Analog filter diagnosis using the oscillation based method", *Journal of Electrical Engineering*, ISSN 1335-3632, Vol. 63, No. 6, 2012, pp. 349–356.
[24] M. Stošović, M. Milić, M. Zwolinski and V. Litovski, "Oscillation-based analog diagnosis using artificial neural networks based inference mechanism", *Computers and Electrical Engineering*, Vol. 39, 2013, pp. 190-201.
[25] A. Chaehoi, Y. Bertrand, L. Latorre and P. Nouet, "Improving the Efficiency of the Oscillation-based Test Methodology for Parametric Faults", LATW'03, 4th IEEE Latin American Test Workshop, Natal, Brazil, 2003.
[26] A. Raghunatan, H. Shin and J. A. Abraham, "Prediction of analog performance parameters using oscillation based test", Proc. 22nd IEEE VLSI Test Symp., Apr. 2004, pp. 377-382.
[27] A. Raghunatan, J. H. Chun, J. A. Abraham and A. Chatterjee, "Quasi-Oscillation Based Test for Improved Prediction of Analog Performance Parameters", Proc. of the ITC'04, International Test Conference 2004, pp. 252-261.
[28] K. Suenaga, E. Isern, R. Picos, S. Bota, M. Roca and E. García-Moreno, "Application of Predictive Oscillation-Based Test to a CMOS OpAmp", *IEEE Transactions on Instrumentation and Measurement* Vol. 59 , Issue 8, 2010., pp. 2076-2082.
[29] E. Romero, M. Costamagna, G. Peretti and C. Marques, "A performance Evaluation of Oscillation Based Test in Continuous Time Filters", *International Journal of Mechanical, Industrial Science and Engineering* Vol. 8, No. 1, 2014, pp 196-201.

[30] M. S. Sankari. and P. Sathish Kumar, "Oscillation Test Methodology for Built-In Analog Circuits", *International Journal Of Computational Engineering Research*, IJCER, Vol. 2, Issue No.3, 2012, pp. 868-877
[31] M. S. Zarnik, F. Novak and S. Macek, "Design of oscillation-based test structures of active RC filters. *IEE Proceedings, Circuits, Devices and Systems*, 2000, Vol. 147, No. 5, pp. 297–302.
[32] M. Wong, "On the issues of oscillation test methodology", *IEEE Transactions on Instrumentation and Measurement*, 2000, Vol. 49, No. 2, pp. 240–245.
[33] S. Hurst, *VLSI Testing: Digital and Mixed Analogue/Digital Techniques*, Institution of Engineering and Technology (IET), UK, 1999.
[34] M. S. Zarnik, F. Novak and S. Macek, "Efficient go no-go test of active RC filters", *International Journal of Circuit Theory and Applications*, 1998, Vol. 26, No. 5, pp. 523–529.
[35] U. Kač and F. Novak, "All-pass SC biquad reconfiguration scheme for oscillation based analog BIST", Proc. of the 9th European Test Symposium, Ajaccio, France, 2004, pp. 133-138.
[36] U. Kač and F. Novak, "Oscillation Test Scheme of SC Biquad Filters Based on Internal Reconfiguration", *Journal of Electron. Test*, vol. 23, no. 6, pp. 485-495, December 2007.
[37] U. Kač and F. Novak, "Reconfiguration Schemes of SC Biquad Filters for Oscillation Based Test", *Information Technology and Control*, vol.42, no. 1, pp. 38-47, 2013.
[38] G. Huertas, D. Vazquez, E. J. Peralias, A. Rueda and H. L. Huertas, "Practical Oscillation-Based Test of Integrated Filters", *IEEE Design & Test of Computers*, Vol. 19, No. 6, 2002, pp. 64-72.
[39] K. Martin and A. Sedra, "Effect of the OpAmp Finite Gain & Bandwidth on the Performance of Switched-Capacitor Filters", *IEEE Trans. Circuits Syst.*, vol. CAS-28, no. 8, pp. 822-829, Aug 1981.
[40] J. Náhlík, J. Hospodka, P. Sovka and B. Pšenička, "Implementation Of A Two-Channel Maximally Decimated Filter Bank Using Switched Capacitor Circuits", *Radioengineering*, Vol. 22, No. 1, April 2013, pp. 167-173.
[41] M. Robson and G. Russell, "A digital method for testing embedded switched capacitor filters", In Proceedings of the conference on European design automation, EURO – DAC '96/ EURO – VHDL '96, pp. 239–244.
[42] M. Milić and V. Litovski, "Soft defects testing in Notch SC filters using the oscillation method", In Proc. of the LVII ETRAN Conf., Zlatibor, Serbia, 2013, pp. EL 2.3.
[43] M. Milić and V. Litovski, "Testing Capacitors' Hard Defects in Notch SC Filters Using the Oscillation Method", In Proc. of the 5th Small System Simulation Symposium, SSSS 2014, Niš, Serbia, pp. 30-36.
[44] P. E. Allen and D. R. Holberg, *CMOS Analog Circuit Design*, 2nd ed., Oxford University Press, New York, USA:, 2002.
[45] F. H. Ironns, *Active filters for integrated circuits applications*, Artech House, Norwood, MA, USA, 2005.
[46] P. E. Fleischer, and K. R. Laker, "A Family of Active Switched Capacitor Biquad Building Blocks", Bell System Technical Journal, No. 58, December 1979, pp. 2235-2269.
[47] -, LT Spice User Manual, http://www.intactaudio.com/forum/viewtopic.php?t=596.
[48] C. Chalk, M. Zwolinski, and B. R. Wilkins, "Test Stimulus Generation for Steady-State Analysis of Analogue and Mixed-signal Circuits", Proc. of the 3rd IEEE International Mixed Signal Testing Workshop,1997, pp. 85-92.
[49] P. Kabisatpathy, A. Barua and S. Sinha, *Fault diagnosis of analog integrated circuits*, Springer, Dordrecht, The Nederland, 2005.
[50] S. Mosin, "A built-in self-test circuitry based on reconfiguration for analog and mixed-signal IC." *Information Technology and Control*, 2011, Vol. 40, No. 3, pp. 260-264.
[51] G. Hu, H. Wang, M. Hu and S. Yang,, "Oscillation test strategy for analog filters by monitoring output voltage and supply current," *Thinghua Science and technology*, Vol. 12, No. SI, July 2007, pp. 78-82.
[52] B. Kaminska, "Analog and mixed signal test", in: *EDA for IC system design, verification, and testing*, CRC Press, Taylor&Francis Group, London, 2006.
[53] Litovski, V., Zwolinski, M., *"VLSI Circuit Simulation and Optimization"*, Chapman and Hall, London, 1997.
[54] -, Linear ethnology,
[55] http://www.linear.com/designtools/software/?gclid=CK_dzsaKnL4CFQbMtAod2AkARg#LTspice