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A SYSTEM-ON-CHIP 1.5 GHz PHASE LOCKED LOOP REALIZED USING 40 nm CMOS TECHNOLOGY

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Abstract. *This work presents the design and realization of a fully-integrated 1.5 GHz sigma-delta fractional-N ring-based PLL for system-on-chip (SoC) applications. Some design optimizations were conducted to improve the performance of each functional block such as phase frequency detector (PFD), voltage-controlled oscillator (VCO), filter and charge pump (CP) and so as for the whole system. In particular, a time delay circuit is designed for overcoming the blind zone in the PFD; an operational amplifier-feedback structure was used to eliminate the current mismatch in the CP, a 3rd LPF is used for suppressing noises and a current overdrive structure is used in VCO design. The design was realized with a commercial 40 nm CMOS process. The core die sized about 0.041 mm2. Measurement results indicated that the circuit functions well for the locked range between 500 MHz to 1.5 GHz.*

Key words: *PLL, blind zone, current mismatch, ring oscillator*

1. INTRODUCTION

Phase-locked loops (PLLs) are widely used in modern digital and communications systems for frequency synthesis, clock generation, retiming, clock signal recovery, etc. [1-6]. With fractional-N feature, variable frequency clocks can be generated for the operation of different communication and digital sub-systems in a mixed signal system-on-chip (SoC) design. To meet some specific system requirements, a PLL was usually realized with analog charge pump, LC oscillator, loop filter with large component values which require large silicon area and non-standard digital/analog CMOS fabrication process [3, 6-7]. This work presents one fully integrated, fractional-N, PLL design solution based solely on a commercial 40 nm CMOS process without much significant performance trade-off.

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Figure 1 shows the system block diagram of a fractional-N PLL. It consists of a phase frequency detector (PFD), charge pump (CP), low-pass filter (LPF), voltage-controlled oscillator (VCO) and multi-modulus divider (MMD) for sigma-delta modulation. The whole structure is configured as a negative feedback system that can keep track with the output signal frequency, f_{out}, with the reference frequency, f_{ref}. If there is a difference in frequency or phase, the PFD will output control pulses UP and DN which are fed into a charge pump for converting into a single end current. A low-pass filter will filter out the high-frequency components and output a DC voltage for the VCO control. That is, the VCO voltage is proportional to the phase error between the f_{ref} and VCO output frequency, f_{out}, or its fraction as divided by the MMD. A generalized transfer function for describing this feedback system is given by

$$H(s)=\frac{\frac{I_{CP}}{2\pi}H_{LPF}(s)\frac{K_{VCO}}{s}}{1+\frac{I_{CP}}{2\pi}H_{LPF}(s)\frac{K_{VCO}}{s}\frac{1}{N}} \tag{1}$$

where $I_{CP}/2\pi$ is the current generated by charge pump per phase angle; $H_{LPF}(s)$ is the transfer function of low-pass filter. K_{VCO}/s is the transfer function of VCO; and $1/N$ represents the frequency division for fractional-N operation.

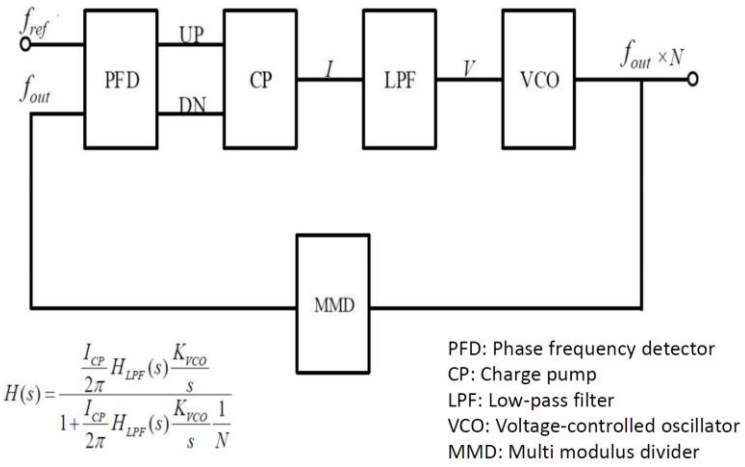


Fig. 1 Major constitutions of a fractional-N PLL.

The system performance is governed by various characteristics of the building blocks. The blind zone of PFD and the mismatch of control currents of the charge pump will cause the VCO to output incorrect signal frequency and cause a large phase noise in the PLL [8-13]. High-order active filter would lead to a better loop and high-order harmonics suppression. However, it may be costly for implementation and conventional integrated PLLs often put the filter as an external component which allows user to have custom designs. The characteristics of VCO will greatly affect the overall performance of PLL

[7]. Within the constraint of given design rules, available component types and values of target 40 nm CMOS process, we designed a fully integrated fractional-N PLL with some special circuit configurations. In PFD circuit, conventional D-type flip-flop based phase detector circuit configuration [14] was used where we introduced a delay line with approximately 280ps delay to eliminate the blind zone [14]. In CP circuit, with reference to some recently reported configuration [9-12], a feedback mechanism constituted by an opamp was established in order to tract with the UP and DN currents. To suppress noises of system, a 3rd order passive LPF was used. In VCO circuit, IO device was used to control the ring oscillator. Preliminary results of this design has been reported in Ref.[15]. This paper presents further detailed analysis on the circuit configuration, results, circuit constraints and methodologies for further performance improvement.

2. Design Methodologies

2.1. Phase Frequency Detector

Phase frequency detector (PFD) which generate a pulse output is proportional to the phase difference between the input and output frequencies/phases [4, 12]. In this work, we construct the PFD using the conventional D-type flip-flop based circuit which is typical in a commercial PLL design [14]. Figure 2(a) gives the specific circuit of PFD. The D flip-flops make the PFD be sensitive to the rising edges of f_{ref} or f_{out} only. In connection with the charge pump (CP), the high output of the top D flip-flop enables the UP current of the charge pump; whereas the output of the lower D flip-flop enables the DN current. At the rising edge of the reference signal f_{ref}, the UP signal changes from 0 to 1. It may remain even after the rising edge of feedback signal f_{out} which changes the DN output from 0 to 1 also. At this point, both signals are fed into the AND gate which resets UP and DN signals simultaneously. This results in a blind zone for UP and DN signal. Blind zone will make the CP be insensitive to a small phase errors and results in a large phase noise of the PLL. Thus, measure to eliminate the blind zone needs to be introduced. Here we introduce a delay line (DL) of about 280 ps in order to eliminate the blind zone. With this configuration, DN will be reset for a period of DL after the UP signal and that eliminates the blind zone. The detailed operation of this circuit could be understood with the aid of the state diagram given in Fig. 2(b). Figure 2(b) highlights the three states of the UP and DN signal generation for the PFD. When a rising edge of f_{out} detected, there is a positive transition from the CP. When the system starts up, the PFD is in the "State 0" (UP = 0, DN = 0). When a rising edge of f_{ref} comes up, PFD changes from "State 0" to "State 1" (UP = 1, DN = 0). If a rising edge of f_{out} comes, the PFD will go back to "State 0"; and if there is another rising edge of f_{ref} detected, the PFD will keep at "State 1". When the system is at "State 0" with a rising edge of f_{out}, the PFD will go into "State 2" (UP = 0, DN = 1). At this point, if a rising edge of f_{ref} comes up, it will switch back to "State 0". However, if a second rising edge of f_{out} detected, the PFD will keep at "State 2".

2.2. Charge Pump

The control signal UP and DN generated by the phase detector are fed into charge pump (CP) to control the current flows in the charge pump so as to produce a single current which will be further converted into a voltage for the VCO control via the low-

pass filter. The total charge, Q_{CP}, is proportional to the durations of UP and DN signals, namely

$$Q_{CP} = I_{UP}T_{UP} - I_{DN}T_{DN} \tag{2}$$

where I_{UP} and I_{DN} are the UP and DN current, respectively, T_{UP} and T_{DN} are the pulse duration of UP and DN control in CP, respectively.

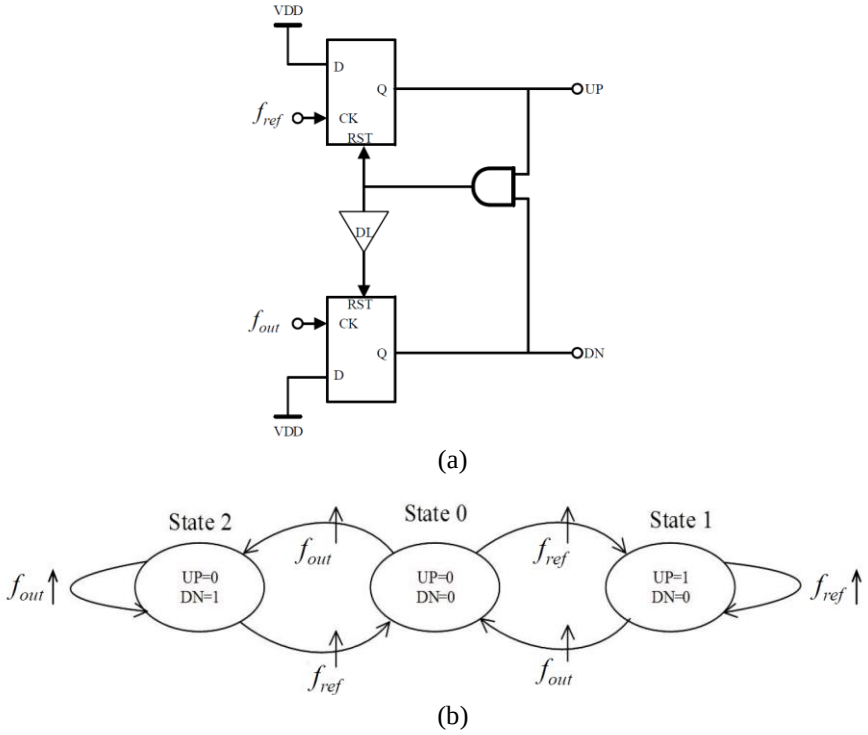


Fig. 2 (a) Schematic of phase frequency detector; and (b) state diagram showing the operation flow of the phase frequency detector.

In ideal case, I_{UP} is always equal to I_{DN}. In real case, the currents may be different due to device mismatch, charge injection, clock feedthrough, channel-length modulation and etc. [8-13]. This issue becomes even worse in nano CMOS circuits as channel length modulation will be more significant. To eliminate the mismatch between UP and DN current, several circuit configurations such as drain-switching charge pump, current steering charge pump, source-switching charge pump and cascade current source charge pump were proposed [8-13]. In our work, we incorporate a comparator to keep UP and DN current to track each other. As shown in Fig. 3, the drains of M1 and M3 are tied to the noninverting and inverting input of the op amp, respectively, which will make the drain voltage of M1 and M3, and then M2 and M4, be equal. It can be readily shown that both UP current ($I_{D,\ \mathrm{M3}}$) and DN current ($I_{D,\ \mathrm{M4}}$) are equal and are both governed by the mirror current of I_{bias}. They will not be affected by the output voltage, channel length modulation or size mismatch of the transistors.

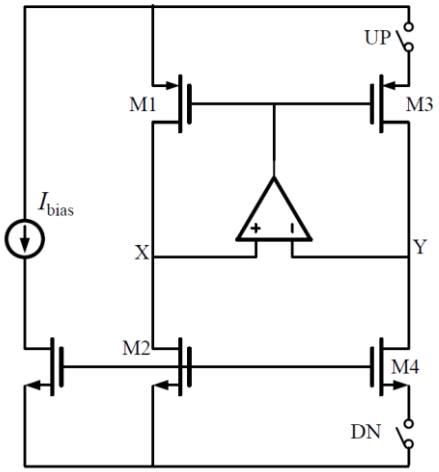


Fig. 3 Schematic of the CP structure with a feedback path constituting by an operational amplifier to keep track with the UP and DN currents.

2.3. Low-Pass Filter

As shown in Fig.1, the low-pass filter (LPF) shapes the error current for VCO control. It governs the damping factor and natural frequency of the system. For sake of flexibility and to save the chip area, most of commercial PLLs often put the LPF as externally-connected circuit and allow the maximum flexibility for specific circuit application design. For SoC applications, this work implements the LPF with on-chip components and it does not treat filter as a tunable building block. To keep a reasonable system performance, simple, third order, passive RC filter shown in Fig. 4 is used. Processes for determining the component values are given in Appendix A.

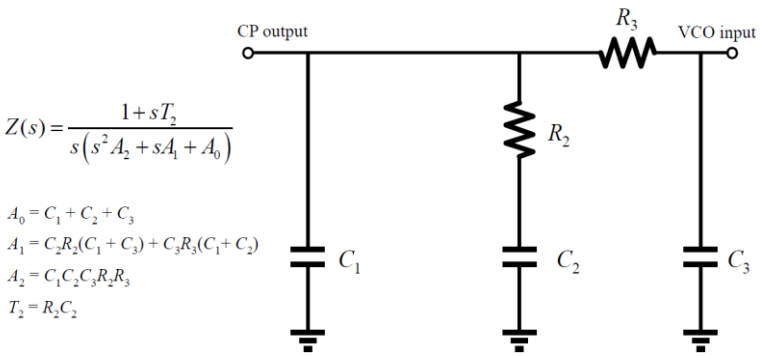


Fig. 4 Schematic of the low-pass filter circuit used in this work.

2.4. Voltage Control Oscillator

Voltage control oscillator is one of the most important building block governing the performance of the PLL. The key performances of concern include:

(a) Frequency tuning range: It determines the operation range of the PLL.
(b) Tuning gain: Expressed in terms of V/Hz, indicates the change in voltage level as the frequency change. It governs the overall gain of the whole system.
(c) Phase noise level: The phase noise level of the VCO is of particular importance in some applications such as used as a frequency synthesizer. It affects the stability of the system and is the major jitter source.

Many advanced VCO circuit configurations based on RC or LC structures have been proposed [1-3, 7]. In most of the high-performance oscillators and PLLs, LC structures are always favorable. However, a high-quality factor inductor requires a thick metal layer for implementation which is not available in most of the CMOS process. It requires a large silicon area also. RC based oscillator also requires a large chip area and there are constraints in high-frequency operation also. Ring-based VCO has poor frequency stability, large phase noise and they are more vulnerable to power and temperature fluctuation [7]. In addition, it was difficult to achieve very high frequency operation and is seldom used in any high-performance PLL. The advantages of the ring-based VCO is that it is simple in circuit design. It is simply built with some cascaded inverters. Ring oscillator is very compact and can be realized with any CMOS process. With the available of nano CMOS technology and some digital circuit techniques, high-performance and high-frequency ring-based PLLs have been obtained [6]. Another area that makes the ring-based PLL be more attractive is the need of low-cost and readily available PLL for full CMOS system integration and SoC applications. Ring-based VCO together with the nano CMOS technology do provide a low-cost implementation of PLL with reasonable performance. In present design, because of the available 40 nm gate length devices, high-speed operation can be readily obtained. Performance of the circuit is still acceptable with such simple VCO design as will be demonstrated later. In our design, we implemented the VCO with a five-stage CMOS inverters. To achieve a higher operation frequency and better stability, the circuit is over-driven with large size IO MOSFET, M1, which operates at high analog supply voltage AVDD of 2.5V. As shown in Fig. 5, being biased at 2.5V, M1 would produce a larger control current so as to generate a higher oscillation frequency. It also reduces the effects

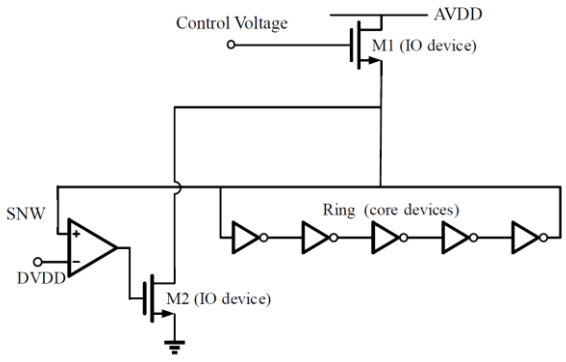
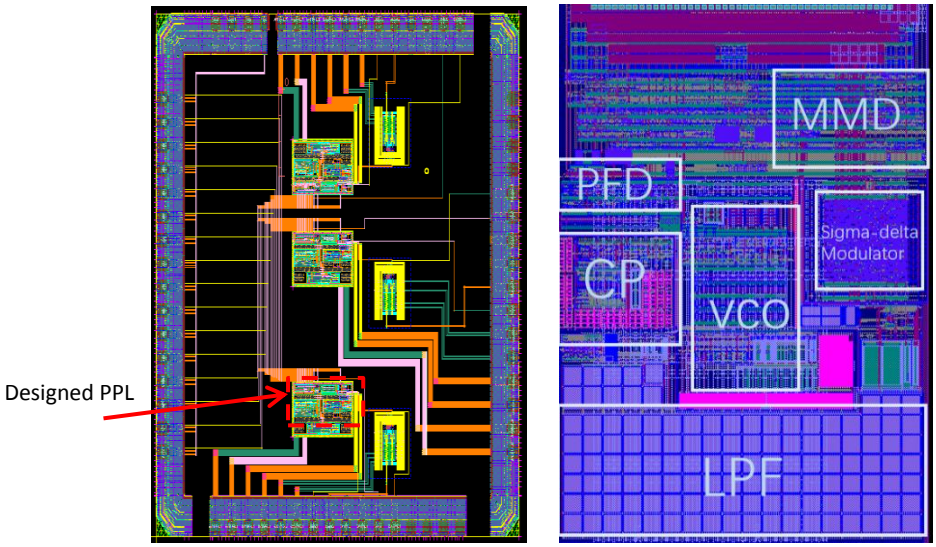


Fig. 5 Schematic of a five-stage voltage control ring oscillator with current overdrive.

due to supply voltage, temperature, and process parameter fluctuations. Note that the core ring oscillator, constituted by the five-stage inverters, was operated at digital supply voltage with DVDD = 1.1 V. To protect the VCO output SNW not to exceed DVDD, an operational amplifier OP and level limiter M2 were used. If SNW exceeds DVDD, transistor M2 will be turned on so as to lower the SNW voltage level to a value equal to DVDD.

3. Testing and Validating

We have realized the designed PLL with a commercial 40 nm CMOS process. Because such short-gate length transistors are available, high-frequency operation can be readily obtained. The layout of the design is shown in Fig. 6. Major building blocks, PFD, CP, LPF, VCO, MMD, sigma-delta modulator are highlighted. The chip size of core functional block (excluding pads and IOs) is about 250 μm × 165 μm or 0.041 mm^2.which is half size of the latest digital fractional-N PLL realized using 65 nm technology [6]. The circuit is operated with both digital and analog supply voltages of 1.1 V and 2.5 V, respectively. The locked range of the chip in from 500 MHz to 1.5 GHz. The overall power consumptions are 1.5 mW and 2.8 mW at 750 MHz and 1.5 GHz, respectively.



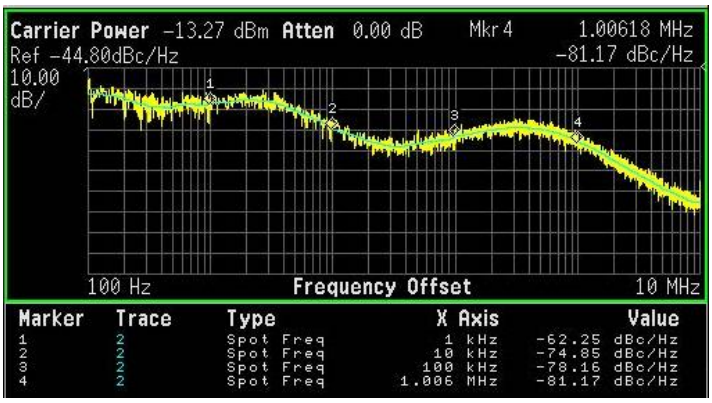
(a) (b)

Fig. 6 (a) Layout of a system chip with embedded PPL designed in this work; (b) Layout of designed PLL. The size of the chip is 250 μm×165 μm or 0.041 mm^2.

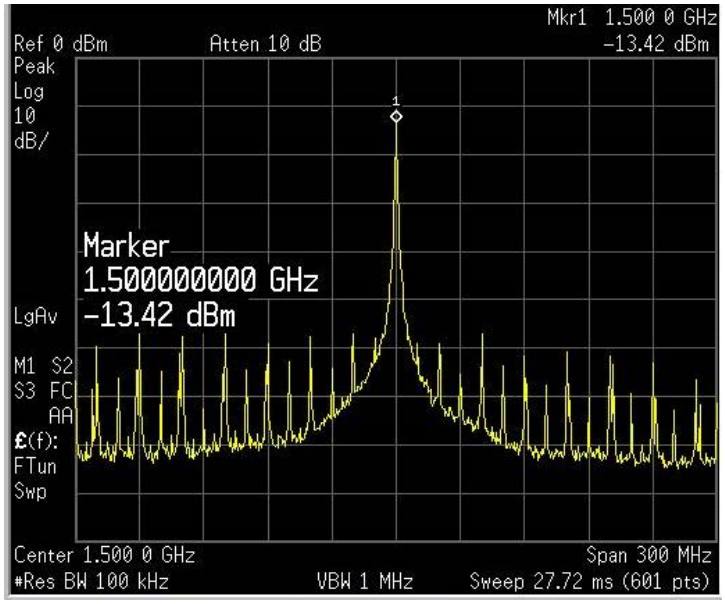
It can be seen that although the low-pass filter is rather simple from the circuit configuration point of view, it occupies the largest portion of chip area for realizing the few passive capacitive and resistive components. Compared to other SoC designs, the chip area of LPF is larger because the use of third order filter. The size of VCO is comparatively compact because the use of ring oscillator structure and minimum size inverters.

The preliminary testing results of the fabricated PLL chip are shown in Fig.7. Figure 7(a) shows the measured output phase noises for the VCO output at 1.5 GHz. The low-frequency (1 kHz) and high-frequency (1 MHz) noise level are -62 dBc/Hz and -81 dBc/Hz, respectively. Figure 7(b) depicts the output spectrum of VCO at 1.5 GHz with 300 MHz frequency span. The peak value 13.42 dBm and a number of spurious peaks at various frequencies such as ±20, ±30, ±40, ±50 MHz and their multiples are found. The sources of the spurs should be due to the clock frequency of signal source and the power line frequency as well. The characteristics are not very good as compared with other integrated PLLs [6]. However, when the operation frequency is lowered, better characteristics are found. Figure 8 plots the phase noise levels as a function of VCO frequency. Phase noise is smaller for smaller value of fractional N. At 500 MHz, the 1 kHz phase noise reduces to -71 dBc/Hz. The phase noises increase as the frequency goes up. In general, the low-frequency noise levels, less than -62 dBc/Hz, are acceptable for a ring-based PLL in some general applications. The high-frequency phase noises are less than -81 dBc/Hz for all investigated VCO frequencies. In addition, the time domain jitter noise was also measured. Fig.9 plots the root-mean-square value of jitter noise as function of oscillator frequency. The peak value was about 13 ps at 500 MHz. The jitter noise levels are smaller at other frequencies.

Figure 10 plots the output amplitude as a function of VCO frequency. As shown in Fig. 10, the output amplitude was -8.6 dBm when the output is set to 500 MHz, it decreases as the frequency increases. Figure 11 shows the change of primary spurs (at 20 MHz) for various VCO frequencies. The spur amplitude is less than -64 dBm for 500 MHz center frequency and the largest spur was found for 1.2 GHz output spectrum. The levels of spurs in our PLL are high and needs to be suppressed. Although it does not directly show up in the present measured data, one can readily anticipate that the performance of the LPF and VCO could be one of the major sources for the characteristics degradation of the system. These are the major performance trade-off for the compact and simple design in the sense of SoC applications. The loop dynamic of the present design could not be adjusted with the fixed LPF components and the loop gain may be lowered because of the losses in the parasitic passive components. In addition, the integrated capacitors used usually have large leakage current because of the use of ultrathin dielectric. This is even worse in the 40 nm technology. As a consequence, the constant DC level for the low-voltage VCO is hard to maintain at the LPF output and that causes some undesirable frequency drifts of VCO. Hence further improvement should focus on the LPF design such as the use of active filter to reduce the chip size and yet to suppress the effect of gate leakage. Yet the second issue needs special attention is stability of VCO against power supply and temperature fluctuations. Ring oscillator was known to have poor power supply and temperature stability. In the 40 nm technology, the digital power supply voltage (DVDD) has been scaled down to 1.1 V. The low supply voltage makes the ring-based VCO more sensitive to supply voltage and temperature fluctuation. Here we use the IO devices for driving and level limiting with operation voltage of 2.5 V (AVDD). It should help in alleviating these effects. Further experimental validation and detailed characterization are under investigation.



(a)



(b)

Fig. 7 Phase noise characteristics and output spectrum of the ring-based VCO in the fabricated PLL operated at 1.5 GHz: (a) phase noise; and (b) output amplitude response.

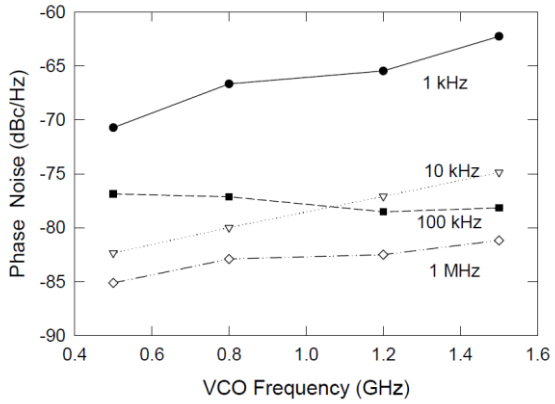


Fig. 8 Plot of measured phase noise of VCO output at different frequencies.

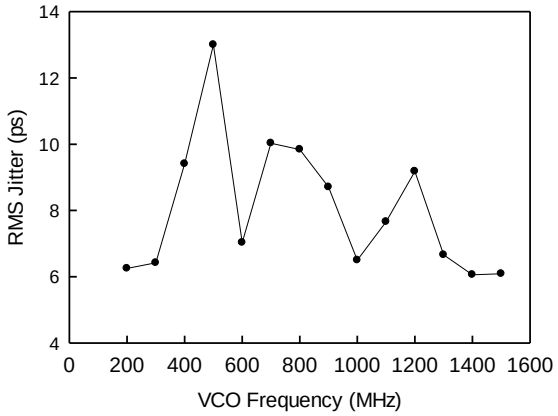


Fig. 9 Measured root-mean-square value of jitter for the whole frequency range of the VCO.

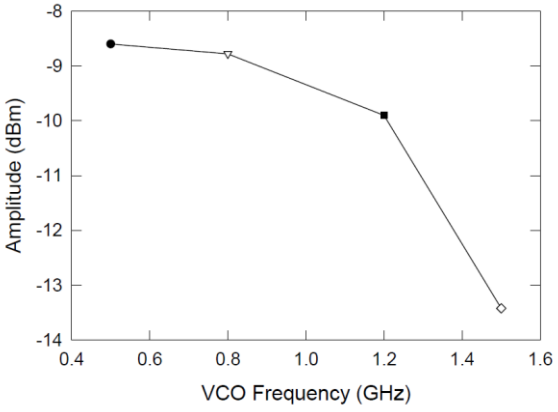


Fig. 10 Peak amplitudes of the VCO running at different frequencies.

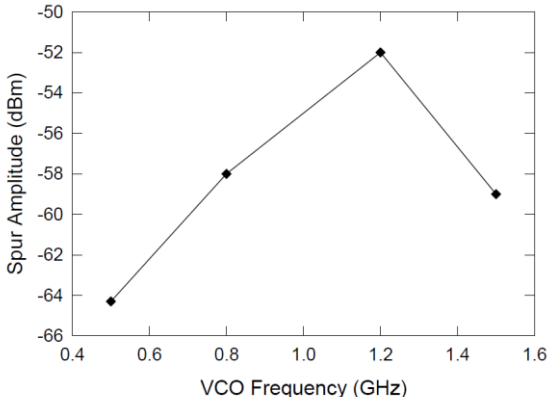


Fig. 11 Levels of primary spur observed at the VCO's output.

4. CONCLUSION

In this work, a fully-integrated compact CMOS Fractional-N PLL was designed and realized. We adopted various strategies for most of the key functional blocks so as to improve the overall performance of the PLL. In particular, a time delay circuit was introduced to the phase detector for overcoming the blind zone in control signal generation; the charge pump characteristics was improved by using an operational amplifier to mirror the UP and DN currents so as to alleviate the effects of current mismatch and channel length modulation of short-channel devices. The major strategy in performance, cost and technology trade-off is the use of a five-stage ring-based VCO in the design. A current overdrive structure was introduced by using IO device and analogue supply voltage which allow a better frequency range and alleviate the possible degradations due to power supply and temperature fluctuations. The design is compact in size and has been realized with a 40 nm CMOS process. Measurement results indicated that the circuit functions well for the locked range between 500 MHz to 1.5 GHz.

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APPENDIX A

According to Fig. 1, the LPF transfer function is defined as the change in voltage at the tuning port of the VCO divide by the current level from the charge pump. For 3rd LPF given in Fig. 4, the transresistance function is:

$$Z(s) = \frac{1 + sT_2}{s(s^2 A_2 + sA_1 + A_0)} \tag{A1}$$

where $A_0 = C_1 + C_2 + C_3$, $A_1 = C_2R_2(C_1 + C_3) + C_3R_3(C_1 + C_2)$, $A_2 = C_1C_2C_3R_2R_3$, and time constant for zero $T_2 = R_2C_2$.

By expressing the transfer function in terms of poles and zeroes, we have:

$$Z(s) = \frac{1 + sT_2}{sA_0(1 + sT_1)(1 + sT_3)} \tag{A2}$$

where poles T_1 and T_3 are given, respectively, by $T_1 = C_1C_2R_2/(C_1 + C_2)$, $T_3 = R_3C_3$.

The phase margin can be readily determined from (A2) with:

$$\phi = 180^{\circ} + \tan^{-1}(\omega_C T_2) - \tan^{-1}(\omega_C T_1) - \tan^{-1}(\omega_C T_3) \tag{A3}$$

By setting the derivative of the phase margin to zero, the following relationships can be obtained:

$$C_1 = \frac{A_2}{T_2^2}\left(1 + \sqrt{1 + \frac{T_2}{A_2}(T_2A_0 - A_1)}\right) \tag{A4}$$

$$C_3 = \frac{-T_2^2 C_1^2 + T_2 A_1 C_1 - A_2 A_0}{T_2^2 C_1 - A_2} \tag{A5}$$

Other components can be evaluated with the following equations:

$$C_2 = A_0 - C_1 - C_3 \tag{A6}$$

$$R_2 = \frac{T_2}{C_2} \tag{A7}$$

$$R_3 = \frac{A_2}{C_1 C_3 T_2} \tag{A8}$$