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RESOLVING THE BIAS POINT FOR WIDE RANGE OF TEMPERATURE APPLICATIONS IN HIGH-K/METAL GATE NANOSCALE DG-MOSFET

Sushanta K. Mohapatra, Kumar P. Pradhan, Prasanna K. Sahu

Nanoelectronics Lab., Department of Electrical Engineering,
National Institute of Technology, Rourkela, Odisha India

Abstract. *This article investigates the Zero-Temperature-Coefficient (ZTC) bias point and its associated performance metrics of a High-k Metal Gate (HKMG) DG-MOSFET in nanoscale. The ZTC bias point is defined as the point at which the device parameters are independent of temperature. The discussion includes sub threshold slope (SS), drain induced barrier lowering (DIBL), on-off current ratio (I_{on}/I_{off}), transconductance (g_m), output conductance (g_d) and intrinsic gain (A_V). From the results, it is confirmed that there are two different ZTC bias points, one for I_{DS} (ZTC_{IDS}) and the other for g_m (ZTC_{gm}). The points are obtained as: ZTC_{IDS}=0.552 V and ZTC_{gm} =0.410 V, which will open important opportunities in analog circuit design for wide range of temperature applications.*

Key words: *DG-MOSFETs, HKMG, SCEs, Analog FOMs, ZTC point.*

1. INTRODUCTION

The growing interest and demand in designing circuits that operate at high temperatures which will be used in the military, automobile, nuclear, and some industries need to be analysed in nanoscale. Silicon on Insulator (SOI) based CMOS devices have the potential for the operation at both low and high temperatures. It is desirable to bias the digital and analog circuits designed for high temperature applications at a point where the *V-I* characteristics show little or no variation with respect to temperature. This point is typically known as *ZTC* point [1-5]. Previously, Shoucair [1] and Prijic, et al. [3] have identified the *ZTC* point for a bulk CMOS in both linear and saturation regions for temperatures between 25^0C - 200^0C. Researchers like Groeseneken, et al. [4] and Jeon, et al. [5] have shown the existence of the *ZTC* point for SOI MOSFET's. Osman, et al. [6] presented a systematic analysis of *ZTC* point for partially depleted (PD) SOI MOSFET over a wide range of temperatures (25^0C - 300^0C), and identified two distinct *ZTC* points, in the linear as well as in the saturation region. Tan, et al. [2] identified that the ZTC_{IDS}

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Corresponding author: Sushanta K. Mohapatra
Nanoelectronics Lab., Dept. of Electrical Engineering, National Institute of Technology, Rourkela, 769008, Odisha India
(e-mail: skmctc74@gmail.com)

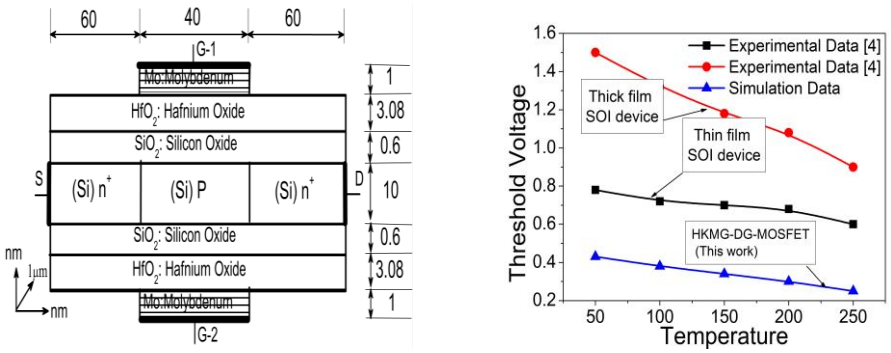
exists in both linear and saturation regions, whereas the ZTC_{gm} lies only in the saturation region for fully depleted (FD), lightly doped, enhanced mode SOI n-MOSFET.

The Double Gate (DG) MOSFET fabricated on SOI wafers is one of the most promising candidates due to its attractive features of low leakage currents, high current drivability (I_{on}) & transconductance (g_m), reduced short channel effects (SCEs), steeper subthreshold slopes, and suppression of latch-up phenomenon [7-10], and also it is a very good option for analog applications [11-14]. Hardly any work has been reported to investigate the *ZTC* point for multi-gate technology.

The behaviour of I_D is exactly opposite after a certain V_{GS} with variation in temperatures. This is due to the degradation in mobility or high electric field effect at higher gate bias [2]. As far as we know, this is a unique attempt to investigate the detailed analysis of *ZTC* point over a wide range of temperatures (100 K-400 K) for analog applications of a DG MOSFET with HKMG technology. Various performance metrics of the device have been systematically examined, which includes the SCEs like *SS*, *DIBL*, I_{on}/I_{off} ratio, and some important analog figures of merit (FOMs) such as g_m, g_d, A_v.

2. Device Description and Simulation Setup

In the 2-D numerical simulation, a symmetric device structure as shown in Fig. 1(a) has been modelled. The silicon channel is covered above and below by oxide layers as gate stack (GS) of equivalent oxide thickness (EOT) having 1.1 nm. Metal gate work function is considered as 4.6 eV. The channel length is 40 nm with a fixed width of 1 μm has been considered. Source and drain extensions are 60 nm with contacts vertically placed (S and D, respectively). The doping profile for channel (p-type 1×10^{16} cm^{-3}) and source, drain (n-type 1×10^{20} cm^{-3}) are set.



(a) (b)

Fig. 1 (a) Schematic structure of Nanoscale HKMG Double Gate N-MOSFET
(b) Calibration between simulation and experimental data of Threshold voltage as a function of temperature.

The 2-D numerical device simulator ATLAS is employed to simulate the planner DG-MOSFET with high-k/metal gate technology. According to ITRS the drain bias has been fixed at V_{DD} = 1.0 V [15]. To study the analog performance the simulation is performed with

V_{DS} = 0.5 V and V_{GS} = 0 V to 1.0 V. In the simulation, the inversion-layer Lombardi constant voltage and temperature (CVT) mobility model has been used, that takes into account the effect of transverse fields along with doping and temperature dependent parameters of the mobility. The Shockley–Read–Hall (SRH) generation and Auger recombination model are used for minority carrier recombination. The model Fermi-Dirac uses a Rational Chebyshev approximation that gives results close to the exact values. The model Temperature is used for various operating temperature in Kelvin which is varied from 100 K to 400 K.

The interface trapped charges during the pre and post fabrications process are a common phenomenon, and these charges cannot be neglected in nanoscale device fabrication. Presence of trapped charges creates an additional non-linear potential and varying electric field across the gate dielectric. According to (1), the high-k gate stack reduces the electric field across the layer of gate stack due to high permittivity. So a lower electric field will require inducing inversion layer charge as [16].

$$Q_{ch} = \varepsilon_{di} \mathrm{E}_i \tag{1}$$

Where Q_{ch} is inversion charge, ε_{di} permittivity of dielectric and E_i is electric field. Even if, the fixed oxide and interface trapped charge densities are very large, it requires moderate potential across the high-k gate stack layer. Consequently, the reduction of threshold voltage and supply voltages can be maintained at reasonable values. This low electric field promotes gate stack reliability with huge unwanted charges inside. As the device is high-k gate stack, the interface trapped charge effects are included in the simulation. The trapped charge densities are considered at semiconductor to insulator interface. The typical concentration of trapped charges considered in this work is 4×10^{11} cm^{-2} at interface [17]. The electron and hole surface recombination velocity is considered as 1×10^{4} cm/sec. In the simulation all the junctions of the structure are assumed to be abrupt in nature. Furthermore, we have chosen two numerical techniques, Gummel and Newton, to obtain solutions [17]. Fig. 1(b) shows excellent agreement with the nature of threshold voltage between our simulation results and experimental data for a wide range of temperature reported in [4].

3. Results and Discussion

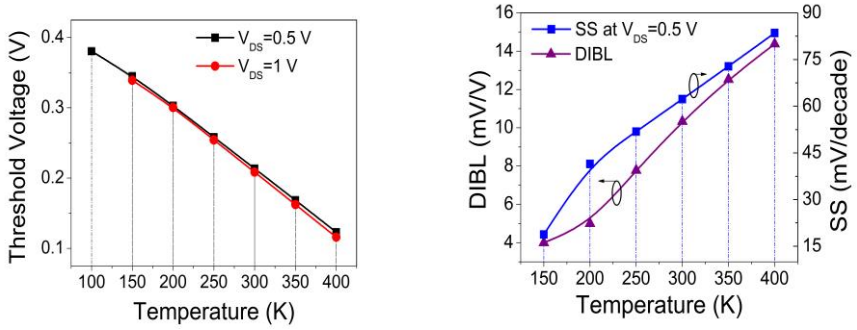
In this section, the device scalability and analog performance metrics are discussed. Threshold voltage (V_{th}), sub-threshold swing (*SS*), DIBL, on-state drive current (I_{on}), off-state leakage current (I_{off}), I_{on}/I_{off} ratio are the important Figures of Merit (FoMs) under device scalability. As far as analog circuits are concerned, the most important parameters are the transconductance (g_m), output conductance (g_d), intrinsic gain (A_V).

Fig. 2(a) and (b) describe all three important SCEs, which include the variation of V_{th}, *SS*, and DIBL for different temperatures. The threshold voltage is determined from I_{DS}–V_{GS} characteristics. It is considered to be that value of the V_{GS} for which the I_{DS} approaches 10^{-6} A/μm at V_{DS} = 0.5 V. The calculation of DIBL is done as per (2).

$$DIBL = \Delta V_{th} / \Delta V_{DS} = (V_{th1} - V_{th2}) / (V_{DS2} - V_{DS1}) \tag{2}$$

The V_{th} is observed at two different drain bias V_{DS1}=0.5 V and V_{DS2}=1.0V. From the Fig. 2(a) and (b), it should be noted that V_{th} is decreasing with an increase in temperature, but the

SS, and DIBL values are decreasing as temperature increases. The typical value for the SS of Multi-gate MOSFET is 60 mV/decade. According to Fig. 2(b), the *SS* value is lowest for T< 300 K (room temperature), then it starts increasing as temperature increases and reaches its typical value at T=300 K. The DIBL value is quite impressive throughout the entire temperature range. As there is a little variation in V_{th} for two different V_{DS} at temperatures from 200 K to 400 K, so the DIBL varies from 5 mV/V to 14.38 mV/V.



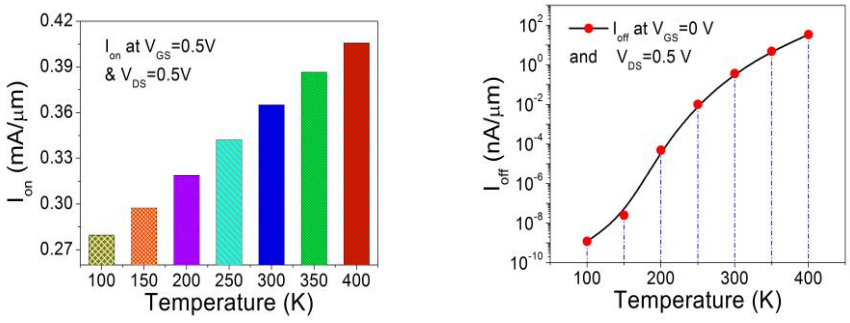
(a) (b)

Fig. 2 (a) V_{th} as a function of temperature for different V_{DS},
(b) *SS* and DIBL as a function of temperature for V_{DS}=0.5 V.

Fig. 3(a) and (b) show the I_{on}, and I_{off} respectively for a wide range of temperature variations at V_{GS}=0.5V and V_{DS}=0.5V. The on state current (I_{on}) is extracted, by calculating the maximum drain current (I_D) from the I_{DS}–V_{GS} characteristics at V_{GS}=0.5 V and V_{DS}=0.5 V. The off state current (I_{off}) is extracted, by calculating the drain current (I_D) at V_{GS}=0 and V_{DS}=V_{DD}. The I_{off} shows a very low value for T< 300 K and then started increasing as temperature increases; this is due to the low *SS* and high V_{th} values at low temperatures. The temperature dependence on the I_D is influence by V_{th} as:

$$I_D(T) \approx \mu(T)[V_{GS} - V_{th}(T)] \tag{3}$$

The temperature dependant $I_D(T)$ is directly related to $\mu(T)$ or V_{GS}–$V_{th}(T)$ term. So, increasing the V_{GS}–$V_{th}(T)$ term causes the $I_D(T)$ to increase because the V_{th} decreases with increase in temperature as shown in Fig. 3(a) and (b).



(a) (b)

Fig. 3 (a) On state current (I_{on}),
(b) Off state current (I_{off}), as a function of temperature for different V_{DS}.

The I_{on}/I_{off} is a very important parameter for switching application; it should be very high for a good switch. According to Fig. 4(a), the I_{on}/I_{off} is 2.30×10^{14} for T=100 K, then it starts falling down as temperature increases and reaches 1.20×10^{4} for T=400 K. At higher temperature regions, the high value of I_{on} because of lower V_{th} and the high value of I_{off} due to the high SS values compensate each other and give rise to nearly constant I_{on}/I_{off}. Fig. 4(b) shows the variation of the I_D and g_m with V_{GS} for different bias temperatures. As per (2), at high gate bias the $\mu(T)$ dominates because at higher T, lattice scattering dominates and causes reduction in the channel mobility, which further reduces the I_D. At low gate bias the V_{GS}–$V_{th}(T)$ term causes the I_D to increase with increasing temperature because a low V_{th} is predicted at higher temperatures. These two opposite effects will cancel each other out at a value of V_{GS} where the I_D shows minimum variation with T. This point is called ZTC bias point. The g_m–V_{GS} plot can be obtained by the derivative of the I_D with respect to the V_{GS}. At $V_{GS}< V_{th}$ (channel is weakly inverted) the I_D is due to diffusion. The diffusion current increases with increase in T due to hike in intrinsic carrier concentration. At $V_{GS} >V_{th}$, g_m will decrease as T increases due to mobility degradation.

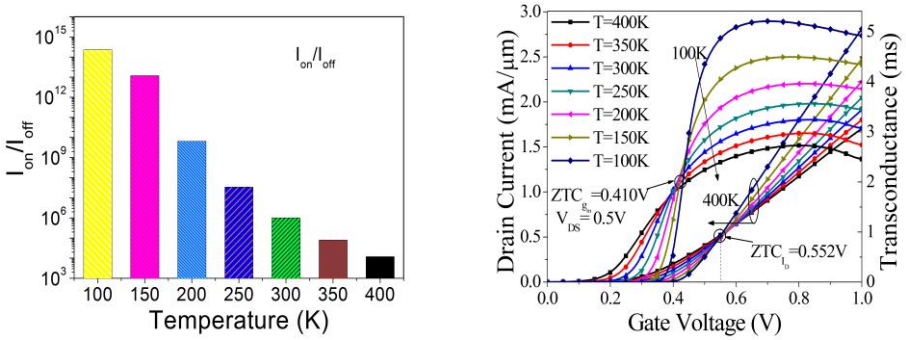
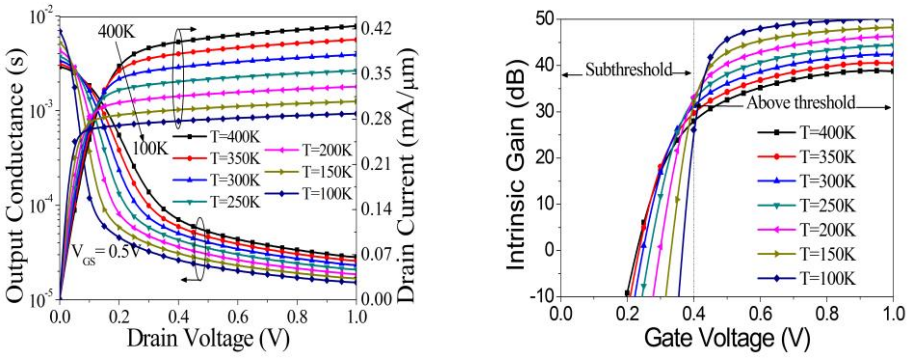


Fig. 4(a) On-off current ratio (I_{on}/I_{off}) as a function of temperature,
(b) Drain current (I_D) and Transconductance (g_m) as a function of V_{GS} for different values of operating temperature.

The reduction in V_{th} with increase in temperature will increase g_m but the reduction of g_m occurs due to degradation of mobility. These two phenomena will compensate each other to give rise to a ZTC bias point for g_m. From the figure we can conclude that the transconductance ZTC point (0.014 V) is lower than the drain current ZTC bias point (0.552 V). The ZTC_{IDS} and ZTC_{gm} bias points are two important measures in analog circuit design. In OPAMP (operational amplifier) design, to maintain constant DC current levels, the devices need to be biased at ZTC_{IDS} points, while input devices can be biased at ZTC_{gm} point to achieve stable circuit parameters.

The simulated output current (I_{DS}) and output conductance (g_d) versus drain bias (V_{DS}) at a V_{GS}=0.5 V for different temperatures are plotted in Fig. 5(a). Because of the above said $\mu(T)$ and V_{th} effects with respect to temperature, the I_{DS} decreases as T increases below the ZTC point and the reverse is happening after the ZTC point for both parameters. The ZTC point for g_d is lower than the output current ZTC point. The intrinsic gain (A_V = g_m/g_d) is a valuable FOM for operational transconductance amplifier (OTA) and it is given in Fig. 5(b). From Fig. 5(b), high gain can be observable for high temperatures in

subthreshold regime and just a reverse effect in above threshold region. From this it can be concluded that the device shows better results in subthreshold regime for higher T and it is a good candidate in above threshold regime for lower T.



(a) (b)

Fig. 5(a) Output current (I_D) and Output conductance as a function of V_{DS} for different values operating temperature,
(b) Intrinsic Gain (A_V) as a function of V_{GS} for the different values operating temperature.

The important performance metrics are tabulated in Table 1. By observing the table, it is clear that our device shows very impressive values in low temperature ranges. The I_{on}/I_{off}, SS and A_V of the device increases as temperature decreases and attains their maximum values for T=100 K.

Table 1 Extracted Parameters for various Temperatures

Temperature in K	I_{on}/I_{off}	DIBL (mV/V)	SS (mV/Decade)	A_v in dB
400	1.20×10^{4}	14.38	83.52	38.780
350	8.08×10^{4}	12.52	72.83	40.514
300	1.02×10^{6}	10.33	62.30	42.402
250	3.45×10^{7}	7.78	51.85	44.355
200	6.50×10^{9}	5.00	41.45	46.311
150	1.19×10^{13}	11.75	18.80	48.248
100	2.30×10^{14}	–	20.87	50.180

4. CONCLUSION

The *ZTC* bias points of the HKMG DG-MOSFET are investigated using the 2-D numerical simulation. The results presented in this work give a detailed idea about the *ZTC* bias point for parameters like I_D, and g_m. These results provided here can serve as a good design tool for designing circuits in a wide range of temperature applications and show promising solutions to minimize temperature degradation of analog circuits. The work identified the distinct *ZTC* points for the device in nanoscale.

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