

A DOUBLE-DIFFERENTIAL-INPUT / DIFFERENTIAL-OUTPUT FULLY COMPLEMENTARY AND SELF-BIASED ASYNCHRONOUS CMOS COMPARATOR

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Abstract: A novel fully complementary and fully differential asynchronous CMOS comparator architecture, that consists of a two-stage preamplifier cascaded with a latch, achieves a sub-100 ps propagation delay for a 50 mV_{pp} and higher input signal amplitudes under 1.1 V supply and 2.1 mW power consumption. The proposed voltage comparator topology features two differential pairs of inputs (four in total) thus increasing signal-to-noise ratio (SNR) and noise immunity through rejection of the coupled noise components, reduced even-order harmonic distortion, and doubled output voltage swing. In addition to that, the comparator is truly self-biased via negative feedback loop thereby eliminating the need for a voltage reference and suppressing the influence of process, supply voltage and ambient temperature variations. The described analog comparator prototype occupies 0.001 mm^2 in a purely digital 40 nm LP (low power) CMOS process technology. All the above mentioned merits make it highly attractive for use as a building block in implementation of the leading-edge system-on-chip (SoC) data transceivers and data converters.

Keywords: Comparator, preamplifier, latch, CMOS, fully-differential, PVT variations, noise immunity, self-biasing, data converters, ADC, transceivers.

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1 INTRODUCTION

After amplifiers, comparators are perhaps the second most widely used analog electronic component. Analog comparators can be used to determine whether one input value is higher or lower than the other one at specific time points (predefined by the clock signal) or to perform the comparisons in an asynchronous manner, that is, to detect the time point at which the difference of the two input signals has changed its sign. These two comparator types are usually classified as dynamic (clocked) comparators and asynchronous (or open-loop), respectively. Further, the compared signal may be any analog physical (i.e., electrical) quantity, like current, voltage, but also charge or even time. This paper settles its contribution in the field of the so-called asynchronous (non-clocked) analog voltage comparators.

Both asynchronous/open-loop [2] and dynamic/synchronous [3] comparator types, are in a widespread use in switched-mode power supplies as well as in the present-day data conversion [4] and/or transmission circuits [5]. After all comparator itself is nothing else but the single-bit analog-to-digital converter (ADC). Often, they are the critical design components as, for example, data converters' bandwidth and maximum (over-)sampling rate directly depend on comparator's propagation delay. Moreover, an analog-to-digital converter's resolution, expressed in terms of signal-to-noise and distortion ratio or effective number of bits, is largely influenced by the comparator's noise figure and its input-referred noise. Finally, on the one hand, comparators should be high speed/low noise, while on the other, for use in battery-powered applications, they should consume as less power as possible.

The basic idea behind high-speed analog voltage comparators is in combination of the best aspects of a preamplifier with the negative exponential step response with a latch that exhibits the positive exponential rise. The

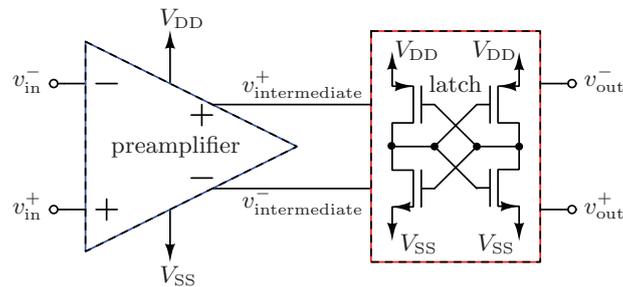


Fig. 1. Fully differential asynchronous voltage comparator that exploits a preamplifier-latch cascade to achieve fast decision making and thereby high operating speeds.

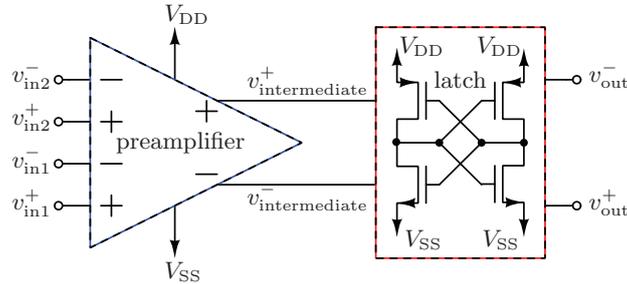


Fig. 2. Fully differential high-speed preamplifier-latch asynchronous voltage comparator that features two pairs of differential inputs (four in total) on the preamplifier.

preamplifier is used to build-up the input voltage difference up to a certain point where the latch takes over and brings the signal to rail. Both clocked and non-clocked comparators can exploit these speed-up principles. A block-level representation of a high-speed asynchronous comparator consisting of a preamplifier-latch cascade is given in Fig. 1.

It is advantageous for high-speed asynchronous voltage comparators to utilize fully differential signaling as it brings with itself increased noise immunity by rejection of the coupled noise components, reduced even-order harmonic distortion, and doubled output voltage swing. Besides using differential output as the one of Fig. 1, the overall noise performance benefits could also be induced from the comparator version of Fig. 2 that features the preamplifier stage with two pairs of differential inputs (four in total).

This article presents a high-speed asynchronous CMOS voltage comparator implementation which exploits two differential pairs of inputs and is suitable for incorporation in the cutting-edge systems on chip (SoCs).

2 FOUR-INPUT ASYNCHRONOUS COMPARATOR TOPOLOGY

Transistor-level and block-level schematics of the proposed complementary and fully differential self-biased asynchronous CMOS voltage comparator that features two pairs of inputs are shown in Fig. 3 and Fig. 4, respectively.

The comparator is comprised out of three fully differential self-biased CMOS voltage amplifiers that share identical circuit topology, and a CMOS latch. Inputs of two amplifiers (four in total) at the same time act as the comparator inputs, while the biasing nodes and respective outputs of these two amplifiers are connected to each other in parallel, thus constituting the first preamplifier stage. The third amplifier is cascaded to the outputs of the first two, hence effectively forming the preamplifier's second stage. The

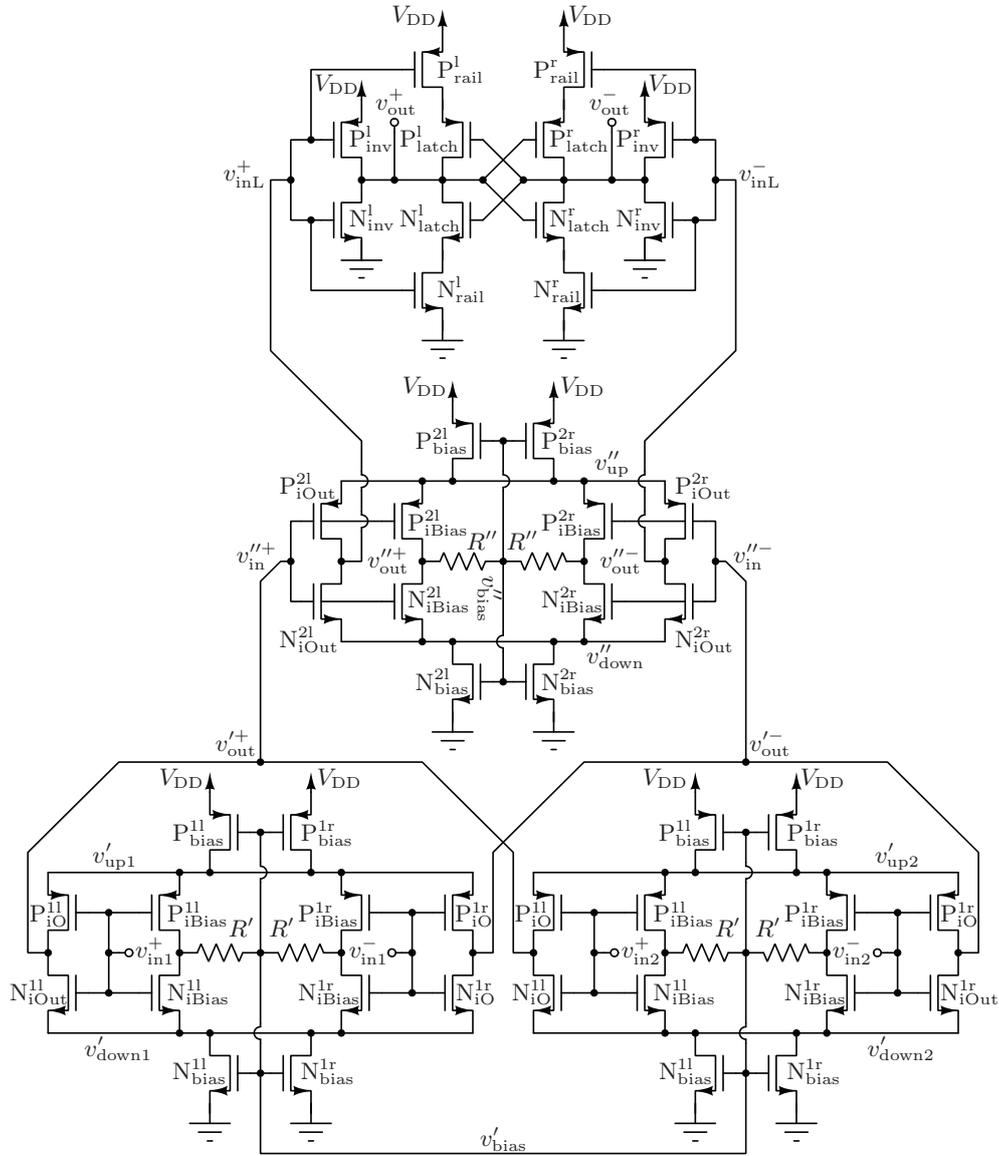


Fig. 3. Transistor-level schematic of the proposed self-biased asynchronous CMOS analog voltage comparator which features two pairs of differential inputs and differential output.

amplifiers constructing the first preamplifying stage are mutually identical (corresponding transistor sizes of both are matched), but are different from the one serving as the second preamplifying stage (meaning, its transistor sizes are optimized independently). Finally, preamplifier is cascaded with a

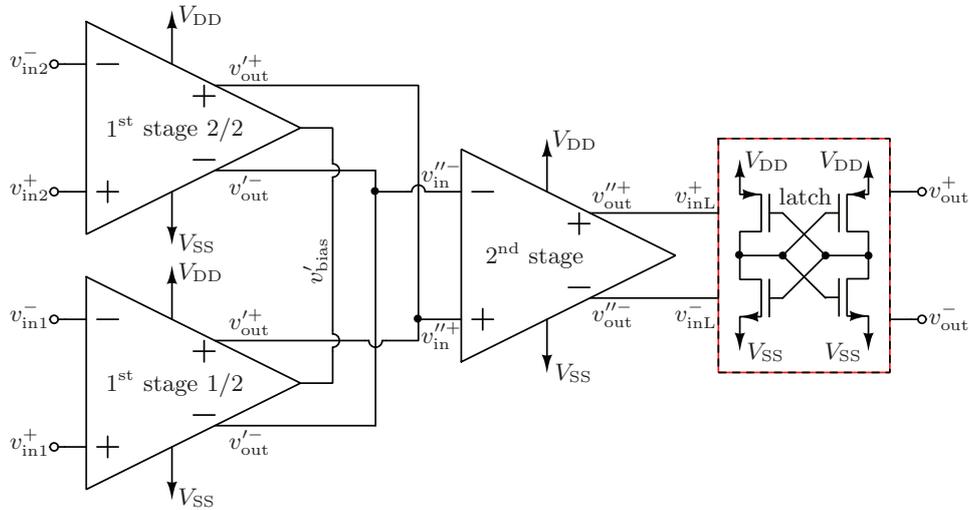


Fig. 4. Block-level schematic of the proposed self-biased asynchronous analog voltage comparator which features two pairs of differential inputs and differential output of Fig. 3.

simple latch whose outputs are at the same time the comparator outputs.

Inputs of each of the three fully differential self-biased inverter-based CMOS amplifiers [5, 6] are amplified through the push-pull inverters consisting of transistors N_{iOut}^{xx} and P_{iOut}^{xx} , thus rendering the outputs of that particular amplifier. The CMOS inverters at the inputs bring with themselves inherent advantages like very high input impedance and nominally doubled transconductance. The biasing of each stage is accomplished through complementary transistor pairs N_{bias}^{xx} and P_{bias}^{xx} which are controlled by v_{bias} and are operating deep within the linear region. This potential is in turn stabilized through the negative feedback loop utilizing N_{iBias}^{xx} and P_{iBias}^{xx} . Namely, any variation in processing parameters or operating conditions (change of supply voltage or ambient temperature) that shifts v_{bias} from its nominal value, results in an instant attenuation of these deviations [7] in an extent proportional to the value of the loop gain. As the biasing transistors are operating in the triode region, potentials v_{down} and v_{up} are very close to the negative and the positive supply rail, respectively. In such configuration, self-biasing is not compromising with the output voltage swing which is nearly equal to the difference between the values of the two supply rails.

Resistors R' and R'' serve to avoid establishment of the low-resistive paths through v'_{bias} and v''_{bias} nodes, respectively, for high (by absolute value) input voltage differences. Placed in the biasing part, the resistors have no impact on comparator performance except that it drastically reduces dissipation while mutually distant potentials are applied as comparator inputs.

Problem of the same kind will also occur in the path through $v_{\text{out}}^{\prime+}$ and $v_{\text{out}}^{\prime-}$ nodes but it cannot be avoided using the resistor trick instead these metal lines must be made thicker in order to sustain higher current values.

As already stated, the output of the last preamplifier stage is connected to the input of the latch stage. The latch itself is implemented as the cross-coupled connection of two CMOS inverters (composed out of transistors N_{latch}^x and P_{latch}^x). The coupling between the preamplifier's output and the latch itself is done through inverters consisting of transistors N_{inv}^x and P_{inv}^x . Without transistors N_{rail}^x and P_{rail}^x , the coupling inverters should be large/strong enough to have the ability to pull the latch out of the positive feedback saturation, but still small/weak enough not to firmly dictate the output voltage (because having a latch in that case is senseless). Connecting these four field-effect transistors to the supply rails relaxes the last requirement and consequently increases design's reliability and robustness.

Besides being fully complementary, the proposed asynchronous voltage comparator circuit with two pairs of inputs is also perfectly symmetrical with respect to the vertical and the horizontal axis in Fig. 3 and Fig. 4, respectively. This is the reason why the biasing transistors on each preamplifier stage are drawn separately. Symmetry implies beneficial repercussions on the process of laying the circuit out, as one can naturally match paired devices and the propagation delay through separate circuit blocks.

3 CIRCUIT ANALYSIS OF THE COMPARATOR ARCHITECTURE

Analysis of the proposed comparator topology can be accomplished by analyzing two of its subcomponents, namely the preamplifier and the latch.

3.1 Preamplifier

If the voltage drops across the biasing transistors are neglected, that is, if v_{down} and v_{up} are approximately at the supply rails, then the small-signal differential gain of the comparator's preamplifier is just equal to the transfer function of the push-pull inverter and hence it can be written as

$$\frac{V_{\text{out}}^{\prime+} - V_{\text{out}}^{\prime-}}{(V_{\text{in}1}^+ - V_{\text{in}1}^-) - (V_{\text{in}2}^+ - V_{\text{in}2}^-)}(s) = H_{\text{preamplifier}}(s) = \frac{R_o' R_o'' (s - g_m' / C_{gd}') (s - g_m'' / C_{gd}'')}{R_o' R_o'' \zeta s^2 + \left[R_o' (C_{gd}' + C_{gd}'' (1 + g_m'' R_o'')) + C_{i2o1} \right] + R_o'' (C_{gd}'' + C_L)} s + 1, \quad (1)$$

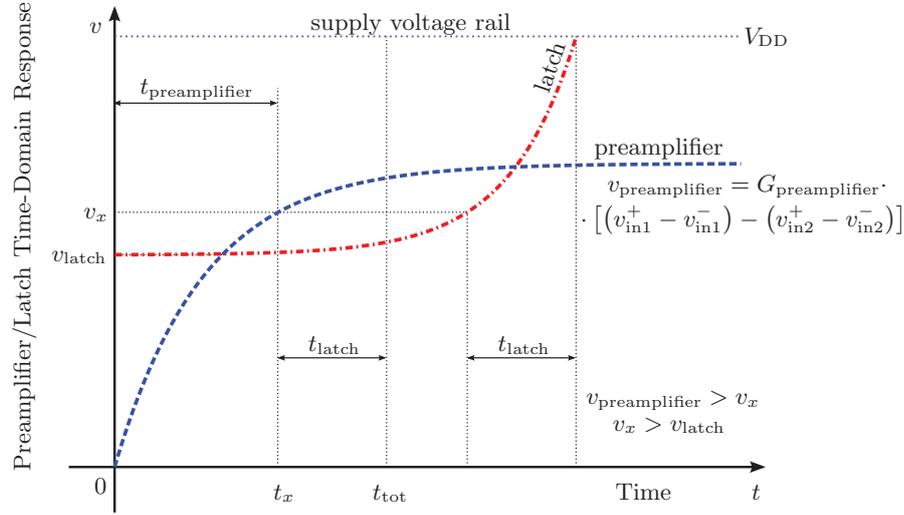


Fig. 5. Combination of the preamplifier negative exponential step response (dashed line) with the positive exponential initial condition time response of the latch (dash-dotted line). At optimum point (t_x, v_x) , which is at the same time the preamplifier-latch takeover point, the first derivatives of the two curves are the same. This minimizes preamplifier-latch cascade propagation delay $t_{\text{total}} = t_{\text{preamplifier}} + t_{\text{latch}}$ and makes the combined output signal quicker which implies fast decision making of the proposed asynchronous comparator.

where $g'_m = g'_{mN} + g'_{mP}$ and $g''_m = g''_{mN} + g''_{mP}$ are the total transconductances of the first and the second preamplifier's stage inverter, respectively, R'_o and R''_o are the total resistances seen at the output of the first and at the output of the preamplifier's second stage, $C'_{gd} = C'_{gdN} + C'_{gdP}$ and $C''_{gd} = C''_{gdN} + C''_{gdP}$ are the sums of the gate-drain capacitances of the nMOS and pMOS of the first and the second preamplifier's stage, respectively. For simplicity reasons, $\zeta = C_L (C'_{gd} + C''_{gd} + C_{i2o1}) + C''_{gd} (C'_{gd} + C_{i2o1})$ is introduced, while C_{i2o1} is the total capacitance at the output of the first and the input of the second preamplifier stage and C_L is the total load capacitance at the output of the preamplifier or at the input of the latch.

It may be observed that the transfer function (1) in which $s = \sigma + i\omega$ is the complex angular frequency, is of the second order with two real left complex half-plane poles. It also possesses two real high frequency right complex half-plane zeroes at frequencies $z_1 = g'_m/C'_{gd}$ and $z_2 = g''_m/C''_{gd}$.

The step response of the preamplifier can be predicted based on its transfer function. If the effect of the two high frequency zeroes, z_1 and z_2 is neglected, together with the dominant pole approximation, the system's step

response may be written as

$$\begin{aligned} v_{\text{out}}''^+(t) - v_{\text{out}}''^-(t) &= \mathcal{L}^{-1} \{H_{\text{preamplifier}}(s)/s\} \approx \\ &\approx G_{\text{preamplifier}} [(v_{\text{in1}}^+ - v_{\text{in1}}^-) - (v_{\text{in2}}^+ - v_{\text{in2}}^-)] [1 - \kappa \exp(-t/\tau_A)] u(t) , \end{aligned} \quad (2)$$

where $G_{\text{preamplifier}}$ and τ_A are the preamplifier low frequency gain and time constant which is inversely proportional to the value of the dominant pole, κ is a constant dependent on coefficients of the polynomial found in the transfer function denominator, while $u(t)$ and \mathcal{L}^{-1} represent the Heaviside step function and the inverse Laplace transform operator, respectively.

3.2 Latch

If the initial voltage that is applied to the latch output nodes (through the preamplifier-latch coupling inverters) at specified time point t' is $v_{\text{out}}^+(t') - v_{\text{out}}^-(t')$, then the time response of the linearized latch approximation on this initial condition (for $t \geq t'$ and $\Delta t = t - t'$) has the form of an exponentially increasing [8] function of time Δt and can be written as

$$v_{\text{out}}^+(t) - v_{\text{out}}^-(t) = \exp(\Delta t/\tau_L) [v_{\text{out}}^+(t') - v_{\text{out}}^-(t')] . \quad (3)$$

The time constant of the portrayed cross-coupled CMOS inverter latch is approximately equal to $\tau_L \approx C/g_{mL}$, where C is the total capacitance seen at the output of the latch, i.e., comparator, while $g_{mL} = g_{mNL} + g_{mPL}$ is the total transconductance of the latch complementary transistor pair. Note that this is a typical temporal response of positive-feedback systems which have a single or a dominant real right complex half-plane pole.

4 OPERATING PRINCIPLES OF THE DESCRIBED COMPARATOR

As already stated in the introduction, the basic idea behind the presented comparator is in combination of the best aspects of the preamplifier, which is characterized by the negative exponential step response (2), with the positive exponential response (3) latch. The preamplifier builds up the voltage up to a certain point where the latch takes over and brings the signal to a rail.

The previous principle concepts are illustrated in Fig. 5. In this figure, the preamplifier gain times the input voltage alone is not sufficient for the output to reach the rail. Nevertheless, it achieves a high enough output value to pull the latch out of one saturation state and trigger its positive feedback loop that drives the comparator to the saturation state on another supply rail, thus producing a firm logical level (high or low) at the output.

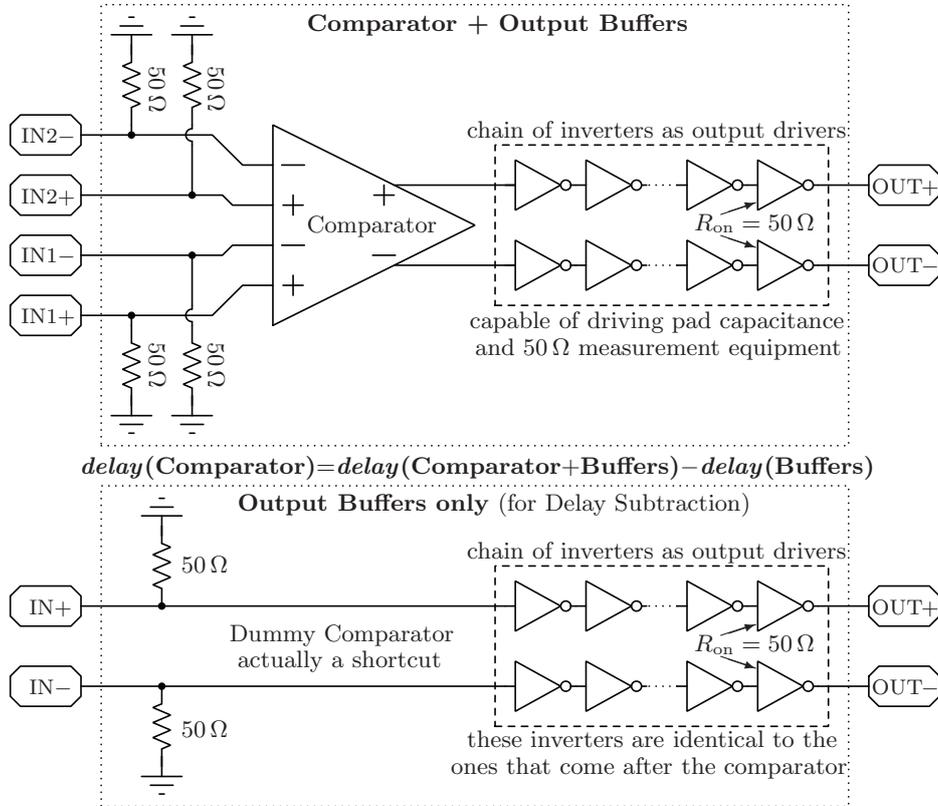


Fig. 6. On-chip comparator structure with output buffers and the corresponding dummy comparator structure used for exact extraction of the comparator's propagation delay.

With the total propagation delay through the comparator being the sum of propagation delays of the cascaded components it consists of, namely,

$$t_{\text{total}} = t_{\text{preamplifier}} + t_{\text{latch}} \quad , \quad (4)$$

it is obvious that reducing the time constants of the separate comparator subcircuits (τ_A and τ_L) is essential to increase its speed of operation. Additionally, it can be proven that there exists the optimum preamplifier-latch takeover point (t_x, v_x) that is located in the point where the first derivatives of the preamplifier and the latch function are equal. This was somewhat expected and hence for high-speed applications the comparator should be optimized such that the subcomponent function that has larger first derivative of the two is used for the corresponding part of the characteristics.

Apart from acceleration, another role of the latch block is also to align comparator's complementary output fall-time and rise-time edges.

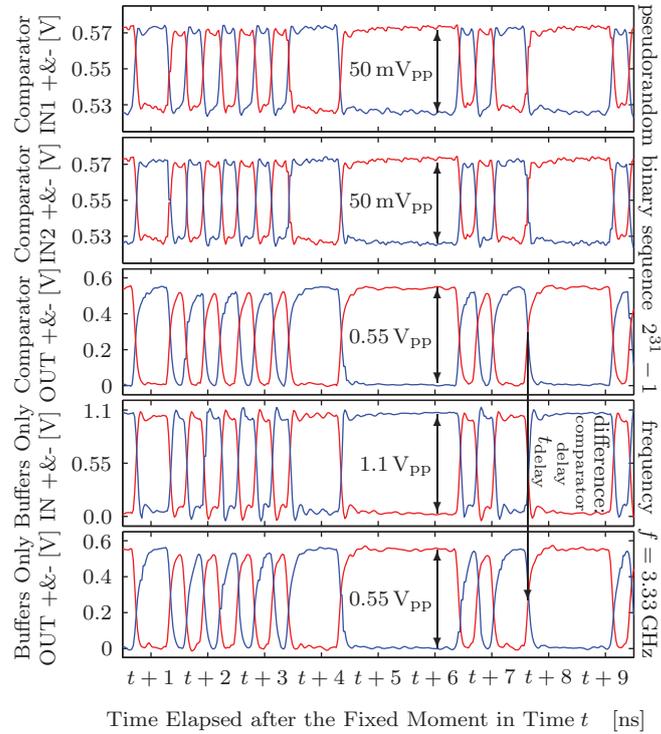


Fig. 7. Measured inputs and outputs of the on-chip structure containing asynchronous voltage comparator featuring two pairs of differential inputs with output drivers and the corresponding on-chip dummy comparator structure containing the output drivers alone.

5 ON-CHIP MEASUREMENT SETUP FOR PROPAGATION DELAY

The output of the latch, which is at the same time the comparator output, has rail-to-rail swing and is hence designed to be cascaded by some digital circuitry which regularly features relatively low input capacitance with respect to a pad capacitances. To measure the comparator characteristics in a realistic configuration a chain of several inverters which drive the pad capacitance and the $50\ \Omega$ measurement equipment follows each of the comparator outputs as shown in Fig. 6. Both transistors in the last inverter are designed to have the on-resistance of $R_{\text{on}} = 50\ \Omega$ to avoid reflection thus halving the output signal amplitude to $V_{\text{DD}}/2$. For the same reason all four inputs have $50\ \Omega$ on-chip termination to ground. To enable indirect delay measurement of the comparator, output drivers are also placed on chip, on their own, as explained by Fig. 6. Special attention is paid so that the metal lines routed to and off the comparator (with the output drivers) and the output drivers alone

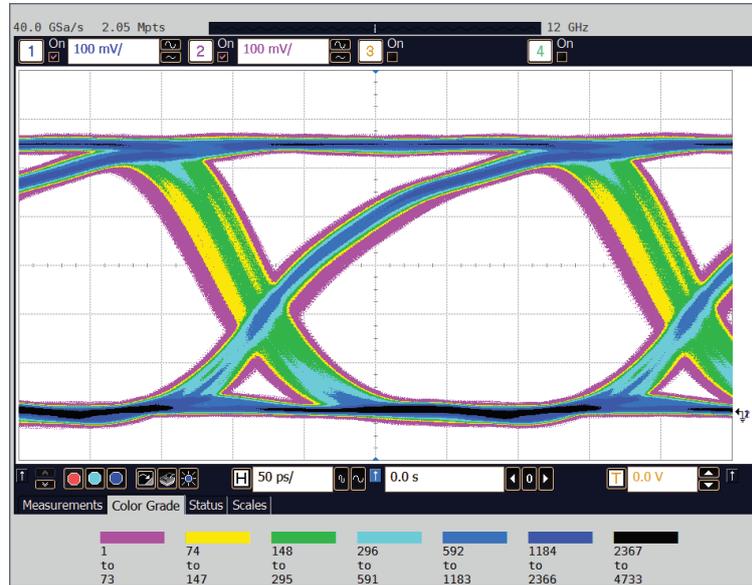


Fig. 8. Oscilloscope display showing an eye pattern for the two comparator outputs that are connected to channels 1 and 2. Input pseudorandom sequence's frequency is 3.33 GHz.

are identical in every aspect. This enabled the use of identical printed circuit boards, identical coaxial cables and finally identical measurement equipment to drive and characterize both on-chip structures. Thus, delay of the comparator is obtained as the difference between the delay of the structure with comparator plus output buffers and the delay of the dummy structure containing the buffers only. The previous subtraction eliminates the influence of coaxial cables, printed circuit board microstrip lines, on-chip metal lines, etc., which were identical for both measurements and are therefore canceled out in the process of delay subtraction. Additionally, the output drivers are optimized for small propagation delay variation, the standard deviation of which is $\sigma(\text{delay}) < 5$ ps based on one thousand Monte-Carlo simulations and the sample of ten relative on-chip measurements. Also, the comparator and the buffers have separate supply pads (i.e., analog and digital, respectively) to enable power consumption measurement of the comparator alone.

Measured inputs and outputs of the on-chip characterization structures depicted in Fig. 6, driven by pseudorandom binary sequence signal with frequency of 3.33 GHz, are shown in Fig. 7 in a form of an oscilloscope screenshot. It can be observed that the structure containing buffers only is always driven with rail-to-rail signal resembling the comparator outputs. Difference between the two outputs yields the comparator propagation delay.

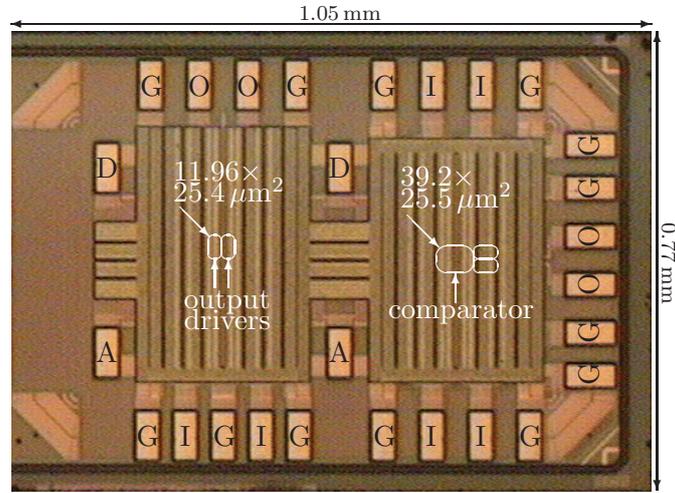


Fig. 9. Test chip photomicrograph. Abbreviations: (G) ground, (A) analog supply, (D) digital supply, (I) input, (O) output. Left – output buffers; Right – four-input comparator.

6 MEASUREMENT RESULTS OF THE PROPOSED COMPARATOR

Having in mind reasonable power consumption, the described comparator is optimized for speed and is fabricated in a standard 1P8M digital 40 nm low power multi-threshold CMOS process technology shrank to 90% (minimum transistor gate length 36 nm). To optimize latency and power the exploited technology offers transistors with three different values of threshold voltage. Threshold voltages for low- V_T transistor types, which are used in the design to minimize propagation delay, are around $V_{Tn}/V_{Tp} \approx 0.33 \text{ V}/-0.28 \text{ V}$, while the nominal supply voltage for the given process is $V_{DD} = 1.1 \text{ V}$.

The propagation delay of the comparator with two pairs of inputs, measured in the upper described manner, is lower than 100 ps for the 50 mV_{pp} step applied at both of its differential inputs. Total power dissipation of the comparator under these circumstances equals 2.1 mW and is dominated by the preamplifier's static consumption. Ergo, the DC current consumption accounts for the major part of the total comparator's power consumption.

Measured eye diagram of the comparator at 3.33 GHz, what was the limit of stimulus equipment, is shown in Fig. 8, however, based on the propagation delay measurements, the eye opening should be present up to 10 GHz.

Test chip photomicrograph is given in Fig. 9. Our proposed four-input comparator design implementation occupies an area of $39.2 \times 25.5 \mu\text{m}^2$.

7 CONCLUSIONS

The article presents a prototype of a novel fully differential asynchronous comparator topology that features two-pairs of inputs and is implemented in 40 nm LP CMOS technology. The comparator consists of a preamplifier-latch cascade and is completely self-biased thus overcoming the need for a reference circuit and reducing the influence of PVT variations. Comparator propagation delay is extracted using subtractive method which exploits on-chip dummy output driver structures. Measurements indicate that, depending on the actual input signal amplitude and common-mode, the comparator can operate at frequencies beyond 10 GHz under dissipation of 2.1 mW. Although both comparator delay and its power consumption greatly depend on the input signal amplitude and common-mode value, this still places it among the fastest non-clocked comparators published up to date. Finally, the proposed comparator circuit is well-suitable for implementation in the cutting-edge system-on-chip (SoC) data transceivers and data converters.

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