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DEMANDS FOR SPIN-BASED NONVOLATILITY IN EMERGING DIGITAL LOGIC AND MEMORY DEVICES FOR LOW POWER COMPUTING

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Abstract. *Miniaturization of semiconductor devices is the main driving force to achieve an outstanding performance of modern integrated circuits. As the industry is focusing on the development of the 3nm technology node, it is apparent that transistor scaling shows signs of saturation. At the same time, the critically high power consumption becomes incompatible with the global demands of sustaining and accelerating the vital industrial growth, prompting an introduction of new solutions for energy efficient computations.*

Probably the only radically new option to reduce power consumption in novel integrated circuits is to introduce nonvolatility. The data retention without power sources eliminates the leakages and refresh cycles. As the necessity to waste time on initializing the data in temporarily unused parts of the circuit is not needed, nonvolatility also supports an instant-on computing paradigm.

The electron spin adds additional functionality to digital switches based on field effect transistors. SpinFETs and SpinMOSFETs are promising devices, with the nonvolatility introduced through relative magnetization orientation between the ferromagnetic source and drain. A successful demonstration of such devices requires resolving several fundamental problems including spin injection from metal ferromagnets to a semiconductor, spin propagation and relaxation, as well as spin manipulation by the gate voltage. However, increasing the spin injection efficiency to boost the magnetoresistance ratio as well as an efficient spin control represent the challenges to be resolved before these devices appear on the market.

Magnetic tunnel junctions with large magnetoresistance ratio are perfectly suited as key elements of nonvolatile CMOS-compatible magnetoresistive embedded memory. Purely electrically manipulated spin-transfer torque and spin-orbit torque magnetoresistive memories are superior compared to flash and will potentially compete with DRAM and SRAM. All major foundries announced a near-future production of such memories.

Two-terminal magnetic tunnel junctions possess a simple structure, long retention time, high endurance, fast operation speed, and they yield a high integration density. Combining

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nonvolatile elements with CMOS devices allows for efficient power gating. Shifting data processing capabilities into the nonvolatile segment paves the way for a new low power and high-performance computing paradigm based on an in-memory computing architecture, where the same nonvolatile elements are used to store and to process the information.

Key words: *digital spintronics, SpinFET, SpinMOSFET, spin-transfer torque, STT, spin-orbit torque, SOT, MRAM, in-memory computing*

1. INTRODUCTION

Continuous miniaturization of complementary metal-oxide semiconductor (CMOS) devices is enabling the unprecedented increase of speed and performance of modern integrated circuits. Numerous outstanding technological challenges have been resolved on this exciting path. Among the most crucial technological achievements implemented by the semiconductor industry within the last 15 years to boost CMOS performance while maintaining the gate control over the semiconductor channel are the introduction of strain [1], high-k gate dielectrics and metal gates [2], and three-dimensional (3D) tri-gate transistor architecture [3],[4], [5]. While chips with 5nm technology based on nanosheets are already nearing production [6], the semiconductor industry is now focusing on a 3nm technology node. Although setting limits for scaling has proven to be a mere meaningless task in the past, it is obvious that the conventional transistor scaling is showing signs of saturation. To sustain the growing demand for high performance small area central processing units (CPUs) and high-capacity memory needed to handle an increasing information flow, the introduction of a disruptive technology employing new computing principles is anticipated. Most importantly, any emerging technology must be energy efficient. Indeed, a harmful active power penalty already prevents the clock frequency from increasing in CMOS circuits and is saturated at approximately 3.7 GHz with the possibility to be boosted for a short time up to 4.2 GHz under heavy load in high-end consumer-level workstation CPUs. Although the transistor size has been scaled down, the load capacitance value per unit area remained approximately unchanged, which keeps the on-current approximately constant for maintaining appropriate high speed operation due to the unavoidable charging of this capacitance.

In addition, small transistor dimensions lead to rapidly increasing leakages. A rapid increase of the stand-by power due to transistor leakages at small transistor dimensions, as well as of the dynamic power and the need to refresh the data in dynamic random access memory (DRAM), is becoming a pressing issue. The microelectronics industry is facing major challenges related to power dissipation and energy consumption, and the scaling of silicon semiconductor devices will soon hit a power wall.

An attractive path to mitigate the unfavorable trend of increasing power at stand-by is to introduce nonvolatility in the circuits. The development of an electrically addressable nonvolatile element, which combines fast operation, simple structure, and high endurance, is essential to mitigate the increase of the stand-by power and the power needed for data refreshment. Nonvolatile elements also enable instant-on architectures without the need of data initialization when going from a stand-by to an operation regime. Recently, a fruitful cooperation between Intel and Micron resulted in bringing a nonvolatile memory to the market, which is based on a three-dimensional X-point cross-bar architectural solution [7]. Although the physics principle of operation has not been officially released, there is a

consent within the community that, as a phase-change memory, it is based on a resistance change due to the phase transition. Although being nonvolatile, the phase-change memory requires a high power to write information as compared to other nonvolatile memories, for example, resistive RAM.

Oxide-based resistive RAM (RRAM) exploits filamentary switching between the on/off states and is thus intrinsically prone to significant resistance fluctuations in both states. In addition, the endurance reported is only slightly better than that of flash memory. Although RRAM possesses a simple structure and a large on/off current ratio, it is premature to consider RRAM at its current stage of development for digital applications. Since continuous conductance modulation is suitable for implementing analog synaptic weights, both filamentary and non-filamentary switching RRAM types are currently intensively investigated, particularly for neuromorphic applications [8].

To be competitive with the traditional volatile technologies and also with nonvolatile flash, emerging nonvolatile devices must offer a fast switching time and high integration density supported by good scalability. In addition, emerging nonvolatile memory must possess a long retention time, a high endurance, and a low write power. At the same time, it must exhibit a simple structure to reduce fabrication costs and must be compatible with CMOS to benefit from advantages provided by outstandingly well-developed CMOS fabrication technology.

Traditional CMOS technology is based entirely on the electron charge. Another intrinsic characteristic of electrons, the electron spin has remained relatively unexploited for digital applications until recently. Although the electron spin is characterized by the two states with distinct projections at a quantization axis and may require a negligible energy for spin reversal, the property attractive for digital electronics is, that the spin interacts effectively with a magnetic, not an electric, field. As the magnetic field is usually generated by a current, this technology turns out to be not suitable for downscaling as reducing the current carrying wire's cross-section increases the current density, which results in reliability issues due to electromigration. It is therefore necessary to proceed to the quantum mechanical level to make the coupling of the electron spin to the electric field efficient.

We briefly review below the current status of spin-based digital switches including the recently demonstrated spin field effect transistor (SpinFET) and the Spin MOSFET, and we outline the exciting challenges still preventing the spin-based switches from entering mass production. Thereafter we document the current status in spin-based purely electrically addressable nonvolatile magnetoresistive memories, which are proven to be competitive with flash memory and possess a considerable potential to enter the dynamic and static RAM markets. We conclude the review with an outlook focusing on nonvolatile logic architectures.

2. Spin-based Switches for Digital Applications

Discovery of the gate-voltage dependent Rashba spin-orbit field [9] acting on the electron spin in the transistor channel opened a possibility for a purely electrical way to manipulate the spin of a propagating electron, which resulted in the proposal of a spin-based transistor, in which the charge functionality was complemented and enhanced by the electron spin – the spin field-effect transistor, or SpinFET [10]. The SpinFET (Fig.1) is a promising future semiconductor device with a performance potentially superior to

that achieved in the present transistor technology [11], [12], [13]. An additional functionality is added by replacing the non-magnetic source and drain electrodes in a FET by ferromagnetic counterparts. The two ferromagnetic contacts (source and drain) are connected by a non-magnetic semiconductor channel region. Metallic ferromagnetic contacts serve not only as an injector/detector of the electron charge current in the channel. Because of their magnetization, the source and drain electrodes inject/detect electron spins [9] ,[10]. The electron current is enhanced in the case of parallel alignment between the source/drain electrodes as electrons injected with spins parallel to the drain magnetization can easily escape from the channel to the drain. Alternatively, the current is suppressed for antiparallel magnetization alignment [9], [10]. The device with the on-current depending on the relative alignment between source and drain is termed spin metal-oxide-semiconductor field-effect transistor (SpinMOSFET). As the magnetization of the source/drain can be manipulated by means of the external magnetic field and/or current (by means of the spin-transfer torque), the two on-current states for parallel/antiparallel magnetization alignment potentially enable the design of reprogrammable logic [10]. Importantly, the relative magnetization orientation between the source and drain is preserved without external power, which makes reprogrammable logic partly nonvolatile.

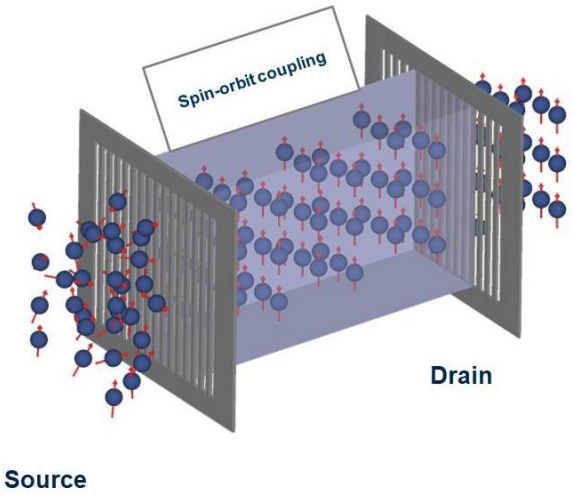


Fig. 1 Illustration of SpinFET functionality [10]. Spin-polarized electrons are injected from a ferromagnetic source and absorbed by a ferromagnetic drain. The electron spins in the channel can be additionally manipulated by means of the gate voltage dependent spin-orbit interaction.

The total current through the device depends on the relative orientation between the magnetization direction of the drain and the electron spin polarization at the end of the semiconductor channel. The electron spin polarization close to the drain interface is determined by the source magnetization and can be additionally modulated by the effective gate voltage dependent spin-orbit interaction in the channel. However, in contrast to the electron charge, the spin injected into the channel is a non-equilibrium quantity and is not conserved. The injected spin relaxes to its equilibrium zero value while propagating through

the channel. Spin relaxation is an important detrimental factor affecting the SpinFET functionality as it reduces the current modulation due to spin functionality.

The spin relaxation is governed by the spin-orbit interaction (SOI) in combination with scattering, so even a spin-independent scattering potential will result in a spin decay. The spin relaxation manifests itself differently in semiconductors of the group IV including silicon and in III-V semiconductors. In crystals obeying the inversion symmetry (silicon, germanium) the spin relaxation is governed by the Elliott-Yafet mechanism [14], [15]. Because the wave function with fixed spin projection is not an eigenstate of the Hamiltonian with the spin-orbit interaction included, the wave function possesses a small but finite contribution with an opposite spin projection. Therefore, the small but finite probability to flip the electron spin appears at every spin-independent scattering event – the Elliott process [14]. This is complemented by the Yafet spin-flip events due to spin-dependent contribution to electron-phonon scattering. In silicon the electron spin relaxation is determined by the inter-valley transitions [14] and can be efficiently controlled by stress [15]. In silicon channels, uniaxial stress generating shear strain is particularly efficient to suppress the spin relaxation [16] as it lifts the degeneracy between the two unprimed subband ladders [17]. In addition, choosing the spin injection direction also boosts the spin lifetime by a factor of two [18]. Recently, the first successful demonstration of a silicon SpinMOSFET at room temperature [19] was presented. A large absolute current modulation in the SpinMOSFET was achieved by altering the relative magnetization between the source and the drain from parallel to antiparallel. However, the relative ratio of the on-currents, a characteristic similar to the tunnel (T) magnetoresistance (MR) ratio, is still several orders of magnitude lower [19] than the TMR in magnetic tunnel junctions. In the SpinMOSFET studied, a MR less than 1% was experimentally observed at room temperature [19]. A possible option to boost the modulation is to employ an electric field at the contact interface between the ferromagnet and the two-dimensional electron gas to increase spin-to-charge conversion [20]. Although a large TMR of 80% was reported on a III-V surface layer at low temperature, at about 1K, which is needed to avoid spin relaxation, the technique of boosting spin-to-charge conversion possesses potential for being employed in silicon at room temperatures.

In III-V materials the crystal lattice does not have any inversion symmetry, and the degeneracy between the up and down spin states with the same electron momentum is lifted. The spin relaxation is governed by the Dyakonov-Perel mechanism [12], [13] and becomes stronger for larger spin-orbit interaction. At the same effective spin-orbit, the design of a SpinFET is facing a tough trade-off. From one side, one needs a stronger spin-orbit interaction for more efficient spin manipulation. From the other side, strong spin-orbit interaction results in a short spin-diffusion length characterizing the distance for which non-equilibrium spins can propagate along the channel before relaxing to the zero equilibrium value. Therefore, the first convincing experimental demonstration of a SpinFET [21] was performed at a very low temperature to effectively suppress spin relaxation.

SpinFETs and SpinMOSFETs can properly function only, if the electron spins are efficiently injected/extracted in/from the channel. To achieve spin injection/detection from a metal ferromagnet in the semiconductor channel and vice versa, a properly engineered tunneling barrier must be placed between the electrodes and the channels [22] to mitigate the spin impedance mismatch. However, the signal attributed to the spin injection [23] appears to be much weaker as compared to the large effect [24] currently attributed to the spin-dependent resonant tunneling [25], [26], [27]. Peculiarities of spin-dependent trap-

assisted tunneling in a multi-terminal configuration may result in switches driven by a single spin on the trap [28] and with characteristics similar to those of a single-electron transistor.

The lack of an efficient way to electrically inject spins from a ferromagnetic metal in a semiconductor was one of the reasons why it took more than 25 years from the vision of a SpinFET in 1990 [10] to the first reliable experimental SpinFET demonstration [21], where a clever idea to employ the voltage-dependent spin-orbit interaction in III-V materials was used for an efficient spin injection from point contacts into the channel. Additional gates were employed to create the point contacts to the two-dimensional electron gas by confining it to a one-dimensional channel. Applying different voltages to these gates produces the spin-orbit Rashba field perpendicular to the point contact. Then all electrons impinging the two-dimensional channel through the one-dimensional point-like contacts are spin-polarized. This way an efficient and purely electrical spin injection is achieved, which allowed the ever first reliable demonstration [21] of a working SpinFET.

New 2D materials (graphene, transition metal dichalcogenides) are attractive for emerging microelectronics applications as they allow developing new concepts, in particular for spin switches [29]. Spin-polarized electrons injected into a graphene sheet propagate to the drain and remain spin-polarized as the spin relaxation in graphene is weak. However, if a MoS_2 single layer is put on top, a parallel path for electrons through the material with strong spin relaxation is open, and the current reaching the drain is not spin-polarized. As the chemical potential of the MoS_2 layer can be tuned from the conduction band to the gap, this opens the opportunity to have a switch between spin-polarized/spin-unpolarized drain currents depending on the gate voltage, which operates at 200K.

Although many fundamental challenges have been resolved and a SpinFET and a SpinMOSFET have been successfully demonstrated, both devices still rely on the charge current to transfer the spin, which may set some limitations for the applicability of such devices in main-stream microelectronics. In addition, the absence of an efficient and purely electrical spin injection scheme results in a low MR inferior to that in magnetic tunnel junctions. Nonvolatile devices based on magnetic tunnel junctions possess a TMR suitable for practical applications, in particular in memory devices discussed below.

3. NONVOLATILE MAGNETORESISTIVE MEMORIES

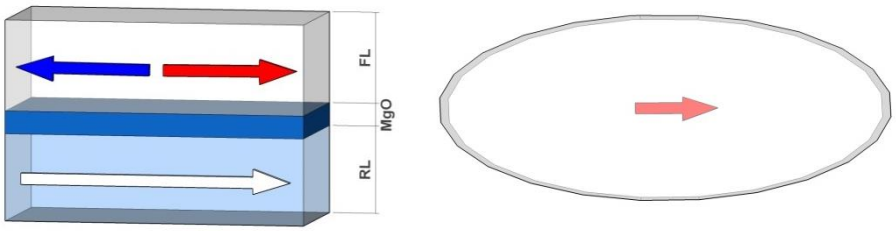
An efficient coupling between the electrical and the magnetic degree of freedom at the quantum mechanical level, called the giant magneto-resistance effect, was discovered in 1986. The discovery offered a purely electrical way of reading the stored magnetization information, which revolutionized hard drive storage devices and was honored with the Nobel Prize in 2007 [30].

It then was discovered that the tunneling current through a magnetic tunnel junction (MTJ) consisting of two ferromagnets separated by a thin tunnel barrier structure strongly depends on the relative polarization of the ferromagnetic contacts. The difference in the MTJ resistivity between the parallel and the antiparallel configuration reaches several hundred percent at room temperature [31], which represents an efficient way of converting the spin (magnetization) degree of freedom into a charge (current) employed by CMOS devices. Thanks to this technology a new generation of hard drives with even higher storage densities has been developed.

However, in order to introduce competitive nonvolatile memory based on MTJs, an efficient way of converting charge information into magnetic moment (spin) orientation by purely electrical means is required. The spin-transfer torque effect (STT) [32], [33] has been proven to be perfectly suited for purely electrical data writing by passing a current through the MTJ (Fig.2a). When electrons pass through a fixed ferromagnetic layer, their spins become aligned with the magnetization. When these spin-polarized electrons enter the free magnetic layer, they become aligned with the magnetization of the free layer within a transition layer of a few angstroms. Due to the conservation of the total angular momentum the change of the electron spin is compensated by the modification of the free layer magnetization. Therefore, the spin-polarized current exerts a torque on the magnetization of the free layer. If the current is sufficiently strong to overcome the damping, this torque causes magnetization switching. If the current tends to switch the magnetization from the parallel to the antiparallel configuration, altering the current direction will result in the magnetization switched from the antiparallel to the parallel state.

3.1. Spin-transfer torque MRAM

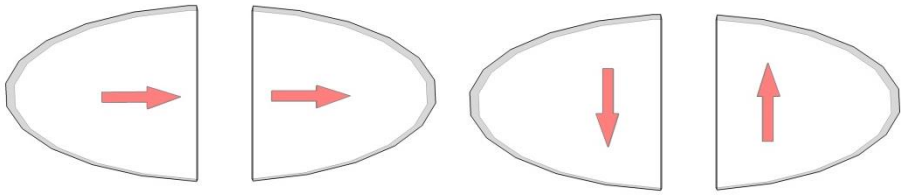
The exciting journey of bringing STT-MRAM to the market was ignited by the observation of spin torque induced switching in MgO-based [34] STT-MRAM cells. Depending on the orientation of the layer magnetizations the magnetic pillars can be divided into in-plane with the magnetization lying in the plane of the magnetic layer (Fig.2) and out-of-plane with the magnetization direction to be discussed later.



(a) (b)

Fig. 2 (a) Magnetic tunnel junction with in-plane magnetization orientation. The magnetization of the reference layer (RL) is fixed, while the magnetization of the free layer (FL) can be flipped between the two preferred magnetization orientations by means of the spin transfer torque generated by the current passing through the structure. The two ferromagnetic layers are separated by a thin MgO tunnel barrier. (b) The preferred magnetization direction in in-plane magnetized free layers is defined by their shape. For elliptic structures these directions are along the long ellipse axes.

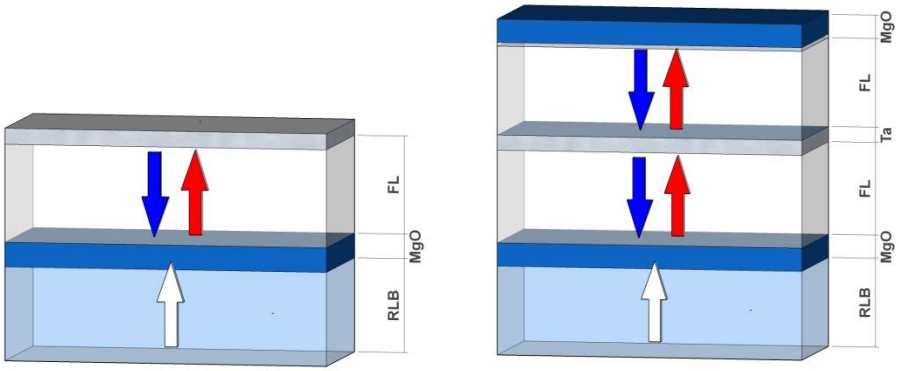
For in-plane MTJs, faster switching is achieved, when the free layer is made of two half-ellipses separated by a narrow gap [35], [36] schematically shown in Fig.3. The switching of the half-elliptic parts appears in-plane in opposite senses (Fig.3b). This way a large demagnetization penalty of the magnetization getting out of plane at switching of a monolithic structure (Fig.2b) is avoided, and the switching barrier becomes equal to the thermal barrier. Because the thermal barrier depends on the free layer volume, the required large thermal stability factors of ~80kT are easily achieved in this structure.



(a) (b)

Fig. 3 (a) Equilibrium magnetization in an in-plane composite layer made of two half-elliptic parts separated by a narrow gap.
(b) At spin transfer switching, the magnetization of either half-elliptic part remains mainly in-plane. The magnetizations move in opposite senses and pass through the configuration defining the thermal barrier between the two equilibrium states [35].

In perpendicular MTJs (p-MTJs) shown in Fig.4a the thermal barrier separating the two states is equal to the switching barrier, which reduces the switching current. In addition, p-MTJs are better suited for high-density integration [37].



(a) (b)

Fig. 4 (a) Illustration of a perpendicularly magnetized MTJ. The perpendicular uniaxial anisotropy is interface-induced [38]. (b) The thermal stability is enhanced by adding the second CoFeB/MgO interface with the interface induced anisotropy [42]. The Gilbert damping is also reduced for the composite free layer made of two thin ferromagnetic CoFeB layers separated by a Ta metallic spacer [42].

However, it is difficult to find a material with so strong uniaxial anisotropy that it can overcome the demagnetization field of a layered structure bringing the magnetization in-plane. A critical technological step allowing to solve this problem was the discovery of an interface-induced perpendicular anisotropy at the CoFeB/MgO interface [38], which makes the very thin CoFeB layer perpendicularly magnetized. To scale the diameter of the MTJ beyond 10nm, the use of shape anisotropy was suggested [39]. It has been

shown that the thermal stability can be boosted for small diameters without sacrificing on TMR and without any need of new materials, as FeB for the ferromagnetic free layer and MgO for the tunnel barrier were used.

Any nonvolatile memory including MRAM must be characterized by the ability to write the data with low energy without damaging the device, long data retention, and the ability to read the data without destroying it. Improving one or two aspects of its functionality usually leads to a degradation of the remaining functionality [40]. Therefore, a careful parameter optimization specific to a particular technology must be properly addressed. An innovative design yielded already a successful implementation of 8Mb 1T-1MTJ STT-MRAM embedded in a 28nm CMOS logic platform [41].

Another issue with STT-MRAM is the relatively high current required for fast STT-induced writing. This fact has several implications. Firstly, due to the relatively high energy required for writing, STT-MRAM cannot be used in high-level processor caches due to the high activity factor. The necessity to switch memory frequently negates the benefits of nonvolatility provided by MRAM. Secondly, large switching currents are supplied via an access transistor. Finally, a large switching current density can result in serious reliability issues like MTJ's resistance drift and eventually its dielectric breakdown. The critical current density depends on the switching pulse duration, with a substantial current increase for sub 10ns switching. A plausible way to reduce the switching current density is to work with p-MTJs, however, even in this case the switching current competes with the Gilbert damping and must be sufficiently strong to overcome the potential barrier separating the two states, the thermal stability barrier.

The height of the thermal stability barrier determines the data retention. For 10 year data retention the thermal stability barrier must be at least 80kT for gigabit MRAM arrays. As the barrier cannot be decreased without violating the retention, in order to reduce the switching current density and preserve the large thermal barrier at the same time, one has to reduce the Gilbert damping and increase the spin current polarization. A solution which helps boosting the thermal stability barrier is to employ a free layer with two CoFeB/MgO interfaces [42] with the interface induced perpendicular anisotropy shown in Fig.4b. It turns out that the use of the p-MTJ structure with two CoFeB/MgO interfaces and a composite free layer CoFeB/Ta/CoFeB [42] also reduces the Gilbert damping by half, thus allowing to simultaneously boost the thermal barriers and to reduce the switching current.

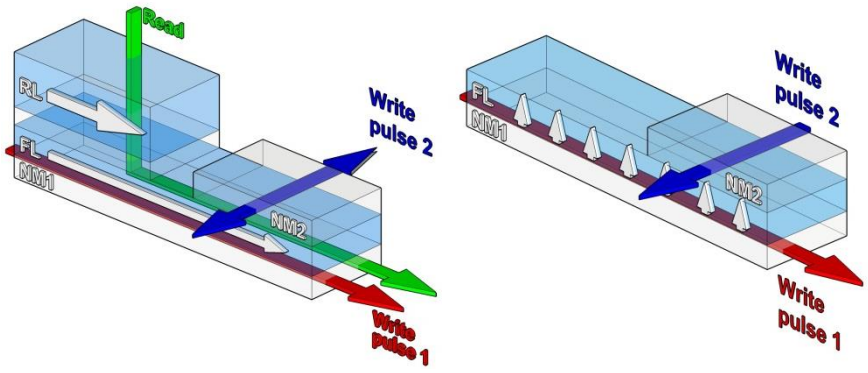
In order to integrate STT-MRAM with the CMOS fabrication process, MTJs must sustain at least 400C temperature typical for the back-end-of-line process. Recently, IMEC reported a process allowing to preserve the high TMR and thermal stability of MTJs [43]. The idea is to invert the free and the fixed layer by putting the fixed layer on top of the MTJ. An additional synthetic ferromagnet instead of an antiferromagnet is employed to pin the magnetization of the fixed layer. The design requires a compensating magnet to be in addition integrated in the structure. Optimization of this magnet can be used to achieve a symmetric switching between the parallel and the antiparallel configuration and back.

Advanced STT-MRAM is characterized by a high-speed access time of 10ns. It is thus suitable for last level caches. 4Gbit STT-MRAM arrays with p-MTJs and compact memory cells were recently reported [37]. Currently, 256Mb STT-MRAM from Everspin Technologies is already available [44]. All major foundries including Samsung [45] and Globalfoundries [46] announced the beginning production of embedded STT-MRAM based on the 28nm [41]/22nm [46] fully-depleted silicon-on-insulator technology. We are therefore witnessing the beginning of nonvolatile STT-MRAM entering the embedded

memory market and competing with DRAM and potentially SRAM, traditionally dominated by CMOS-based volatile devices. If successful, this will result in an exponential growth of the STT-MRAM market with a momentous impact on information storage and processing in the near future.

3.2. Spin-orbit torque MRAM

Spin-transfer torque magnetic RAM (STT-MRAM) is fast (10ns), possesses high endurance (10^{12}), and has a simple structure. It is compatible with CMOS and can be straightforwardly embedded in circuits. It is particularly promising to employ nonvolatility in internet of things (IoT) and automotive applications, as well as a replacement of conventional volatile CMOS-based DRAM and nonvolatile flash memory. Although the use of STT-MRAM in last-level caches is conceivable [47], the switching current for operating faster than at 10ns is quite high. The need of even higher switching currents for faster operation in higher-level caches potentially prevents STT-MRAM from entering in L2 and L1 caches currently mastered by static RAM (SRAM). In addition, rapidly increasing critical currents required for operating STT-MRAM at 5ns result in large current densities running through magnetic tunnel junctions. This leads to oxide reliability issues, which in turn reduces the MRAM endurance to that of the flash memory, thus negating one of the important MRAM advantages over flash.



(a) (b)

Fig. 5 (a) Spin-orbit torque memory cell with an in-plane magnetized free layer (FL) switched by current write pulses (red and blue) applied through heavy metallic wires NM1 and NM2 with a high spin Hall angle. FL is grown on NM1. Read current (green) is applied through an MTJ. (b) The switching scheme [36] based on two short consecutive orthogonal current pulses provides fast, deterministic, and magnetic field free magnetization reversal of a perpendicularly magnetized FL [68].

The engineering of an electrically addressable nonvolatile memory combining high speed (sub-ns operation) and high endurance suitable for replacing SRAM in higher-level caches of hierarchical multi-level processor memory structures cannot be based on STT, and the use of new physical principles is required. Among the newly discovered physical phenomena suitable for next-generation MRAM is the spin-orbit torque (SOT) assisted

switching at room temperature in heavy metal/ferromagnetic [48], [49], [50], [51], [52], [53], [54], [55] or topological insulator/ferromagnetic [56], [57], [58], [59] bilayers (Fig.5). In this memory cell, the magnetic tunnel junction's free layer is grown on a material (NM1 in Fig.5) with a large spin Hall angle. The SOT acting on the adjacent magnetic layer is generated by passing the current through this material, schematically shown by the red arrow. The large switching current is injected in-plane along the heavy metal/ferromagnetic bilayer and does not flow through the MTJ, the state of which is read by passing a small current through the MTJ shown by the green arrow. This results in a three-terminal configuration where the read and write current paths are decoupled. Since the large write current does not flow through the oxide in the MTJ, this prevents the tunnel barrier from damage. Therefore, three-terminal MRAM cells are promising candidates for future generations of nonvolatile memory for fast sub-ns switching [54]. SOT-MRAM is an electrically addressable nonvolatile memory combining high speed and high endurance and is thus suitable for applications in caches [54]. Although the high switching current is not flowing through a magnetic tunnel junction but rather through a heavy metal wire under it, the current is still high, and its reduction is the pressing issue in the field of SOT-MRAM development.

Topological insulators (TIs) are promising materials for reducing the switching current as they are characterized by a high spin Hall angle and efficiency of charge to spin conversion due to peculiar perpendicular spin-momentum locking in the interface states. In addition, the strong spin-orbit interfacial Rashba field helps generating spin density in TIs boosting the charge to spin conversion efficiency above 100%.

However, although high charge to spin conversion efficiency in TIs has been reported, the electrical conductivity of TIs required to build a high-density, ultra-low power, and ultra-fast nonvolatile memory was not sufficiently high because of their insulating bulk. Recent developments introduce BiSe [57] and BiSb [58] based TIs as suitable candidates for emerging SOT-MRAM as they possess a charge to spin conversion efficiency of 18.8 and 52 times, respectively. This allows reducing the switching current by two orders of magnitude as compared to tungsten-based SOT-MRAM. In addition, BiSb samples [58] exhibit very high electrical conductivity making thin BiSb films leading candidates for emerging fast and low-power SOT-MRAM, and the process integration of BiSb into a realistic MTJ stack is currently under scrutiny.

Despite an undisputable progress in developing SOT-MRAM, one important shortcoming has not been convincingly resolved so far. Namely, a static magnetic field is still required to guarantee deterministic switching [60] or a perpendicularly magnetized free layer. Several paths to achieve deterministic switching without magnetic fields were suggested. They require unusual solutions to break the mirror symmetry either by means of the shape of the dielectric [61] or the free layer [62], or by controlling the crystal symmetry of the metal line at the microscopic layer [53]. Biasing the free layer by employing an exchange coupling to an antiferromagnet [63], [64], [65], [66] as well as the use of a peculiar sample shape, which controls the switching [67], were recently reported. However, even if in most of these studies a field-free switching was reported, these methods either require a local intrusion into the fabrication process, or are based on solutions whose scalability is questionable (antiferromagnets, shapes), which makes further large scale integration of the fabricated memory cells problematic

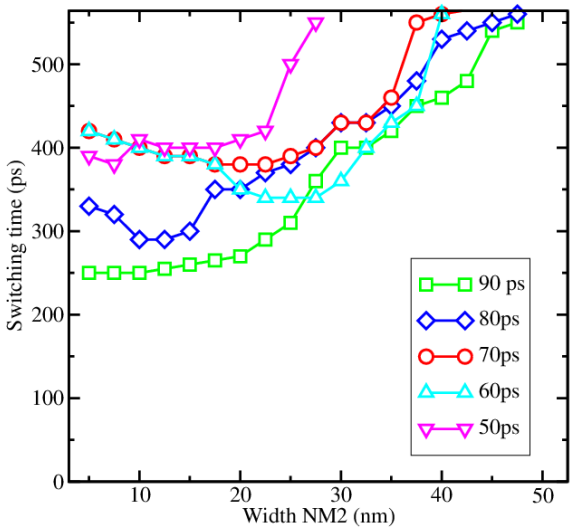


Fig. 6 Switching time of a perpendicular FL as a function of the width of the heavy metal line NM2, for several durations of the second write current pulse in the two-pulse switching scheme [36]. A NM2 width of 12.5nm is optimal as it guarantees fast, robust, and deterministic switching which is insensitive to small variations of the pulse duration or the NM2 width. The applied write currents are equal to 100μA. The first write current pulse of 100ps is applied after initial thermalization at 300K. The saturation magnetization is M_S=4×10^{5}A/m, the Gilbert damping is α=0.05, and the FL dimensions are 52.5nm × 12.5nm × 2nm.

The SOT switching scheme based on the use of two consecutive orthogonal sub-nanosecond current pulses shown in Fig.5 can switch in-plane structures efficiently [37], [68]. The implementation is suitable for integration in a cross-bar architecture [37]. The two-pulse switching scheme is applicable for switching perpendicularly magnetized free magnetic layers of rectangular shape shown in Fig.5b [69]. The second consecutive pulse is applied through the wire NM2 with a large Hall angle. Sub-300ps, 100% reliable, and magnetic field-free switching is achieved at around 30% overlap of the second pulse wire NM2 with the free layer as shown in Fig.6. In addition, at these overlaps the switching is not sensitive to small variations of the NM2 width and the second pulse duration.

A proper integration of SOT-MRAM represents a significant challenge as the memory cells must withhold at least the back-end-of-line thermal budget. As IMEC presented recently a technology to integrate a perpendicular beta-phase W/CoFeB/MgO/CoFeB/synthetic antiferromagnetic stack based SOT-MRAM on a 300mm CMOS wafer with fully CMOS compatible processes [70], there is a cautious confidence that fast low-power nonvolatile magnetoresistive memory suitable for processor caches will be developed soon.

4. NONVOLATILE COMPUTING

MRAM is CMOS compatible and is embedded directly on top of a CMOS logic chip. This layout is practically relevant as it facilitates 3D integration of circuits in which high-performance CMOS layers are separated by low energy consuming nonvolatile MRAM containing spacers. Fast nonvolatile memory combined with nonvolatile processing elements is a fertile ground for realizing microprocessors with reduced power consumption working on an entirely new principle. In addition, placing MRAM arrays directly on top of CMOS circuits allows reducing the length of interconnects and the corresponding delay time. The computer architecture, where nonvolatile elements are located on a chip with CMOS devices, is traditionally called logic-in-memory, although as of yet no information is processed in nonvolatile elements. Power-efficient MRAM-based logic-in-memory concepts have already been demonstrated [71]. They include field-programmable gate arrays and ternary content addressable memory, as well as other variants. These CMOS/spintronic hybrid solutions are already competitive in comparison to the conventional CMOS technology with respect to power consumption and speed. The introduction of nonvolatility in circuits helps cutting the power consumption by 50%, with outstanding 90% reduction in specific circuits [71].

Placing the actual computation into the magnetic domain reduces the need of converting magnetically stored information into currents and voltages for processing and helps to simplify the circuit layout and to increases the integration density. The idea is to use MTJs as elementary blocks for non-conventional in-memory computing architectures. For example, any two of the 1T-1MTJ cells in an MRAM array can not only serve as nonvolatile memory units, but can also be employed for implementing a conditional switching of a target MTJ depending on the state of the source MTJ [72]. This results in a logical operation known as the material implication operation (IMP), which in combination with the FALSE operation can cover the whole space of all Boolean operations. A compact implication-based single-bit full adder realization involving only six 1T-1MTJ cells and 27 subsequent FALSE and IMP operations can be realized [73]. Recently, a massively parallel NOT operation based on IMP implementation by using the voltage asymmetry of the voltage controlled magnetic anisotropy effect and the precessional dynamics of the switching process was proposed [74].

The logic architecture based on the devices acting simultaneously as a memory element and compute unit is termed stateful. An alternative option is to follow a conventional path with memory and computing units separated, in which, like in an all-spin logic concept [75], both elements are nonvolatile and implemented in a magnetic domain. Placing the actual computation into the magnetic domain eliminates the need of converting magnetically stored information into the currents and voltages for processing. The idea of combining MTJs with a common free layer enables the realization of a nonvolatile magnetic flip-flop [76]. The processing unit consists of an STT based nonvolatile majority gate and nonvolatile magnetic flip-flops used as memory registers in a nonvolatile processing environment [77].

The availability of high-capacity nonvolatile memory enables new logic-in-memory and computing-in-memory architectures for future artificial intelligence and cognitive computing [78]. Nonvolatile MTJs are suitable for neural network realizations as they can be considered as a current-driven programmable resistor, a memristor [79]. MTJ based neural networks featuring nonvolatile synapses [80] allow for high-speed pattern

recognition with about a 70% reduction in gate count and a 99% improvement in speed as compared to their CMOS counterparts. Neuromorphic computing is becoming a reality, with the first self-learning chips already revealed [81].

5. CONCLUSIONS

Although spin switches based on spin-enhanced transistors have been successfully demonstrated, the increase of the on-current ratio between the parallel and antiparallel source/drain magnetization configuration at room temperature and the efficient gate voltage induced spin control remain the main challenges preventing these devices from entering the market so far. In addition, as all proposed up-to-date spin switches require the charge current to transfer the spin, it sets limitations for the applicability of such devices in main-stream microelectronics which is already suffering from high power demand, and new ideas to realize spin-based switches for digital applications are urgently needed.

Nonvolatile memories based on magnetic tunnel junctions are about to hit the market as all leading manufacturers announced embedded STT-MRAM production in 2018. STT-MRAM is positioned as a successor not only for flash, but also for CMOS-based main computer memory. However, rapidly growing switching currents and power consumption might prevent STT-MRAM from entering cache memory currently mastered by SRAM. Because of the large switching currents and insufficient speed, STT-MRAM is unlikely to replace SRAM in high-level core caches. Spin-orbit torque innovative nonvolatile devices with improved switching characteristics and enhanced charge to spin conversion efficiency demonstrate a potential for processor-embedded memories.

The successful adoption of nonvolatility in microelectronic systems by developing various logic-in-memory architectures and in-memory processing will inevitably result in increasing dissemination of this technology for other applications such as ultralow-power electronics, high-performance computing, Big Data analysis, automotive electronics, and the Internet of Things.

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