

IGBTS WORKING IN THE NDR REGION OF THEIR I-V CHARACTERISTICS

Riteshkumar Bhojani¹, Thomas Basler¹, Josef Lutz¹, Roland Jakob²

¹Department of Power Electronics and Electromagnetic Compatibility, Technische Universität Chemnitz, Germany

²GE Energy Power Conversion Berlin, Germany

Abstract. *This paper demonstrates the detailed work on high voltage IGBTs using simulations and experiments. The current-voltage characteristics were measured up to the break through point in forward bias operating region at two different temperatures for a 50 A/4.5 kV rated IGBT chip. The experimentally measured data were in good agreement with the simulation results. It was also shown that the IGBTs are able to clamp high collector-emitter voltages although a low gate turn-off resistor in combination with a high parasitic inductance was applied. Uniform 4-cell and 8-cell IGBT models were created into the TCAD device simulator to conduct an investigation. An engendered filamentation behaviour during short-circuit turn-off was briefly reviewed using isothermal as well as thermal simulations and semiconductor approaches for development of filaments. The current filament inside the active cells of the IGBT is considered as one of the possible destruction mechanism for the device failure.*

Key words: *IGBT, I-V characteristic, voltage clamping, short-circuit, filamentation*

1. INTRODUCTION

IGBTs are one of the most important power semiconductor devices in low, medium and high power applications ranging from few hundred volts to several thousand volts. This device offers excellent switching behaviour, easy gate drivability, wide safe operating area, snubber-less operation and robust turn-off capability. In addition, the capability to limit the short-circuit current is one of the superior properties of IGBTs [3, 4]. The basic physics of the IGBTs is explained well in given literatures [1-4].

In the present work, the investigated IGBT chips are taken from a high voltage IGBT press-pack device which consists of 42 single IGBT chips. Each chip is rated at 50 A for 50 Hz half-sine waveform at 75 °C and has a blocking capability of 4.5 kV. The purpose of this paper is to give a comprehensible explanation of the device behaviour from static up to dynamic characteristics. Simulations are performed here to investigate internal

Received October 15, 2014

Corresponding author: Riteshkumar Bhojani

Department of Power Electronics and Electromagnetic Compatibility, Technische Universität Chemnitz
Reichenhainer Str. 70, Room H109, D-09126 Chemnitz, Germany

(e-mail: riteshkumar.bhojani@etit.tu-chemnitz.de)

effects of the IGBTs. The IGBTs presented here have a planer cell structure and a field-stop layer at the collector side.

2. IGBT COMPLETE I-V CHARACTERISTICS UP TO BREAKDOWN POINT

To understand the device behaviour, the static characteristics of the IGBT at different gate voltages has to be well understood. The technique to measure IGBT static characteristics non-destructively was explained in [5]. Complete static characteristics were measured using two different measurement setups. The first setup uses the “Tektronix 371B curve tracer” up to the maximum power of 3 kW. The measurement points in desaturation and breakthrough area at the breakthrough branch were taken using a single pulse short-circuit (SC) type 1 measurement setup given in Fig. 1(a) [5].

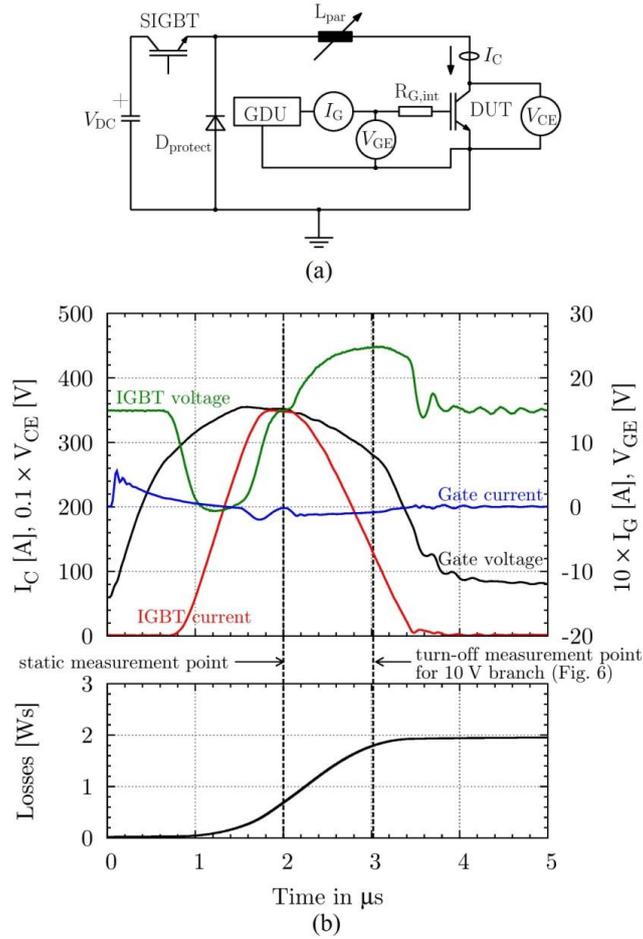


Fig. 1 (a) SC 1 test circuit (b) SC example pulse for static characteristic measurement
 $V_{GE} = 15$ V, $V_{DC} = 3.5$ kV, $L_{par} = 3.9$ μ H, $R_{G,on} = 44$ Ω , $R_{G,off} = 220$ Ω , $T = 400$ K

A protection IGBT (SIGBT) was used to turn-off the short-circuit in a case of DUT (device under test) failure. Several measurement points of the desaturation area have been taken during the static short-circuit phase. High parasitic inductances (L_{par}) up to 14 μH in combination with low $R_{\text{G,off}}$ have been used to produce high overvoltages during SC turn-off. Thereby, the breakdown point of the output characteristic can be attained for a short time interval. The course of V_{CE} , I_{C} , V_{GE} and I_{G} moments read-out times of the different measurement points and energy loss during the short-circuit measurement pulse are displayed in Fig. 1(b). The applied collector-emitter voltage during this measurement was 3.5 kV at a temperature of 400 K. The gate to emitter voltage (V_{GE}) and collector-emitter voltage (V_{CE}) were measured very close to the chip to avoid parasitic influences. Charging process of the IGBT capacitances and self heating during the short-circuit pulse has to be considered to get exact points of the I-V characteristics. Since the width of the short-circuit pulse is reduced to small values, the losses generated up to the measurement point are low. A very small increment in the chip temperature can be calculated due to the large base width of the high voltage IGBT. Temperature change ΔT_{SC} during the short-circuit turn-off was calculated using Equation (1) by assuming a homogeneous temperature distribution throughout the chip [5].

$$\Delta T_{\text{SC}} = \frac{W_{\text{SC}}}{C_{\text{th}}} = \frac{W_{\text{SC}}}{c_{\text{th,Si}} \cdot \rho \cdot d \cdot A} \quad (1)$$

$$\Delta T_{\text{SC}} = \frac{0.7 \text{ J}}{788 \text{ J kg}^{-1} \text{ K}^{-1} \cdot 0.00234 \text{ kg cm}^{-3} \cdot 0.128 \text{ cm}^3} \approx 3 \text{ K}$$

In Equation (1), W_{SC} is the energy loss during single pulse short-circuit, C_{th} is the thermal capacitance, $c_{\text{th,Si}}$ is the lattice heat capacity of Silicon, ρ is the density of Silicon, d is the IGBT thickness and A is the IGBT area. The calculated temperature rise for SC was added to the measurement temperature of static curve tracer measurements [5].

The measured and simulated I-V characteristics of the IGBTs are shown in Fig. 2(a) and Fig. 2(b) at two different temperatures 300 K and 400 K respectively. The graphs exhibit good agreement between measured and simulated results. At higher currents, the bipolar current gain increases due to increase in injection efficiency and base transport factor. This is the reason for an increment in IGBT saturation current at higher collector-emitter voltages. The current equation of the IGBT and its relation to bipolar current gain are mentioned below [1-4].

$$I_{\text{C,sat}} = \frac{1}{(1 - \alpha_{\text{pnp}})} \cdot \frac{k}{2} \cdot (V_{\text{GE}} - V_{\text{TH}})^2 \quad (2)$$

$$k = \frac{W \cdot \mu_{\text{n}} \cdot C_{\text{ox}}}{L} \quad (3)$$

$$\alpha_{\text{pnp}} = \gamma_{\text{E}} \cdot \alpha_{\text{T}} \quad (4)$$

$$\gamma_E = \frac{j_p}{j_p + j_n} \quad (5)$$

$$\alpha_T = \frac{1}{\cosh\left(\frac{W_{\text{eff}}}{L_{p,\text{NB}}}\right)} \quad (6)$$

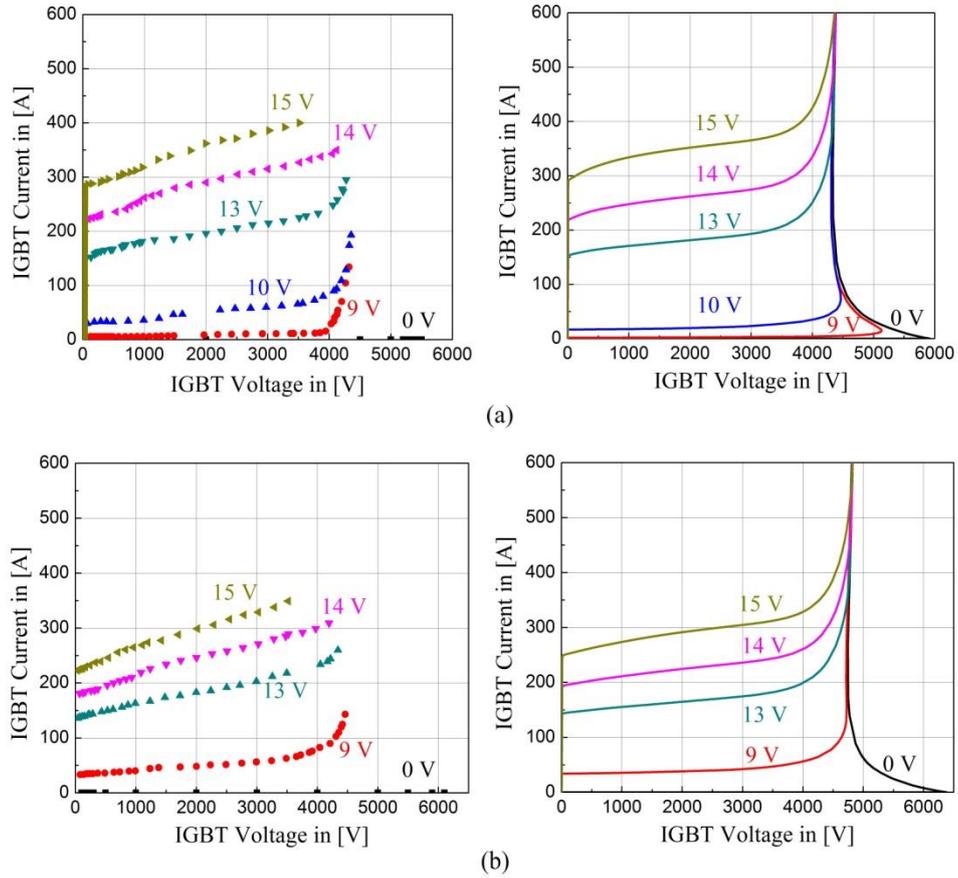


Fig. 2 Measured (left-side) and simulated (right-side) IGBT static characteristics
(a) $T = 300$ K (b) $T = 400$ K

In above Equation (2), k is the channel conductivity and α_{pnp} is the bipolar current gain given by Equations (3) and (4). V_{GE} is the gate emitter voltage, V_{TH} is the threshold voltage, μ_n is the electron mobility, C_{ox} is the oxide capacitance, γ_E is the injection efficiency, α_T is the base transport factor, j_p is the hole current density, j_n is the electron

current density, W_{eff} is the non-depleted width of the n^- base and $L_{p,\text{NB}}$ is the diffusion length for holes in collector side buffer region.

The higher the applied battery voltage the more holes are injected from the collector side. If V_{CE} increases, the space charge region expands. Consequently the effective base width will be reduced. The effective base width is the non-depleted width of the base region under applied collector-emitter voltage. Therefore, the injection efficiency and the base transport factor increases with higher V_{CE} which results in increased bipolar current gain. Hence, the IGBT collector current grows with the increment in applied collector-emitter voltage. Moreover, the reduced collector current at higher temperatures for gate voltages, significantly higher than threshold voltage, were resulted from the strong mobility dependency on temperature. For gate voltages slightly higher than the threshold voltage, the saturation current can also increase with temperature due to the strong reduction of the V_{TH} . These operation points are below the so called ‘‘Temperature Compensation Point’’ (TCP) [18].

When gate voltage is lower than the threshold voltage of the IGBT, the MOS channel cannot supply electrons to conduct current. As the gate voltage comes close to the threshold voltage, a very small amount of current flows due to the starting of accumulation of electrons below the gate oxide. The saturation current strongly depends on the thickness of the gate oxide layer below the gate contact. A small reduction in gate oxide thickness influences the channel conductivity k which is given by Equation (3). Thus, the gate oxide considered as one of the crucial parameter for designing IGBT simulation model.

On the breakdown characteristic, the measurement results describe that for $V_{\text{GE}} > V_{\text{TH}}$, the IGBT is able to block about 4.2 kV at 300 K. This breakdown voltage is significantly lower than the breakdown voltage at $V_{\text{GE}} = 0$ which is 5.5 kV shown in Fig. 2(a). At 400 K, the measured breakdown voltage is slightly lower than the simulated breakdown voltage. In practice, during the short-circuit turn-off event it is more practical that the operating point comes on the NDR (negative differential resistance) branch of the IGBT static characteristics for low $R_{\text{G,off}}$. This could lead the IGBT to destructive mechanisms. One of the possible destruction mechanisms was filamentation due to the rapid turn-off of the IGBTs during short-circuit type 1. Later on, the filamentation phenomenon is explained using simulation results.

3. SELF-CLAMPING AT SHORT-CIRCUIT TURN-OFF OF HIGH VOLTAGE IGBTs

IGBTs have the potential to block high overvoltages during fast switching or short-circuit. In this part of work, investigations were done on the single IGBT. The measured IGBTs were able to clamp the overvoltages induced during short-circuit turn-off event. The high V_{CE} can occur during fast short-circuit turn-off and self turn-off [7] and this can be clamped by IGBTs itself. A similar clamping mechanism has already been described for the IGBT overcurrent turn-off in [9] and switching self clamping mode (SSCM) [7-9]. However, for low gate turn-off resistor, the IGBT turn-off may become critical and unstable which leads to the device destruction. Here, the gate turn-off resistor ($R_{\text{G,off}}$) controls the speed and the overvoltage during turn-off process.

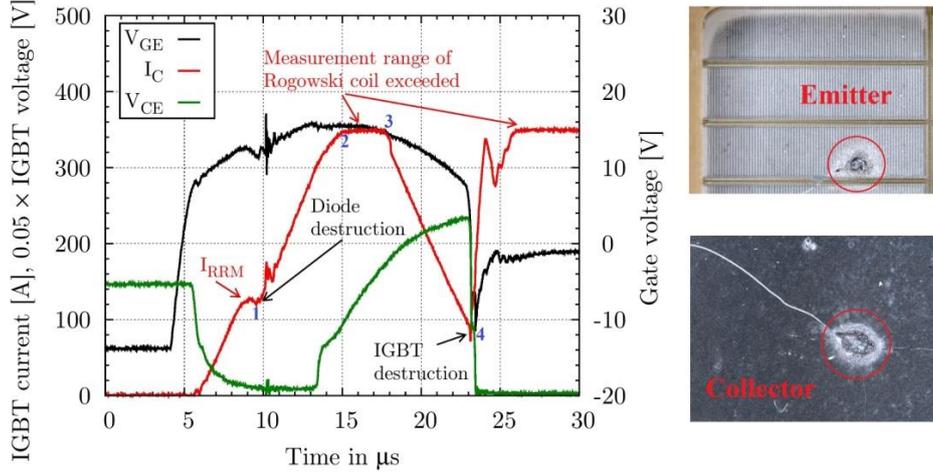


Fig. 3 IGBT destruction during short-circuit turn-off (initial failure: freewheeling diode failed during double pulse test with high turn-on inductance, SC type 2 for IGBT) $V_{DC} = 3$ kV, $L_{par} = 7.75$ μ H, $R_{G,off} = 300$ Ω , $T = 400$ K

Fig. 3 demonstrate waveforms of the short-circuit type 2 turn-off, where at point 1 the freewheeling diode fails first during its reverse recovery and the IGBT runs under short-circuit. In the measurement, the IGBT current exceeds the measurement range of the used rogowski coil. At point 3, the IGBT is automatically turned-off by the gate drive unit. Therefore, a large overvoltage is induced which comes on the post avalanche branch of the static characteristic and the IGBT was destroyed, see point 4. The values used for the parasitic inductance, gate turn-off resistor and temperature are displayed in Fig. 3. The destruction point on the chip is clearly visible from the emitter and from collector side as well [14]. A crack engendered during the destruction which propagates towards the junction termination. The detailed explanation about different short-circuit types are given in [10-12].

Fig. 4 (a) and (b) shows the measured and simulated clamping mechanisms by IGBTs during single pulse short-circuit turn-off. To compare measurement with simulation, different values for the gate turn-off resistor were taken. High overvoltage induced due to the high parasitic inductance during the falling di_C/dt . For small $R_{G,off}$, di_C/dt is limited by avalanche generation to

$$\frac{di_C}{dt} = \frac{V_{Clamp} - V_{DC}}{L_{par}} \quad (7)$$

which is defined for SSCM mode and holds for measurements as well as simulations [9]. In difference to overcurrent turn-off, the density of the charge carrier is quite low for the short-circuit case due to high applied electric field.

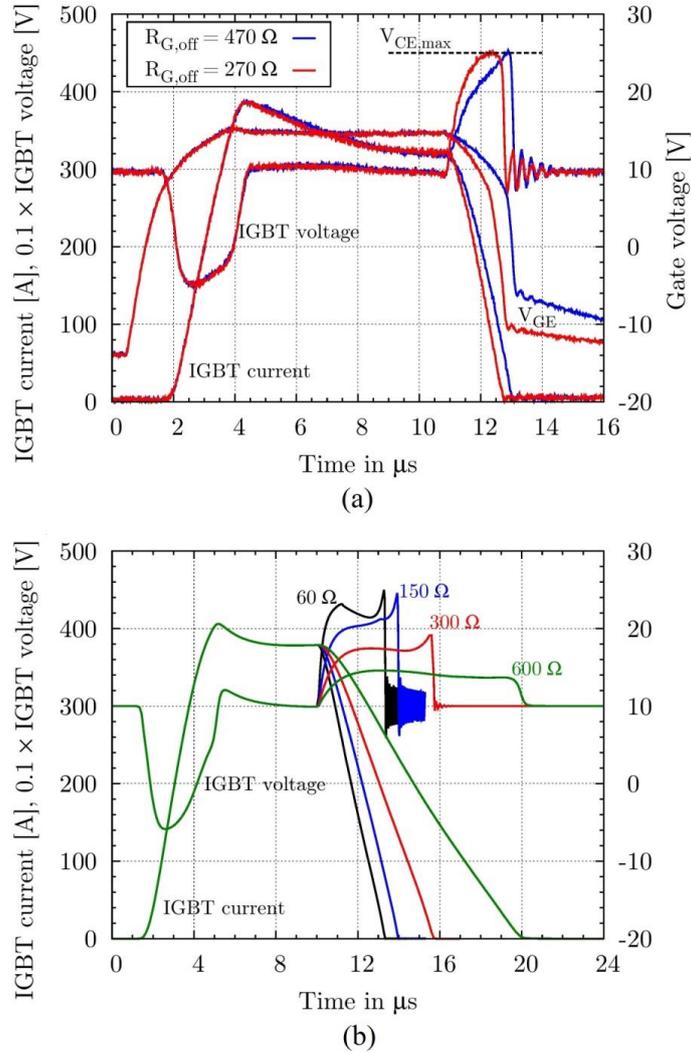


Fig. 4 (a) Measured SC 1 behaviour $V_{DC} = 3 \text{ kV}$, $L_{par} = 7.3 \mu\text{H}$, $T = 300 \text{ K}$
 (b) Simulated SC 1 behaviour $V_{DC} = 3 \text{ kV}$, $L_{par} = 10 \mu\text{H}$, $T = 300 \text{ K}$

Measurements and simulations were done using different gate turn-off resistors. The clamping mechanism is shown with the help of simulations using a half-cell IGBT model in Fig. 4(b). Half-cell, 4-cell and 8-cell IGBT models are proposed in this work to inspect the physical behaviour. They were fitted to match the behaviour of the real IGBT. The measurements clearly show a course through the NDR region of the static curve for the phase of rapidly increasing V_{CE} during fast turn-off. At this point, the IGBT turn-off behaviour completely relies on the course of the applied gate voltage which will be explained in the next section.

The NDR branch of the IGBTs is related to the bipolar current gain explained in previous section. It has a vast influence on the I-V characteristics. By increasing the buffer deepness of the IGBT, it is possible to adjust the bipolar current gain and emitter efficiency that will result in high blocking capability. That means the NDR branch shifts towards higher voltages for e.g. deeper field-stop regions. There are other possible ways to adjust bipolar current gain. More detailed explanation has been given in the following literature [13, 14]. From this clamping behaviour, it is difficult to conclude the physical reasons behind the destruction of the IGBTs. Therefore, investigations were completed using 4-cell and 8-cell IGBT isothermal and thermal simulations to investigate the cause for the IGBT destruction.

4. FILAMENTATION IN IGBTs DURING SHORT-CIRCUIT TURN-OFF

Simulation allows complex analysis of the internal behaviour and gives several physical parameters like electric field expansion, electron and hole density, temperature distribution, current density and much more. Precise knowledge of those various physical quantities can explain the possible reasons for device destruction. In this section, an isothermal simulation of the 4-cell and 8-cell IGBT model shall be demonstrated. Furthermore, it is not possible to ascertain filamentation behaviour using half-cell IGBT model. Therefore, the IGBT model should have more than one full cell structure to realize current filaments. The simulation time has to be considered as well for simulation of structures with large number of IGBT cells. Filaments were found before in IGBTs under various conditions and at different places inside the IGBTs in given published works [15-17].

The single pulse short-circuit type 1 turn-off was used with adjusted pulse length of 20 μ s. At 20 μ s, the IGBT was turned-off with high current velocity di_C/dt . A very high slope of the falling current is more feasible to induce voltage and current stress on the IGBTs during turn-off. The value of the parasitic inductance, the applied battery voltage and gate turn-off resistor were adjusted to achieve fast switching. Under given circumstances, the IGBTs have to work on the breakdown branch. During current falling time, the collector-emitter voltage of the IGBT rises rapidly.

Fig. 5(a) and (b) shows the simulated short-circuit type 1 switching waveform. The course of collector current, collector-emitter voltage and gate voltage are plotted as a function of time. As far as the gate voltage is higher than the threshold voltage, the IGBT can conduct large saturation currents simultaneously with large applied battery voltage across it during short-circuit. These points can be the stable operating points on the linear region of the IGBT static characteristics. On the other side, a point comes when the gate voltage becomes lower than the threshold voltage. When that happens, the MOS channel below the gate oxide closes and the IGBT stops conducting through this channel. There comes the influence of the NDR (negative differential resistance) branch on device behaviour. From now on, the IGBT is "self-controlled" and the influence of the NDR branch on device behaviour shows a higher impact on the switching behaviour for fast and high-inductive turn-off.

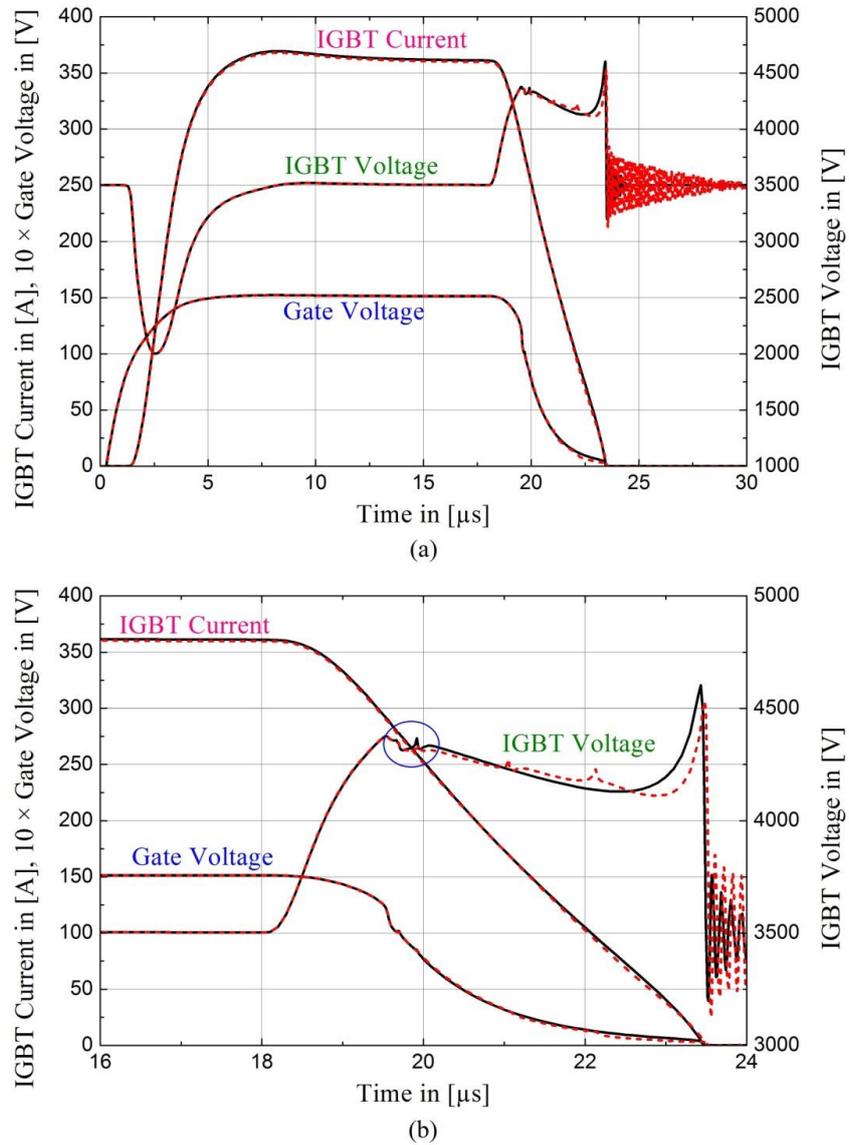


Fig. 5 Simulation of SC turn-off (a) 4-cell model - black lines and 8-cell model - red dashed lines (b) magnified picture $V_{DC} = 3.5$ kV, $L_{par} = 10$ μ H, $R_{G,off} = 30$ Ω , $T = 300$ K

The IGBT operating point is already on the NDR branch of the IGBT due to large voltage overshoot. This NDR phenomenon may be destructive. The working point of the IGBTs comes on this branch only if the gate voltage becomes less than the threshold voltage of the given IGBT, compare with the above shown static I-V characteristics. In this case it is hard for the IGBTs to survive. One of the possible failure pictures was

given in Fig. 3. The demeanours of the current filaments during short-circuit turn-off for the 4-cell and 8-cell are exemplified in Fig. 6(a) and (b) respectively. At the beginning of the short-circuit turn-off event, the gate signal has been set to zero to turn-off the IGBT. The IGBT current starts to fall while the gate voltage approaches to 0 V.

Starting with 4-cell model at time point 19.5 μs , the IGBT is still flowing current through its fully opened n-channel. The base of the IGBT is flooded with charge carriers. The electrons are flowing from emitter to collector and holes opposite to that. The range of the electron and hole density during IGBT conducting state is significantly lower than $1 \times 10^{15} \text{ cm}^{-3}$. The current density in each cell at the p-well has a value of about 1 kA/cm^2 which is quite high. Since the gate voltage is 12.6 V, the IGBT channel is still conducting. The generated overvoltage at this point is about 870 V. The voltage overshoot is superimposed to the battery voltage of 3.5 kV and is blocked by the reversed biased junction at the emitter side. This overvoltage resulted due to high parasitic inductance, understandable from Equation (7). That means the IGBT is working in a breakdown branch of the static characteristics. Nevertheless, there is no destruction phenomenon initiated at this point. This belongs to the stable operating phase during short-circuit turn-off.

Just after 100 ns when the gate voltage reduces from 12.6 V to 10.6 V, the operating point shifts on static characteristics from 12.6 V gate voltage branch to 10.6 V branch. This is a starting of the NDR branch of IGBT output characteristics. Since only a small amount of current flowing through the channel, the remaining current forced to flow directly through p-well. The peak of the electric field at time point 19.6 μs along the reverse biased junction is observed to exceed 250 kV/cm. This high electric field generates large number of electron-hole pairs by avalanche generation at this junction. The remaining charge carriers inside the IGBT base region will conduct the current additionally by means of avalanche generated electron-hole pairs. To get physical understanding for the IGBT destruction, this time point is very important. Only if all IGBT cells carry the same current, this could be a stable operating point otherwise it is the initial point for current filamentation.

At 19.7 μs , the channel is partially closed due to further reduction in gate voltage. Here, a small current is still flowing through the channel which is clearly visible from Fig. 6 at 2nd and 4th cell of the 4-cell IGBT model. At this time point, the values of gate voltage, collector current and collector-emitter voltage are 10.1 V, 277 A and 4335 V respectively. A small kink has been seen in a magnified voltage waveform of a 4-cell IGBT inside the blue circle of Fig. 5(b).

As can be seen from Fig. 6, the current filament is already initiated at first and third cell from left hand side of the IGBT structure. The current density along the third cell at this time point becomes double due to avalanche generated electron-hole pairs. Subsequently, the current filament starts to dominate on a single cell. This means the whole current starts to flow through a single cell due to reduced resistance and thus current crowding. Eventually, at 20 μs only single filament can be seen in one of the active cell in simulation results of the 4-cell IGBT model.

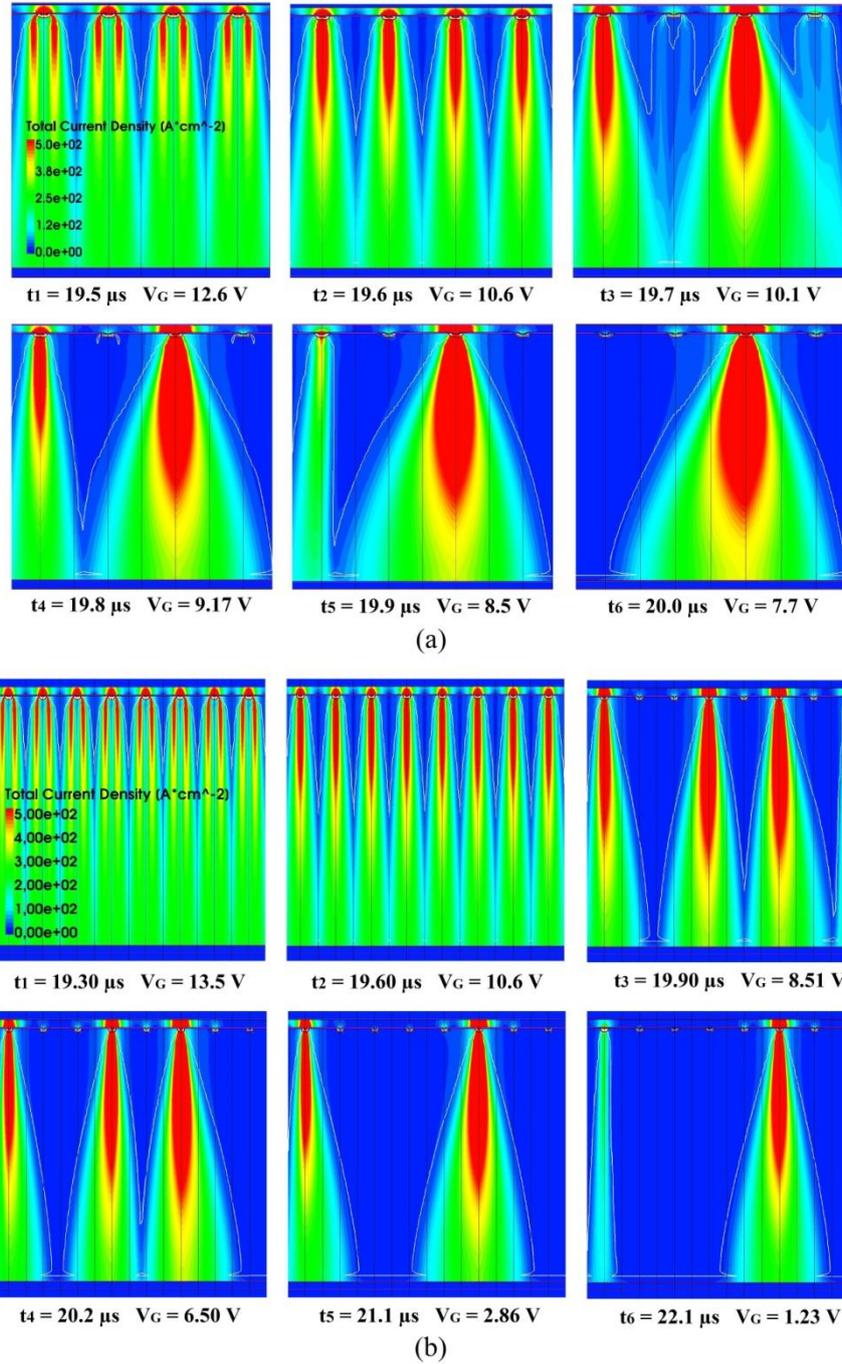


Fig. 6 Filamentation in the IGBT during isothermal simulations (a) 4-cell model and (b) 8-cell model picture $V_{DC} = 3.5 kV$, $L_{par} = 10 \mu H$, $R_{G,off} = 30 \Omega$, $T = 300 K$

The investigation was also done for an 8-cell IGBT model. Similar behaviour was observed for an 8-cell IGBT model simulated again at room temperature. Out of eight cells, the current filament found initially into the four random active cells of the IGBT at 19.90 μs . The intensity of these current filaments is different at each cell. Later, the IGBT current wants to flow through one single cell. Like in the 4-cell IGBT model, the current filament has converged along sixth cell at time 22.1 μs in an 8-cell model. In practice, a very high localized current density increases the temperature inside the IGBT which cannot be seen through the isothermal simulation. Hence, the temperature inclusion into the device simulation should be considered.

To examine the temperature influence on filamentation, thermodynamic simulation was performed utilizing a 4-cell IGBT model. Similar current filament effect was found out through the IGBT simulation. In device simulation, a starting temperature and the pulse width were adjusted to 300 K and 10 μs respectively. This thermodynamic simulation can give more realistic behaviour like in a real application of the IGBT. Fig. 7(a) and (b) show the thermodynamic switching behaviour and the respective demeanour of the current filament. To correlate switching behaviour with the internal IGBT behaviour during turn-off, eight different time points are taken to allege the physical reasons for the IGBT failure. As previously explained, the gate voltage plays a major role during the short-circuit turn-off.

The demeanor of the current filament is shown in Fig. 7(b) by taking eight different points of the switching waveform. At 10.5 μs , the collector-emitter voltage is about 5 kV and the gate voltage is 13.6 V. This large overvoltage is induced due to the falling di_C/dt . The IGBT is working in the avalanche branch due to the high overvoltage. First three time points belongs to the stable operating points on the IGBT static characteristic. In the next time step at 10.75 μs when the gate voltage becomes 9.6 V, the avalanche branch becomes NDR-like and filamentation event occurs. Likewise the previous results of the isothermal simulations, the current filament start to converge into the single active cell. Eventually, the collector current reaches to zero.

The movement of the current filament from time step 11.50 μs to 11.75 μs was ascertained. The filamentation jumping from one cell to other can be related to the temperature compensation point (TCP) of the IGBT transfer characteristics and at the position of the filaments high temperatures are reached. Therefore, the ionization rates are lowered and the avalanche generation decreases. Now the current wants to flow at a cooler region. Thus, the current instability has been analyzed on the IGBT transfer characteristics below TCP point [18]. The maximum temperature observed during the short-circuit turn-off was about 480 K at 11.50 μs . Maximum electric field simulated at this point has reached more than 270 kV/cm. High localized current density and high temperature across a single IGBT cell should be the reason for the found device destruction. During the simulations, an anomalous behaviour of the forming filamentation was investigated under different starting parametric conditions like DC-link voltage, parasitic inductance and temperature.

To improve the short-circuit turn-off ruggedness, the gate turn-off resistor for this case must be chosen well. A trade-off between short-circuit turn-off losses and a stable filament behaviour must be found. In practice, a high resistance is often used for the short-circuit turn-off (e.g. soft-turn-off resistor). A reduced parasitic inductance can additionally lead to a lower generated overvoltage. Furthermore, an active clamping can be used to recharge the gate and thus to overcome the NDR region. Adjustment of bipolar current gain can be one of the possibilities to suppress the NDR influence directly in the semiconductor [6].

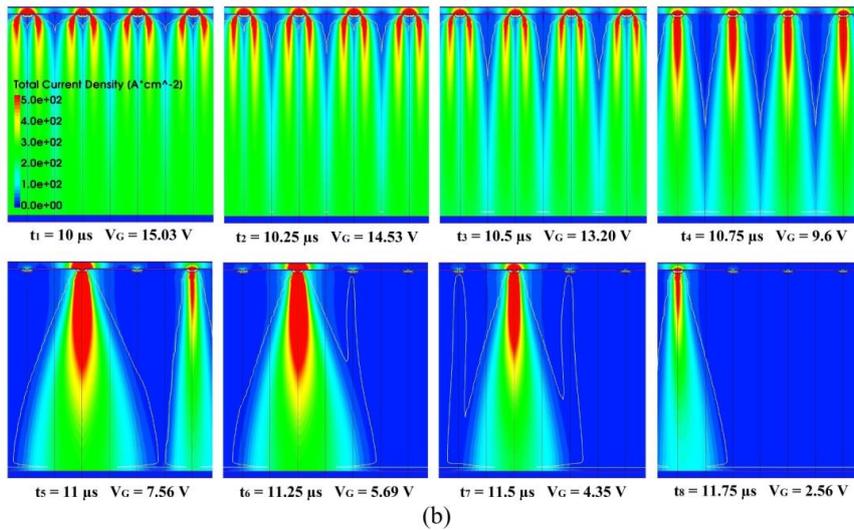
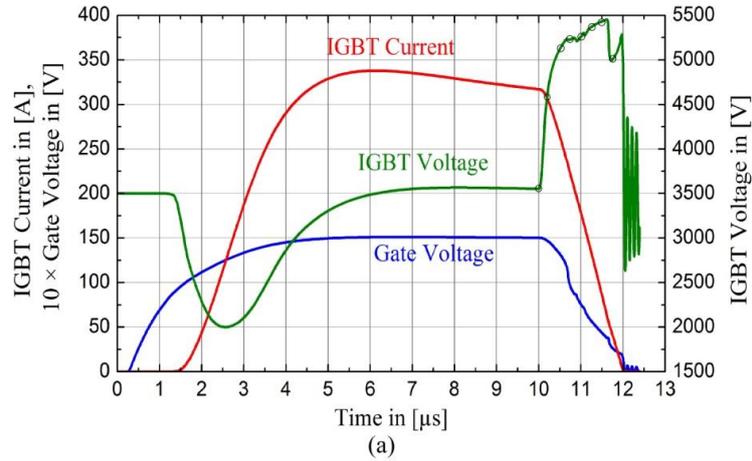


Fig. 7 Thermal simulation of 4-cell IGBT model (a) switching characteristics $V_{DC} = 3.5$ kV, $L_{par} = 10$ μ H, $R_{G,off} = 30$ Ω , starting temperature $T = 300$ K and (b) filamentation behaviour

5. SUMMARY

The investigation concludes that it was possible to measure the I-V characteristics of the IGBT up to the breakdown branch non-destructively. Important facts regarding IGBT failure can be interpreted with the help of this measured output characteristics. The results manifest that the IGBT is able to work on avalanche branch.

The failure analysis can be clearly related to the NDR branch of the I-V characteristics. A stable operating point can be feasible in the avalanche branch of the IGBT during fast turn-off. The destructive event occurs if the IGBT operating points are situated in the

NDR branch during short-circuit turn-off event. IGBTs are able to clamp large overvoltage generated due to high steepness of falling di_C/dt . This clamping mechanism turned out unstable and led IGBT towards destruction. The internal behaviour of the IGBT was analyzed with the help of single pulse short-circuit type 1 simulation.

The found IGBT failure is connected to the inhomogeneous current conduction through the IGBT structure. The complete current was converged at a single cell. A very high localized current density and high temperature were observed with the help of simulation. The results state that both, avalanche branch and negative differential resistance branch are same on the static characteristics. When the IGBT is still conducting current through its MOS channel during short-circuit, no destruction of the device was found. As soon as the MOS channel ended, the operation points are moving into the NDR branch by approaching the IGBT towards destruction. The stability of the short-circuit turn-off can be achieved with adjustment of the bipolar current gain. A high gate turn-off resistor can suppress the filamentation but it will increase the short-circuit turn-off losses. A trade-off has to be found.

REFERENCES

- [1] J. Lutz, H. Schlangenotto, U. Scheuermann and R. D. Donker, *Semiconductor Power Devices Physics, Characteristics, Reliability*. SpringerLink, 2011, Chapter 10, pp. 315-340. DOI: 10.1007/978-3-642-11125-9
- [2] J. Tihanyi, "MOS-Leistungsschalter", ETG-Fachtagung Bad Nauheim, Fachbericht Nr. 23, VDE-Verlag, pp. 71-78, Mai 1988.
- [3] G. Miller, J. Sack, "A new concept for a non punch through IGBT with MOSFET like switching characteristics", Proceedings of the PESC '89, vol. 1, pp. 21-25, June 1989. DOI: 10.1109/PESC.1989.48468
- [4] T. Laska et al, "Short Circuit Properties of Trench/Field Stop IGBTs Design Aspects for a Superior Robustness", Proceedings of the 15th International Symposium on Power Semiconductor Devices & ICs, Cambridge, pp. 152-155, April 2003. DOI: 10.1109/ISPSD.2003.1225252
- [5] T. Basler, R. Bhojani, J. Lutz and R. Jakob, "Measurement of a complete HV IGBT IV characteristic up to breakdown point", 15th European Conference on Power Electronics and Applications (EPE), pp. 1-9, September 2013. DOI: 10.1109/EPE.2013.6634454
- [6] T. Basler, R. Bhojani, J. Lutz and R. Jakob, "Dynamic Self-Clamping at Short-Circuit Turn-off of High-Voltage IGBTs", Proceedings of the 25th International Symposium on Power Semiconductor Devices & ICs, Japan, pp. 277-280, May 2013. DOI: 10.1109/ISPSD.2013.6694440
- [7] T. Basler, J. Lutz, T. Brückner and R. Jakob, "IGBT Self-Turn-off under Short-Circuit Condition", International Seminar on Power Semiconductor, Prague, pp. 235-242, September 2013.
- [8] URLs: https://www.bibliothek.tu-chemnitz.de/uni_biblio/frontdoor.php?source_opus=7514
- [9] T. Basler, J. Lutz, R. Jakob and T. Brückner, "The Influence of Asymmetries on the Parallel Connection of IGBT Chips under Short-Circuit Condition", 14th European Conference on Power Electronics and Applications (EPE), pp. 1-8, September 2011.
- [10] URLs: http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=6020357
- [11] M. Rahimo, A. Kopta, S. Eicher, U. Schlapbach, and S. Linder, "Switching-self-clamping-mode "SSCM", a breakthrough in SOA performance for high voltage IGBTs and diodes", Proceedings of the 16th International Symposium on Power Semiconductor Devices & ICs, Japan, pp. 437-440, May 2004. DOI: 10.1109/ISPSD.2004.1332970
- [12] H. G. Eckel and L. Sack, "Experimental Investigation on the Behaviour of IGBT at Short-Circuit during the On-state", 20th International Conference on Industrial Electronics, Control and Instrumentation (IECON), vol. 1, pp. 118-123, September 1994. DOI: 10.1109/IECON.1994.397762
- [13] Lutz J, Döbler R, Mari J, Menzel M: "Short Circuit III in High Power IGBTs" Proceedings EPE, Barcelona (2009) URLs: http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=5279057
- [14] J. Lutz and T. Basler: "Short-Circuit Ruggedness of High-Voltage IGBTs", 28th International Conference on Microelectronics (MIEL), pp. 243-250, May 2012. DOI: 10.1109/MIEL.2012.6222845

- [15] T. Balsler, "Short-Circuit Ruggedness of High-Voltage IGBTs", PhD Thesis, Technische Universität Chemnitz, February 2014.
- [16] URLs: http://www.qucosa.de/fileadmin/data/qucosa/documents/14710/Dissertation_Thomas_Basler.pdf
- [17] R. Bhojani, "Simulation of High-Voltage IGBTs in Short-Circuit and Avalanche Mode", Master Thesis, Technische Universität Chemnitz, April 2013.
- [18] P. Rose, D. Silber, A. Porst and F. Pfirsch, "Investigations on the Stability of Dynamic Avalanche in IGBTs", Proceedings of the 14th International Symposium on Power Semiconductor Devices & ICs, New Mexico, pp. 165-168, June 2002. DOI: 10.1109/ISPSD.2002.1016197
- [19] T. Raker, H. Felsl, F. Niedernostheide, F. Pfirsch, and H. Schulze, "Limits of Strongly Punch Through Designed IGBTs", Proceedings of the 23rd International Symposium on Power Semiconductor Devices & ICs, U.S.A., pp. 100-103, May 2011. DOI: 10.1109/ISPSD.2011.5890800
- [20] Z. Chen, K. Nakamura and T. Terashima, "LTP(II)-CSTBTTM(III) for High Voltage Application with Ultra Robust Turn-off Capability Utilizing Novel Edge Termination Design", Proceedings of the 24th International Symposium on Power Semiconductor Devices & ICs, Belgium, pp. 25-28, June 2012. DOI: 10.1109/ISPSD.2012.6229014
- [21] D. Dibra, M. Stecher, S. Decker, A. Lindemann, J. Lutz and C. Kadow, "On the Origin of Thermal Runaway in a Trench Power MOSFET", *IEEE Trans. on Electron Devices*, vol. 58, pp. 3477–3483, October 2011. DOI: 10.1109/TED.2011.2160867