**FACTA UNIVERSITATIS**
Series: **Electronics and Energetics** Vol. 33, Nº 2, June 2020, pp. 317-326
https://doi.org/10.2298/FUEE2002317S

# A SINGLE POWER SUPPLY 0.1-3.5 GHZ LOW NOISE AMPLIFIER DESIGN USING A LOW COST 0.5 µM D-MODE PHEMT PROCESS *

**Denis Sotskov, Vadim Elesin, Alexander Kuznetsov, Nikolay Usachev, Nikita Zhidkov, Alexander Nikiforov**

[1]National Research Nuclear University MEPhI (Moscow Engineering Physics Institute), Moscow, Russian Federation
[2]Specialized Electronic Systems, Moscow, Russian Federation

**Abstract**. *Design and testing results of a single power supply wide-band low noise amplifier (LNA) based on low cost 0.5 µm D-mode pHEMT process are presented. It is shown that the designed cascode LNA has operating frequency range up to 3.5 GHz, power gain above 15 dB, noise figure below 2.2 dB, output linearity above 17 dBm and power consumption less than 325 mW. Potential immunity of the LNA to total ionizing dose and destructive single event effects exceed 300 krad and 60 MeV·cm$^2$/mg respectively.*

**Key words**: *low noise amplifier (LNA), pseudo high-electron mobility transistor (pHEMT), cascode, radiation tolerance*

## 1. INTRODUCTION

Low noise amplifier (LNA) is an important functional unit in receiver paths of communication, radar and navigation systems. LNA parameters determine the sensitivity (noise figure), power gain and input linearity ($P_{1dB}$) of the receiver [1-3].

Nowadays mass-produced LNA IC's are manufactured with III-V and silicon based technologies using the following devices: GaAs depletion (D-) or enhancement (E-) mode pseudo high-electron mobility transistor (pHEMT); GaN high-electron mobility transistor (HEMT); GaAs and SiGe heterojunction bipolar transistors (HBT).

D-mode pHEMT process has become a good choice for LNA design because of transistor low noise figure, high cut-off frequency (Ft) and appropriate fabrication costs [4]. In addition, low sensitivity of pHEMT to total ionizing dose (TID) and single event effects

Received September 26, 2019; received in revised form December 29, 2019
**Corresponding author:** Denis Sotskov
National Research Nuclear University MEPhI (Moscow Engineering Physics Institute); Specialized Electronic Systems, Moscow, Russian Federation
E-mail: disot@spels.ru
*An earlier version of this paper was presented at the 31st International Conference on Microelectronics (MIEL 2019), September 16-18, 2019, in Niš, Serbia [1].

(SEE) makes them promising for space applications [5, 6]. A disadvantage of a D-mode pHEMT based LNA is a negative bias supply requirement, which limits the possible field of applications [2, 7]. Meanwhile, the conventional approach to single positive supply LNA design on D-mode pHEMT is based on self-biasing [2].

The purpose of this work was design, manufacturing, and testing of LNA with a single positive supply and 0.1-3.5 GHz operation frequency range using a low cost 0.5 μm D-mode pHEMT process [8].

## 2. LNA DESIGN

Wide-band (multi-octave) LNA's are designed using various architectures including distributed (traveling-wave), balanced and resistive feedback configurations [9]. The resistive feedback is widely used to achieve tradeoff among several LNA performances (operated frequency range, noise figure, gain, gain flatness, linearity, VSWR, power consumption) [9, 10]. Among the possible configurations based on resistive feedback, cascode LNA can provide not only flat gain and power over its operating band but also flat linearity in the same band and higher output impedance (better wide-band potential) [11]. Therefore the single positive power supply cascode LNA based on resistive feedback configuration and self-biasing techniques are presented in this work.

LNA was implemented in D-mode pHEMT 0.5 μm process with Ft up to 35 GHz and minimum noise figure (NFmin) is 1.2 dB at 8 GHz. The LNA circuit schematic is shown in Fig. 1.

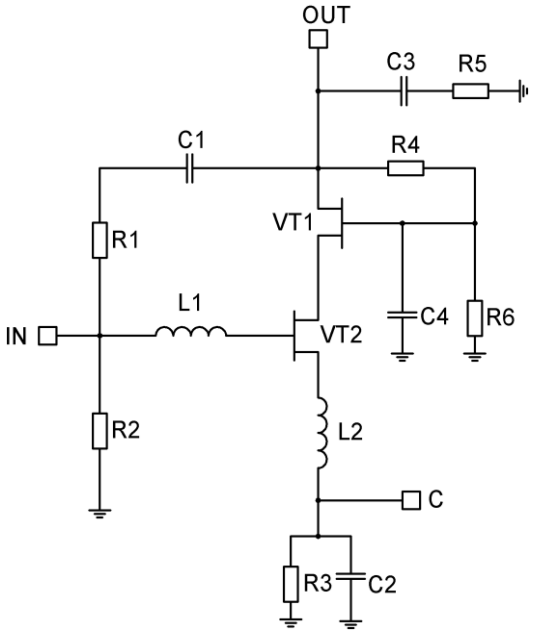


**Fig. 1** Simplified circuit of the LNA

The amplifier is composed of cascoded input (VT2) and output (VT1) transistors with the same width of 4×150 μm. Series feedback (resistor R3, capacitor C2, inductor L2) and parallel feedback (capacitor C1, resistor R1) are used to provide stability and gain flatness in a wide frequency range. It should be noted what cascode transistor with capacitance connected to the gate terminal forms a Collpits oscillator. A damping resistor should be added to the gate of the cascode transistor to decrease parasitic resonator quality factor in order to improve amplifier stability [12].

LNA is designed with a single positive voltage supply 5 V. Resistor R2, resistive divider implemented by R4-R6 and self-bias circuit R3 provide required transistors operation point. The input matching network consists of integrated spiral inductors L1 and L2. The output matching network consists of capacitor C3 and resistor R5.

Circuit parameters optimization was carried out in a computer aided design (CAD) tool using the technique presented in [13], which allows determining the operating current, the width of the transistors and parameters of the matching networks, providing optimal values of the gain, noise figure and return loss.

The LNA's area is 2.15×1.65 $mm^2$ and includes additional pad "C" needed to connect external bypass capacitors for enhanced performance at frequencies below 0.5 GHz.

## 3. LNA PERFORMANCES

### 3.1. Simulation and measurement setups

Simulation has been performed using scalable pHEMT non-linear model and linear models for microstrip lines, inductors, T-shapes, vias and pads based on scattering (S-) parameters measurement verified up to 20 GHz and provided by foundry [8].

Measurements have been performed on the wafer for a significant amount (above 50) of LNA chips using a specialized microwave test system, based on Cascade semi-automated probe station, vector network analyzer (VNA) and signal (spectrum) analyzer with noise figure measurement option described in [14]. The experimental setup used for LNA dies testing is shown in Fig. 2. According to the test procedure, S-parameters and $P_{1dB}$ (linearity) are measured at 5 V supply, the noise figure is measured at 3 V supply.

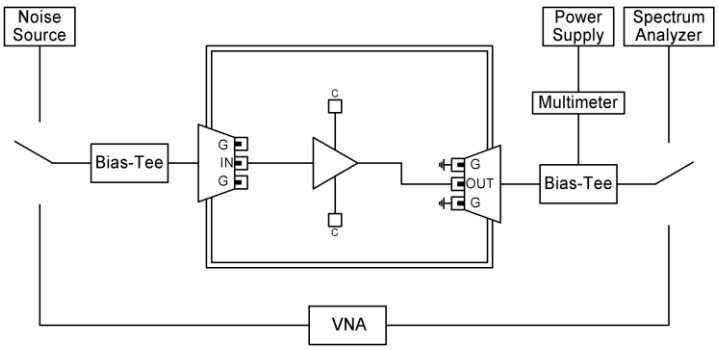


**Fig. 2** Experimental setup based on the microwave probe station

### 3.2. Simulation and measurement results

The simulated and measured LNA chip performances (gain, noise figure, $P_{1dB}$, etc.) are shown in Fig. 3 and Fig. 4. The measured and simulated results are in good agreement in the frequency range 0.5-3.5 GHz, and demonstrate that LNA has power gain above 15.3 dB, noise figure below 2.2 dB, output $P_{1dB}$ above 17 dBm (F = 1.5 GHz).

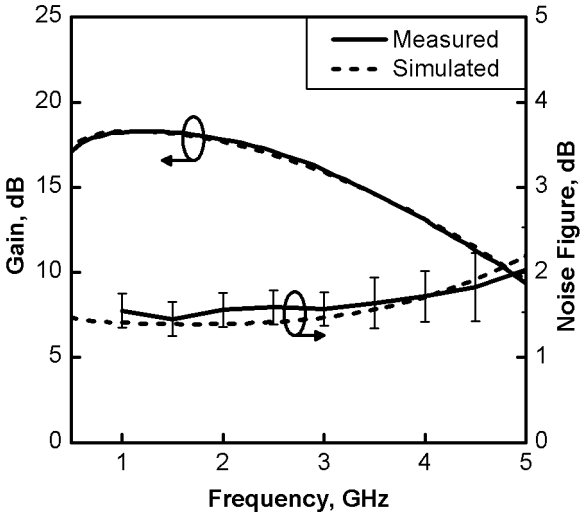


**Fig. 3** Simulated and measured LNA gain and noise figure versus frequency

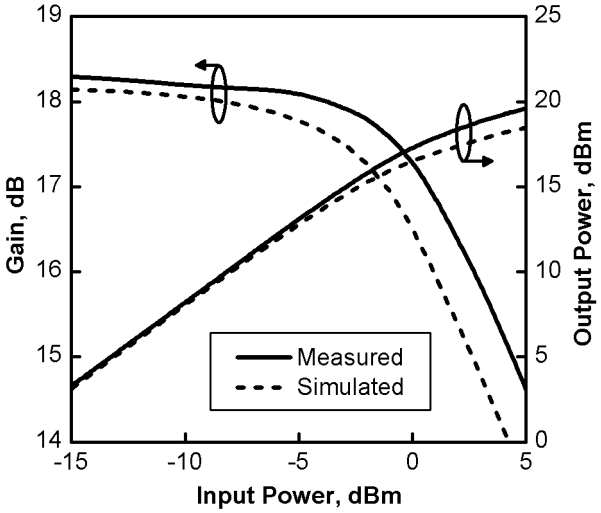


**Fig. 4** Simulated and measured LNA gain and output power versus input power

### 3.3. Model accuracy estimation

The simulation results relative error estimation was carried out with the following expression:

$$\delta_X = \{|Xm\text{-}Xs|/Xm\}\cdot 100\%, \quad (1)$$

where Xm and Xs are the measured and simulated gain and noise figure values respectively.

According with a small-signal analysis the relative gain error and the noise figure error do not exceed 3 % (frequency range 0.5-3.5 GHz) and 4 % (frequency range 1-3.5 GHz) respectively, that confirms pHEMT model accuracy. The relative input $P_{1dB}$ error does not exceed 15 % (F = 1.5 GHz) for the worst case, the typical value is less than 5 %.

### 3.4. Parameters variation estimation

The coefficient of variation estimation was carried out with the following expression:

$$V_X = \{\sigma/\bar{X}\}\cdot 100\%, \quad (2)$$

where σ and $\bar{X}$ are a standard deviation and mean (average) values respectively.

On wafer measurement results showed that the coefficient of variation does not exceed 1.3 % for gain (frequency range 0.5-3.5 GHz), 0.5 % for noise figure (frequency range 1-3.5 GHz) and 2.8 % for current consumption.

### 3.5. Special measurement test-fixture

Special test-fixture based on RO4003C laminate has been designed and implemented to provide LNA performance measurements especially under extreme temperature and ionizing radiation exposure. The special measurement test-fixture schematic and photograph are shown in Fig. 5 and Fig. 6 respectively. External capacitors C2 and C3 can be used to improve LNA performance at frequencies below 0.5 GHz.

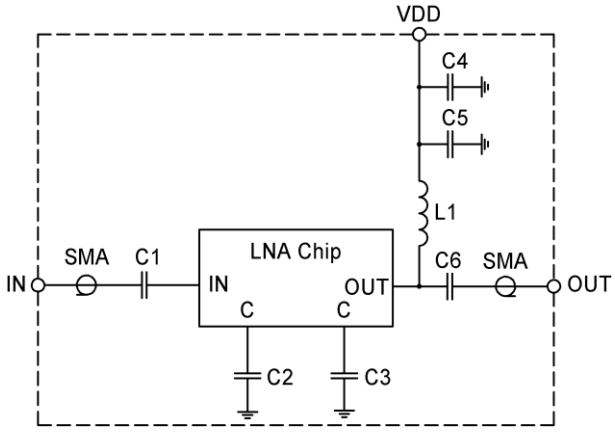


**Fig. 5** Special measurement test-fixture schematic

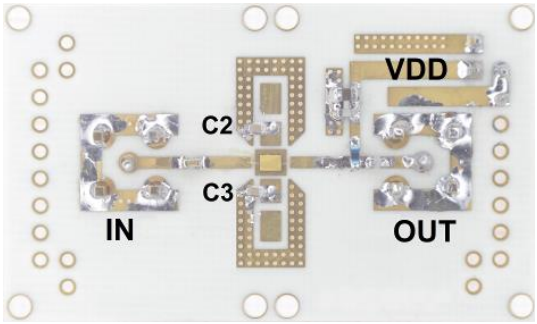


**Fig. 6** Special measurement test-fixture photograph

### 3.6. Low-frequency applications

Measurement of low-frequency S-parameters and noise figure were performed at 5 V and 3V supply (VDD) respectively using special test-fixture (see Fig. 5, 6) and microwave test system operating up to 26 GHz [14].

Measured LNA low-frequency performance with and without mounted 1 nF SMD capacitors C2 and C3 are shown in Fig. 7. Dependencies in Fig. 7 demonstrate that at frequency 100 MHz power gain and noise figure have been improved by more than 10 dB and 5 dB respectively.

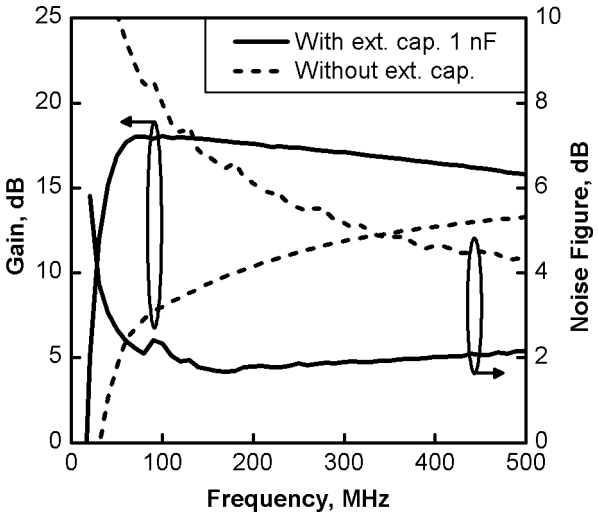


**Fig. 7** Measured LNA gain and noise figure versus frequency

### 3.7. Parameters variation over temperature range

The LNA parameters measurement results in the ambient temperature range from -60 °C to +125 °C and frequency 1 GHz are shown in Fig. 8 and Fig. 9. The gain value monotonically decreases with increasing ambient temperature, the gain change does not

exceed 2 dB. The noise figure monotonically increases with increasing ambient temperature, the variation in the noise figure does not exceed 1.3 dB. The output linearity (output $P_{1dB}$) monotonically decreases with increasing ambient temperature, the output $P_{1dB}$ shift does not exceed 2 dB in the temperature range. The current consumption change in the considered ambient temperature range does not exceed 3.8 mA.

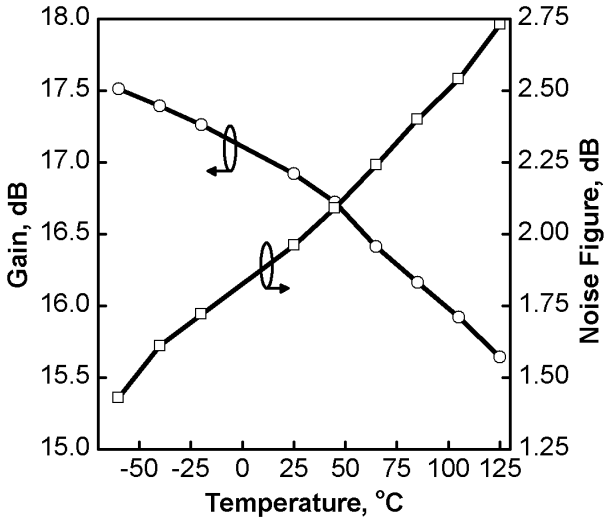


**Fig. 8** Measured LNA gain and noise figure at 1 GHz versus temperature

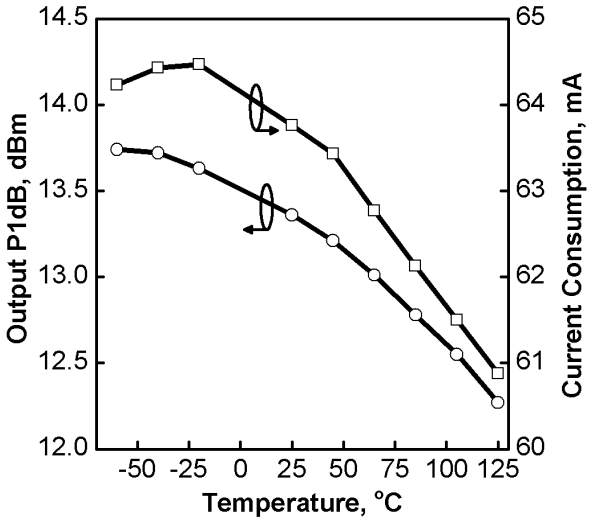


**Fig. 9** Measured LNA output $P_{1dB}$ at 1 GHz and current consumption versus temperature

### 3.8. Radiation tolerance estimation

A radiation tolerance estimation have been performed by SPELS / NRNU MEPHI test center for the typical test structures: transistor and C-band two-stage LNA implemented in given D-mode pHEMT 0.5 μm process.

The experimental research of the test structures under TID irradiation have been performed using Cs-137 "Panorama-MEPhi" irradiation facility [15, 16]. Heavy ion irradiation have been performed at the facility based on U400M heavy-ion cyclotron of the Joint Institute for Nuclear Research (JINR, Dubna, Russia).

According to the test results, up to an equivalent gamma dose of 300 krad, no parameter degradation of the test structures is observed. Destructive SEE (SEL, SEB and other) have not been observed for heavy ions exposure with LET up to 60 MeV·cm$^2$/mg.

### 3.9. Performance summary

The LNA's measured performance is summarized in Table 1 compared to its commercially available analogues implemented in different processes (GaAs pHEMT, GaAs HBT, GaN HEMT, and SiGe HBT).

**Table 1** LNA's Performance Summary

| LNA | This Work | TGA5108 | HMC395 | QPL1002 | SGL0622Z |
|---|---|---|---|---|---|
| Company | | Qorvo (TriQuint) | Analog Dev. (Hittite) | Qorvo | Qorvo (RFMD) |
| Process | 0.5 μm GaAs D-pHEMT | 0.5 μm GaAs E/D-pHEMT | GaAs HBT | 0.25 μm GaN HEMT | SiGe HBT |
| Configuration | cascode | cascode | Darlington | cascode | – |
| Operating Frequency[GHz] | 0.5 …3.5 | 0.5…3.5 | 0.5…3.5 | 0.5…3.5 | 0.5…3.5 |
| Gain [dB] | 15.3 | 15.0 | 14.3 | 16.1 | 18.7 |
| Gain Flatness [dB] | 4 | 7 | 2 | 3 | 14 |
| Noise Figure [dB] | 2.2 | 2.2 | 5.0 | 1.6 | 3.2 |
| Output $P_{1dB}$ [dBm] (F = 1.5 GHz) | 17 | 20 | 15 | 23 | 6 |
| Gain Temperature Coefficient [dB/°C] | -0.011 | -0.011 | -0.008 | -0.022 | -0.034 |
| Noise Figure Temperature Coefficient [dB/°C] | 0.007 | 0.005 | 0.012 | 0.016 | 0.010 |
| Power consumption [mW] | 325 | 425 | 270 | 600 | 36 |
| Chip size [mm$^2$] | 2.15×1.65 | 1.49×0.85 | 0.38×0.58 | in package | in package |
| Negative bias supply requirement | no | no | no | yes | no |
| FOM [arbitrary unit] | 0.60 | 0.66 | 0.14 | 1.55 | 0.08 |

In order to compare the presented LNA's, a Figure of Merit (FOM) is introduced as a function of gain (G), gain flatness (ΔG), noise figure (NF), output $P_{1dB}$ ($OP_{1dB}$), gain temperature coefficient (δG), noise figure temperature coefficient (δNF), power consumption ($P_{DC}$) and operating temperature range (ΔT):

$$FOM = \frac{G \cdot OP_{1dB}}{(NF-1) \cdot P_{DC} \cdot \Delta G \cdot 10^{\frac{|\delta G| \cdot \Delta T}{20}} \cdot 10^{\frac{|\delta NF| \cdot \Delta T}{10}}}, \quad (3)$$

where G, ΔG, NF are in arbitrary units; $OP_{1dB}$ and $P_{DC}$ are in mW; δG and δNF are in dB/°C; ΔT = 125 °C (-40 – +85 °C).

According to Table 1, the presented single power supply LNA implemented in 0.5 µm D-mode pHEMT process shows similar performance as compared with LNA based on 0.5 µm GaAs E/D-pHEMT and better noise figure, output $P_{1dB}$ and FOM compared with LNA's based on GaAs and SiGe HBTs. LNA implemented in 0.25 µm GaN HEMT shows superior performance but required a negative bias supply.

## 4. Conclusion

The single power supply wide-band low noise amplifier design approach was considered with respect to the low cost 0.5 µm D-mode pHEMT process. It was demonstrated that the designed LNA's performance in the frequency range 0.5 - 3.5 GHz is not inferior to commercially available single power supply analogues implemented in more expensive GaAs pHEMT, GaAs HBT and SiGe HBT processes.

It is also important to note, that this low cost process is equipped with a proper design kit (models accuracy, low process variations) and is also a good choice for LNA's and control circuits (switches, attenuators, phase shifters) radiation tolerant design for space applications, providing TID (total ionizing dose) and LET (single event effects) up to 300 krad and 60 MeV·cm$^2$/mg respectively.

**Acknowledgment:** *This work was supported in accordance with agreement between Ministry of Education and Science of the Russian Federation and National Research Nuclear University MEPhI № 8.2373.2017/4.6.*

## References

[1] D.I. Sotskov, N.A. Usachev, V.V. Elesin, A. G. Kuznetsov, K.M. Amburkin, G. V. Chukov, M. I. Titova, N. M. Zidkov, "D-pHEMT 0.5 um Process Characterization to Wide-Band LNA Design", In Proceedings of the 31th Int. conf. on microelectronics (MIEL 2019), 2019, pp. 99–102.

[2] G. Gonzalez. *Microwave Transistor Amplifiers: Analysis and Design.* 2nd ed. Pearson. 1996. 528 p.

[3] N. Usachev, V. Elesin, A. Nikiforov, G. Chukov, G. Nazarova, D. Sotskov, N. Shelepin, V. Dmitriev "System Design Considerations of Universal UHF RFID Reader Transceiver ICs", *Facta Universitatis, Series: Electronics and Energetics*, vol. 28, no. 2, pp. 297–307, 2015.

[4] G.D. Vendelin, A.M. Pavio, U.L. Rohde. *Microwave Circuit Design Using Linear and Nonlinear Techniques*. John Wiley & Sons Ltd, 2005, 1058 p.

[5] D.V. Gromov, V.V. Elesin, S.A. Polevich, et al. "Ionizing-Radiation Response of the GaAs/(Al, Ga)As PHEMT: A Comparison of Gamma- and X-ray Results", *Russian Microelectronics*, vol. 33, no. 2, 2004, pp. 111–115.

[6] G.V. Chukov, V.V. Elesin, G.N. Nazarova, A.Y. Nikiforov, D.V. Boychenko, V.A. Telets, A.G. Kuznetsov, K.M. Amburkin, "SEE testing results for RF and microwave ICs", In Proceedings of the 2014 IEEE Radiation Effects Data Workshop, 2014, pp. 233–235.

[7] H.-C. Chiu et al., "Enhancement- and Depletion-Mode InGaP/InGaAs pHEMTs on 6-Inch GaAs Substrate", In Proceedings Asia-Pacific Microwave Conference, 2005, pp. 1–4.

[8] O.R. Fazylkhanov, I.S. Pushnitsa, S.I. Strelnikov, M.A. Kalyakin, A.H. Filaretov, "Process Design Kit verification - methodology and practice", 2017, *Crimico*, pp. 143–149.
[9] I.J. Bahl. *Fundamentals of RF and Microwave Transistor Amplifiers*. John Wiley & Sons. 2009. 671 p.
[10] G. Wang, J. Liu et al., "The Design of Broadband LNA with Active Biasing based on Negative Technique", *Journal of Microelectronics, Electronic Components and Materials*, vol. 48, no. 2, pp. 115–120, 2018.
[11] J.P. Conlon, N. Zhang, M.J. Poulton et al., "GaN wide band power integrated circuits", *IEEE Compound Semiconductor Integrated Circuit Symposium (CSIC)*, 2006, pp. 85–88.
[12] Bagher Afshar, Ali M. Niknejad. "X/Ku Band CMOS LNA Design Techniques", *IEEE Custom Integrated Circuits Conference*, 2006, pp. 389–392.
[13] G.N. Nazarova, V.V. Elesin, D.I. Sotskov, "An approach to low noise amplifier optimization in Advanced Design System CAD", IT Security (Russia), 2016, vol. 23, no. 3, pp. 53–59.
[14] D.I. Sotskov, V.V. Elesin, K.M. Amburkin, G.N. Nazarova, N.A. Usachev, A.Y. Nikiforov, "Design and Testing Issues of a High-Speed SOI CMOS Dual-Modulus Prescaler for Radiation Tolerant Frequency Synthesizers", In Proceedings of the 30th Int. conf. on microelectronics (MIEL 2017), 2017, pp. 329–332.
[15] A.S. Artamonov, A.A. Sangalov, A.Y. Nikiforov, V.A. Telets, D.V. Boychenko, "The New Gamma Irradiation Facility at the National Research Nuclear University MEPhI", In Proceedings of the IEEE Radiation Effects Data Workshop, 2014, pp. 258–261.
[16] D. Boychenko, O. Kalashnikov, A. Nikiforov, A. Ulanova, D. Bobrovsky, P. Nekrasov. "Total ionizing dose effects and radiation testing of complex multifunctional VLSI devices", *Facta Univesitatis, Series: Electronics and Energetics*, vol. 28, no. 1, pp. 153–164, 2015.