FACTA UNIVERSITATIS
Series: **Electronics and Energetics** Vol. 34, Nº 1, March 2021, pp. 115-131
https://doi.org/10.2298/FUEE2101115P

Original scientific paper

SYNTHESIS OF COMPOSITE LOGIC GATE IN QCA EMBEDDING UNDERLYING REGULAR CLOCKING

Jayanta Pal[1], Dhrubajyoti Bhowmik[2,a], Ayush Ranjan Singh[2,b], Apu Kumar Saha[2,c], Bibhash Sen[3]

[1]Department of Information Technology, Tripura University, Agartala, Tripura, India
[2]Department of {[a]CSE, [b]EE, [c]Mathematics}, NIT Agartala, Barjala, Tripura, India
[3]Department of CSE, National Institute of Technology, Durgapur, West Bengal, India

Abstract. *Quantum-dot Cellular Automata (QCA) has emerged as one of the alternative technologies for current CMOS technology. It has the advantage of computing at a faster speed, consuming lower power, and work at Nano- Scale. Besides these advantages, QCA logic is limited to its primitive gates, majority voter and inverter only, results in limitation of cost-efficient logic circuit realization. Numerous designs have been proposed to realize various intricate logic gates in QCA at the penalty of non-uniform clocking and improper layout. This paper proposes a Composite Gate (CG) in QCA, which realizes all the essential digital logic gates such as AND, NAND, Inverter, OR, NOR, and exclusive gates like XOR and XNOR. Reportedly, the proposed design is the first of its kind to generate all basic logic in a single unit. The most striking feature of this work is the augmentation of the underlying clocking circuit with the logic block, making it a more realistic circuit. The Reliable, Efficient, and Scalable (RES) underlying regular clocking scheme is utilized to enhance the proposed design's scalability and efficiency. The relevance of the proposed design is best cited with coplanar implementation of 2-input symmetric functions, achieving 33% gain in gate count and without any garbage output. The evaluation and analysis of dissipated energy for both the design have been carried out. The end product is verified using the QCADesigner2.0.3 simulator, and QCAPro is employed for the study of power dissipation.*

Key words: *Composite Gate, Regular Clocking, 2-input Symmetric Function, QCA, RES Clocking, Basic Gates, Energy Dissipation.*

1. INTRODUCTION

The performance of CMOS technology degrades due to its high-power consumption, high leakage current, quantum effects & feature size. It leads International Technology & Roadmap for Semiconductors (ITRS) to make a noteworthy and viable alternative to

Received August 1, 2020; received in revised form September 5, 2020
Corresponding author: Jayanta Pal
Department of Information Technology, Tripura University, Suryamaninagar, Tripura, , India
E-mail: jayantapal@tripurauniv.in

CMOS VLSI. In this context, Quantum-dot Cellular Automata (QCA) [1] is considered as one of the rising nanotechnologies to invalidate the restrictions of current CMOS VLSI [2]. QCA employs the use of Quantum Dots rather than transistors, used in CMOS. The circuit design in QCA enjoys low power dissipation [3] and high operational speed at Nanoscale [4]. The transmission and distribution of information in QCA occur with the position of electron and the interaction of cells in the presence of a clock signal. It does not involve any flow of electrons, as in the case of CMOS. The basic structural components of QCA based architecture are 3-input majority gate (MV) [5, 6], Inverter [7, 8] and Array of Cells [9, 10]. Besides, the fan-out assumes a significant role in signal splitting for the substantial implementation of QCA arrays [11].

Four-Phase clocking [12] namely: Switch, Hold, Release and, Relax phases is used to control the direction of signal propagation. The purpose of these phases is to allow or deny the tunneling of the confined electrons in a QCA cell and achieve a stable logic state. Any complex circuit can be implemented in QCA based technology with these basic primitives [13–16]. However, the QCA logic design is limited to the Majority Voter gate and inverter only and it hampers the cost-effective logic synthesis [17]. A minimization of functional logic blocks is preferred in the realization of a sophisticated QCA logic design. A Composite Logic Gate (CG) allows the maximum realization of logic functions and reduces the circuit complexity & QCA cost. The use of an underlying regular clocking is essential for the design, considering the timing issue for an error-free and high-performance behavior [18, 19].

Few attempts have been made to address the regular clocking related issue [18–20]. However, 2DDWave [20] lacks proper feedback path realization and USE clocking [18] lacks multi-directional information flow although it addresses the issue of feedback as in [20]. The issues were adequately tackled in [19] with a robust, efficient and scalable (RES) scheme introducing multi-input based clock zone.

The researchers have proposed numerous designs employing regular clocking [18–21] and also without regular clocking [22–27]. Most of the designs have utilized more than two logic outputs of the primitive gate. Nevertheless, no design has been reported to consider producing all possible primary logic functions for the given input. Although researches in the field of QCA technology have proposed and presented many remarkable designs. In most cases, they did not take into account the vital use of the underlying regular clock. As a result, they ended up with the cell layout with irregular clocking zones. Such irregular clocking has made it more challenging to provide an easy construct in terms of fabrication. At the same time, the regular clocking scheme should be well-defined and regular.

A Composite Gate (CG) is capable of generating all possible logic gates like AND, NAND, Inverter, OR, NOR, XOR and XNOR for the given inputs. This paper aims to design a low-cost QCA gate to realize all possible logic operations and design the same using the RES clocking scheme. Until now, no previous attempt is made to realize a CG with such flexibility and functionality. On the other hand, the synthesis of symmetric boolean functions is an essential aspect in cryptology [28] and it draws considerable attention of the researchers in QCA. Different designs and techniques to synthesize symmetric functions can be seen in [29–33]. The proposed CG can be utilized as the better choice for the synthesis of two-input symmetric functions. The salient features of the proposed work are as follows:

- A composite gate is proposed, in order to produce all logic gates in a single unit.
- A regular clocking scheme (RES) is applied to ensure the design's scalability and efficiency.
- The design capability of the circuit has been investigated.

- The cost-efficiency of the circuit is evaluated.
- The energy dissipation has also been evaluated for both the design (with & without regular clock).

The remaining part of the paper is arranged in the following order: Section 2 discusses the basics of QCA. In section 3, the different proposals and designs for underlying clocking schemes are discussed. The Composite Gate's basics, the circuit proposed in QCA and the simulated result are presented in section 4. The performance and applicability analysis has been discussed in section 5. The analysis for the power dissipation of the proposed design is discussed in section 6. Section 7 deals with concluding part of the article.

2. QUANTUM-DOT CELLULAR AUTOMATA

In this section, the basic design and working principle of Quantum-dot Cellular Automata (QCA) technology are discussed. A square-shaped QCA cell consists of two electrons residing in two of the four quantum dots inside it. The information flows with the effect of coulombic repulsion force between the electrons and the electron moves between the neighboring dots via tunneling [34] but not between the neighboring cells due to high inter-cell potential.

2.1. QCA Basic Structure

According to the alignment or the position of electrons in the QCA cell, it can either be in one of the two polarization states. One in polarization +1 (binary logic 1) and the other in polarization -1 (binary logic 0). Likewise, according to the QCA dots' position, the cell can be 900 cells or 450 cells. The electrons endeavor to maintain maximum distance placed diagonally because of the coulombic repulsion force, as depicted in Fig. 1(a). The polarization energy for each cell (say P) can be formulated with Eq. 1 as follows.

$$P = \frac{(p_1 + p_3) - (p_2 + p_4)}{(p_1 + p_2 + p_3 + p_4)} \tag{1}$$

Where p_i represents the probability of the presence of an electron in the i^{th} quantum dot [35].

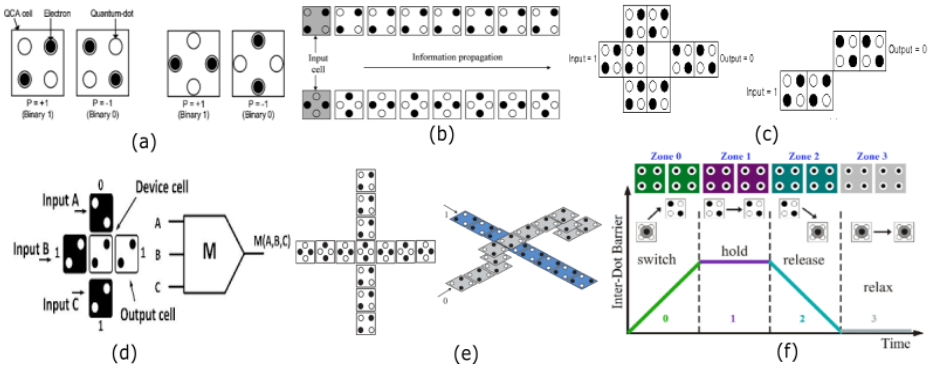


Fig. 1 Basic structural components of QCA.

The QCA cells are set alongside one another to shape a QCA wire, and the data propagates through it. The Coulombic repulsion force between electrons makes the last cell's polarization in the array to have the same value as the first one in the array. It can also be opposite polarization, depending on the structure [36]. There can be two different structures of QCA wire (Fig. 1(b)). The inverter (NOT Gate) can have two ways of implementation (Fig. 1(c)), and it is used as and when the reverse polarized value of a cell is to be used.

The basic building block for most of the QCA based circuits is Majority Voter Gate (MV) and Inverter. The functional logic of MV with three inputs A, B, and C can be represented in Eq. 2. It is designed with 5 QCA cells, with three inputs, one device cell and one output cell (Fig. 1(d)).

$$M(P,Q,R) = PQ + QR + RP \tag{2}$$

To propagate the data through the intersecting point of the wires, two commonly known wire crossing exist in QCA: coplanar approach [37] and multi-layer approach [38, 39]. The crossover can also be achieved in either of three (3) ways by proper placing of clock zones. It can also be implemented using two types of QCA wires (90^0 cells and 45^0 cells) crossed vertically and horizontally. On the other hand, a multi-layer wire crossing can be implemented applying different single layers created one above another (Fig. 1(e)). Still, it is not a suitable approach from a fabrication point of view.

2.2. QCA Clocking

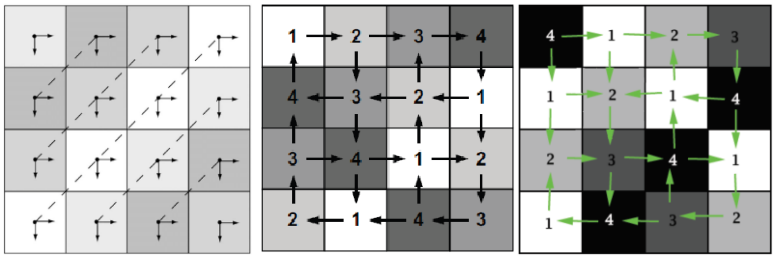
Apart from the basic building blocks in QCA design, it is also essential to have an appropriate synchronization of clock signals with the majority gate with optimization in delay. The QCA signals are driven by four clock phases, such as the Switch phase, Hold phase, Release phase, and Relax phase. QCA cells in a circuit should be organized in terms of consecutive clocking zones with proper synchronization employing some added cells [40] (see Fig. 1(f)).

The inter-dot potential barrier gradually increases between the QCA cells during the switch phase, which leads the input cell to interconnect with the neighbor cells, which results in a polarized state [41]. Palpable computation is achieved in this phase. The barrier becomes high during the hold phase and prevents the tunneling of electrons between the dots. The barrier recurrently decreases in the release phase. On reaching its least value in the relax phase, the cell polarization loses its polarized value entirely and does not indulge any impact on neighboring cells.

3. Related Work

Usually, the QCA design follows the rule of considering minimum or maximum value in cell count in a particular clocking zone. However, it does not justify the design, and also the proper use of clocking phases is ignored, which leads to the need for appropriate use of well defined, underlying, and regular clocking schemes. In this regard, several works have been proposed and presented as reported in [42–45], but none of them have considered a regular layout of the underlying clocking scheme. It will not just help enhance the performance of the design, but also ensure the scalability, reliability, and ease of fabrication.

The concept was first suggested by [12] and further [46] proposed that it should be regular, uniform, and in a bounded shape. But none of them formulated any scheme to be implemented.



(a) (b) (c)

Fig. 2 Regular Clocking Scheme (a) 2DDWave [20] (b) USE [18] (c) RES [19].

A formulation of a clocking scheme was framed by [20] in the name of Two-dimensional QCA clocking schemes. But does not support a proper feedback path; thus, the implementation of sequential circuits was a complication. The issue was taken care of by [18] with multi-layer wire crossing. Despite this, they argue that it can also work for coplanar crossing. However, both solutions are physically challenging to fabricate. An alternative of all the hurdles, as mentioned earlier, was proposed in [19] with an added benefit of the three-dimensional flow of information in any particular clock zone.

Along with a proper regular underlying clocking scheme, a universal QCA design is also essential to realize a complex circuitry. The QCA implementation relies on the majority gate and inverter. Therefore, a single unit capable of generating the basic functions like AND, OR & XOR is the need of the hour. It will enhance the performance of the circuit, makes it cost-effective, and exploitable. A few works can be seen in [32,33,44,47] with different aspects of aim and motivation. But none considered design of the composite gate, using underlying clocking and minimization of garbage outputs while realizing a complex circuit. Whereas AND-NAND methodology [32], UQCALG implementation [33] also analyzed the applicability and performance with the synthesis of symmetric function.

All these factors have influenced to propose a cost-effective composite gate with the capability of generating the essential logic functions like AND, OR, XOR gate. Moreover, the RES clocking scheme enhances efficiency, and scalability is in the center of attention.

4. Proposed Composite Gate

Digital systems are constructed from the basic building blocks, also termed as Logic Gates. These gates include AND, OR, NAND, NOR, NOT, XOR, and XNOR gates. The functionality of all the logic gates can be implemented, simulated, and verified using quantum-dot cellular automata technology [48]. Many attempts have been reported in QCA, but no suitable design found aims in proposing a circuit with primitive logic like NAND, AND, NOR, OR, XOR, X-NOR as output. Therefore, the logic gate design with a potentiality to produce universal logic functions like AND, OR & XOR is necessary. The logic operations can be framed in QCA with the majority gate's help and inverter only, as shown in Fig. 3.

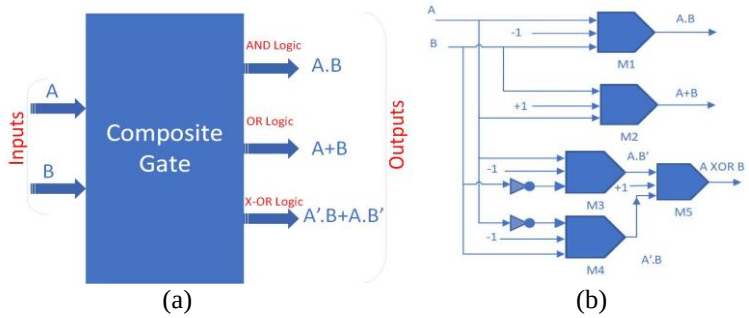


Fig. 3 Composite Gate (a) Block Diagram (b) Schematic diagram.

Such a design may lead to the synthesis of the complex logic function implementation where most of the logic functions are used simultaneously, with a minimum number of the circuit block. The proposed design is a platform that receives two inputs and generates the basic logic outputs like *AND (A.B)*, *OR (A+B)*, *XOR (AB'+A'B)*, for two inputs A & B. The functional logic equation of the proposed design can be expressed as Eq. 3 where A and B are the inputs to the composite gate.

$$f(A,B) = \{A.B, A+B, A.B'+A'.B\} \tag{3}$$

All the functional outputs can also be expressed using Majority Voter Gate and Inverter in QCA as follows.

AND = *Maj(A,B,0)*, equivalent to A.B
OR = *Maj(A,B,1)*, can also be expressed as A+B
XOR = *Maj(Maj(A,B',0), Maj(A',B,0),1)*, expressed as A $\oplus$ B

The remaining underlying logic like NAND gate expressed as *Maj(A',B',1)* or *Maj(A,B,0)'*, NOR gate can also be denoted by *Maj(A',B',0)* or *Maj(A,B,1)'* and X-NOR gate, which can also be expressed as *Maj(Maj(A',B',0),Maj(A,B,0),1) = (A⊕B)'*. In other words, they can be generated directly by applying an inverter in the generated outputs AND, OR, and XOR, respectively, without imposing any additional primitives. Additionally, the inversion of the inputs can be pulled off using XOR logic only setting either of the input to logic 1, like: XOR(A,B)= A for input B = 1 & it is B when A = 1.

The NAND and NOR gates are called the universal gate, as these logics have the capability to generate the basic logic gates like AND, OR, and NOT [48]. To the best of the authors' knowledge, it is the initial attempt to design a cost-efficient Composite Gate. Moreover, the proposed Composite Logic Gate is also introduced with a proper cell layout using the RES clocking scheme, discussed later in this section.

4.1. QCA Realization

As diagrammatically depicted in the schematic diagram (see Fig. 3(b)), it can be inferred that the derivation of the proposed CG requires five (5) majority gates and two (2) inverters. The cell layout of QCA realization for the CG is covered in Fig. 4(a) which testifies to the target of low area, high device density and enhanced computational speed. It is implemented in a coverage area of 0.13μm2, utilizing 88 QCA cells and latency of 0.75 (3 clock zones).

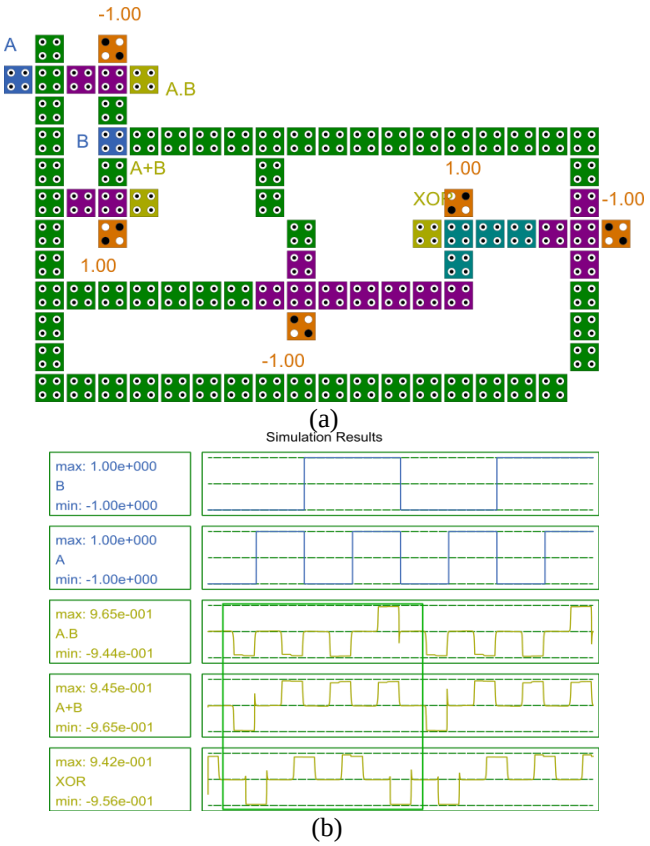


Fig. 4 (a) QCA layout of the proposed Composite Gate (b) Simulated result.

The result generated by the simulation of the proposed design is shown in Fig. 4(b). During the verification of the outcomes with the simulated value, no data loss has been observed. The 2-input composite gate is simulated and verified using the QCADesigner [49] simulator, with default parameters. The result of the circuit has been tested and validated with the truth table of the underlying logic gates.

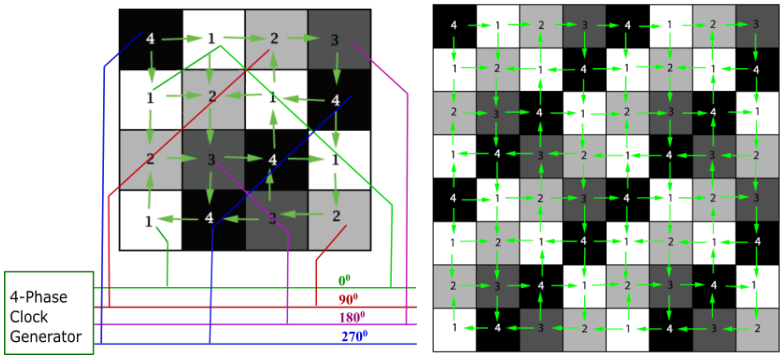
For an intersection in the flow of information, a coplanar wire crossing (preferably clock-based approach) has less fabrication overhead than multi-layer or rotated cell-based crossing. Though any kind of crossing is still a concern of research; it is an essential part of any large circuit. In this proposed design, clock-based coplanar wire crossing can efficiently be utilized if cascading is required. As mentioned earlier, without using an underlying clocking scheme, the design may not be a suitable candidate for fabrication. With this consideration, an extended design is proposed next.

4.2. Regular Clock based design

It is to be noted that a regular clocking scheme is essential to enable the specification of standard cells, routing algorithms and the development of placement and fabrication to

allow QCA technology to progress [18]. It is noticed from the different existing regular clocking schemes, as shown in Fig. 5 that the neighboring clock zones can be identified by continuous zone numbering. For example, clock zone 0 (Switch phase) is denoted by 1, followed by clock zone 1 or Hold phase and so on up to Clock zone 3 (Relax phase). Information proliferates through the clock zones sequentially. Starting from clock zone 0 to 1, then 1 to 2, 2 to 3 and 3 to 0 and continuously.

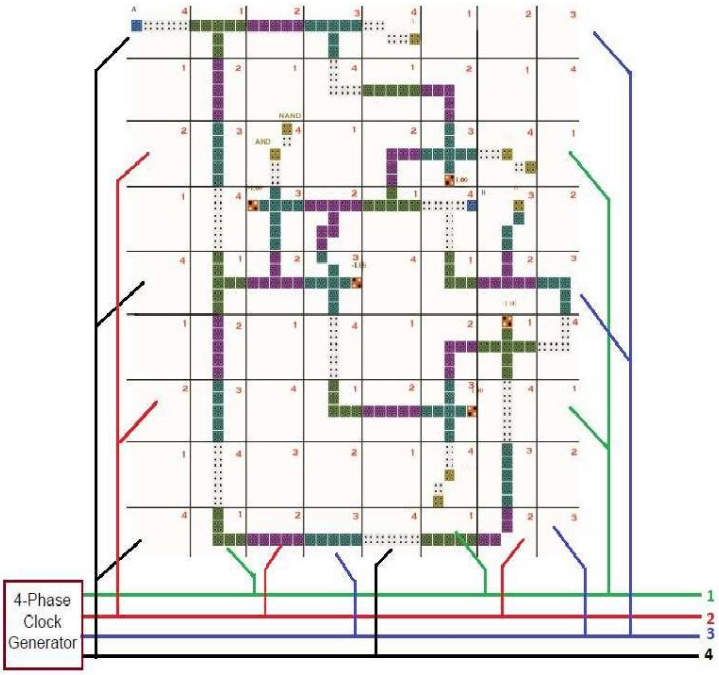
Furthermore, to facilitate the feedback path, there must be an opposite direction available in a clocking scheme in order. These constrictions have been implemented along with a three- dimensional flow of information in the RES clocking scheme [19]. As recommended in [20], to disperse the clock zone signals, the diagonally placed metal wires are inhumed under the QCA design where a 4-phase clock generator generates the signals. Fig. 5(a) shows the generation of electric field uniformly for each clock zone in the RES clocking scheme. Fabrication techniques can adequately consider the realization of these structural designs for the circuits.



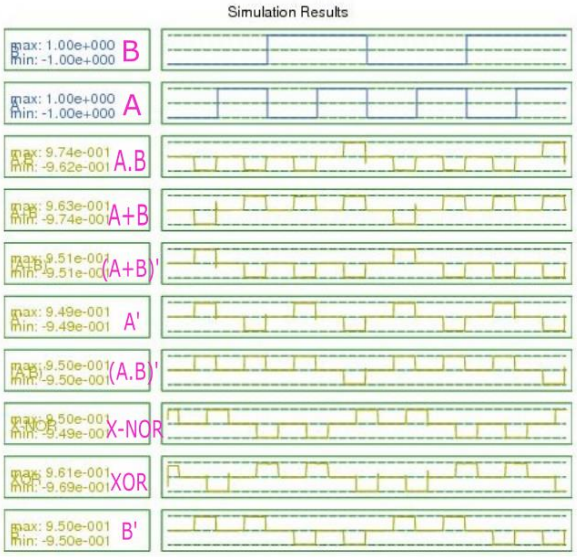
(a) (b)

Fig. 5 RES Clocking Scheme (a) Circuitry generates the electric fields for the clock (b) Extended version.

The clocking scheme block can be made replicated as and when required depending upon the area of the circuit. Accordingly, the extended version of RES is shown in Fig. 5(b). The green arrows show the directions; reverse directional flow is also available side by side for steering feedback purposes. But it creates an unnecessary white space only to have the opposite directions in a circuit. To overwhelmed delinquent, a cell at clock zone 1 is fixed just below the top left corner, creating three-way routing options. Thus, a three-way information flow is achieved in the RES underlying regular clocking scheme. It offers a supplementary benefit to realize an input majority voter gate with three inputs in a single clock zone. With the advent of this advantage, the extended design of the composite gate using RES underlying regular clocking scheme as in Fig. 6(a), and the corresponding simulated waveform is presented in Fig. 6(b). The extended circuit using RES clocking uses an area of 0.64μm2 and 261 cells, utilizing nine clock zones (latency = 2.25).



(a)



(b)

Fig. 6 (a) Proposed composite gate using RES underlying clocking scheme, (b) Simulated waveform.

Table 1 Composite Gate with Clocking VS without clocking

Composite Gate	Cell	Latency	Area(μm2)	Regular	Functions Generate
In Fig. 6	88	0.75	0.13	No	(AND, OR, XOR)
In Fig. 9	261	2.25	0.64	Yes	(AND, OR, XOR) with complement

The structural information of the proposed designs is tabulated in Table 1. Following Table 1, it is worth mentioning that the circuit developed using RES underlying regular clocking scheme have come up with a result in a larger area and number of cells in terms of implementation. It makes the circuit implemented in fabricate technology with a metal wire buried under the circuit and makes the circuit realistic possible.

5. Applicability and Performance Analysis

The compatibility of a circuit can be justified with the application of the same. This section discusses the best use of the proposed composite gate in QCA. At the same time, the performance of the proposed design is also analyzed.

5.1. Synthesis of Symmetric Function

If each variable in a Boolean function is either in un-complemented or in a complemented form in its sum of products (SOP) expression, it is called unate. A switching function expressed as $f(x_1, x_2,..., x_n)$ for all variables $x_1, x_2,..., x_n$ is termed as totally symmetric, if it remains invariant for the permutations of the variables [32]. The weight, say w of a vertex, say v (set of variables where each variable appears only once) is represented as the number of un-complemented variables in v.

Whereas in case the total symmetry which is a set of integers, say $A=(x_1, x_2,..., x_n)$ with $A\subset(0, 1, 2,..., n)$; all the vertices will appear in the function with weight w A. Likewise, an n-variable symmetric function is represented as $f_n(x_1, x_2,..., x_n)$. If set A consists of only consecutive integers $(x_i, x_{i+1},..., x_n)$, the symmetric function is consecutive. In the case of both unate and symmetric, it is called unate symmetric, which is always consecutive.

5.1.1. 2-Inputs Symmetric Function

There are 2^{n+1}–2 different symmetric functions possible for n variables, excluding constant functions 0 and 1. Thus, the number of symmetric functions consist of two input variables is $2^{2+1} – 2$. Therefore, a total of 2^3-2 = 6 functions, as shown in Table 2.

Table 2 Two-input Symmetric Functions

Sl No	Function
1	A.B
2	A'+B'
3	A+B
4	A'.B'
5	A.B'+A'.B
6	A.B+A'.B'

For 2-input variable symmetric functions, only single composite gates are sufficient to produce and get all the two variables symmetric functions. In this case, no garbage output is produced. It is worth mentioning here that a garbage output can be defined as the unused intermediate output generated in each step until the outcome.

To understand the same in terms of QCA and majority voter gate, let us analyze the functions below:

Function 1: Here, A.B is nothing but the AND logic of the input variables. It can easily be implemented using Majority Voter Gate.

Function 2: Here in *A'+B'*, an OR Logic is used in the complemented forms of the inputs. If we consider De-Morgan's Law of digital logic, the same can also be represented as (*A.B*)' which is a NAND logic of the inputs. The inversion of the output in function 1 will serve the purpose, without any extra logic to impose.

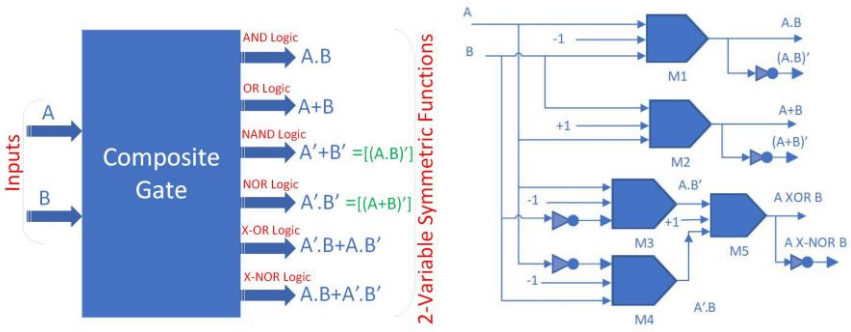
Function 3: Here *A+B* is an OR Logic of the input variables. In this case, also, a Majority Voter Gate is enough for the synthesis.

Function 4: In this case, *A'.B'* is represented as the AND of the complemented forms of the inputs. Like the second function, this function can also be represented as *(A+B)'* or the complement of the OR logic of the inputs. Similar to function 2, an inversion of the output in function 3 will generate this output.

Function 5: The equation *A.B'+A'.B* stands for mutually ANDed inputs with the complemented form of its counterpart in the minterms of the output. It is simply the Exclusive OR of the inputs. In this case, three majority gates are used as per the function structure.

Function 6: The expression *A.B+A'.B'* can further be presented as the complemented form of X-OR and also termed as X-NOR. Here, it is again the inversion of the result produces in function 5.

To sum up, we can say that the six (6) number of symmetric functions generated from 2- input variables produce the outputs as exactly like the proposed composite gate, as shown in Fig. 7(a). Therefore, this is the simplest form of design, ensuring the fastest operation in the realization of 2-input symmetric functions.



(a) (b)

Fig. 7 Composite Gate based realization of 2-variable symmetric functions (a) Block diagram (b) Schematic diagram.

5.1.2. Composite Gate based realization

This section explores the realization of 2-input symmetric functions to demonstrate the effective use of the composite gate. The proposed circuit is best suited for a specific

purpose, where most of the basic logic is required simultaneously. The most effective use of the composite gate structure introduced in this work can be the case where all the outputs are utilized. 2-input symmetric functions can be realized without any garbage or extra output (refer schematic diagram in Fig. 7(b)), which shortens the cost of circuit design, and the same can be realized in QCA approach as in Fig. 8(a). This circuit (similar to Fig. 4) is presented to show the implementation of a 2-input symmetric function using the proposed circuit as it is best suited for the purpose. The only difference lies in the fact that Fig. 8(a) includes the inverted forms of AND, OR & X-OR logic outputs, as generated in the design proposed in Fig. 4(a).

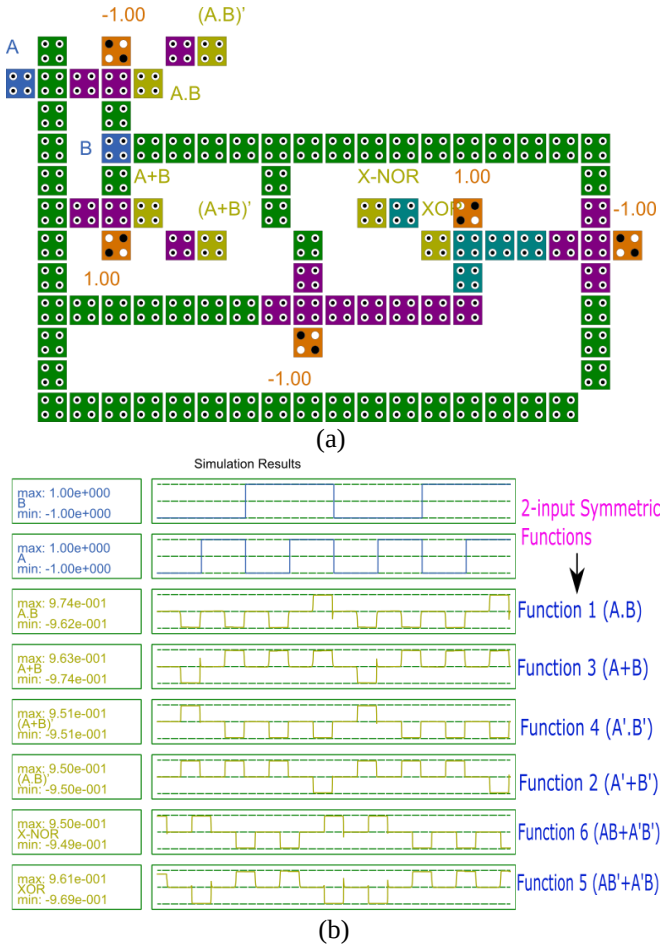


Fig. 8 (a) Composite Gate based realization of 2-variable symmetric functions, (b) Simulation result.

It shows that CG utilizes all the outputs of the composite gate and the inverted forms of each without any garbage outputs while realizing. No wire crossing can be observed in the composite gate-based implementation. However, as mentioned earlier, it may be the

need of the hour for a cascaded circuit. It can also be noted that the proposed composite gate-based realization of implementation of 2-input symmetric functions is most area-saving with only a single gate for all the functions so far, as compared to few existing designs. The simulation result of corresponding QCA based realization, as shown in Fig. 8(b), verifies the output. This figure is used to verify the simulated output with the logic of the 2-input symmetric function.

5.2. Performance Analysis

A Few works in the relevant field have been reported in [32,33,47]. Among them [33] and [47] have proposed a layout of 2-input symmetric functions realization. These designs generate garbage outputs, while other designs suffer from wire crossing. Still, no such single gate has been evolved so far as to accomodate all basic logic functions and at the same time use regular clocking scheme. The analysis and comparison for the effectiveness of composite gate-based realization with its counterpart in the literature review are shown in Table 3.

Therefore, the efficiency of composite gate-based realization is qualified when compared to the existing designs by considering the features like the number of wire crossings, gate count, garbage output and augmenting the underlying clocking scheme. As per the result, analysis, and comparison of the 2-Inputs Symmetric functions, it is found to be the best suitable to use the composite gate in realizing the same. The simulated output for the realization of 2-input symmetric functions, as shown in Fig. 8(b), affirms the synthesis.

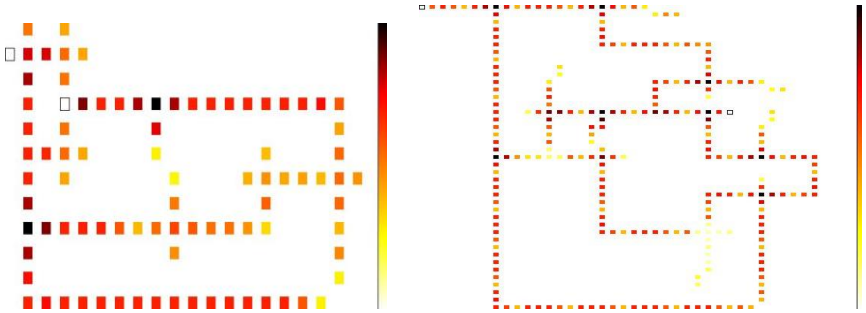
Table 3 Performance of composite gate in synthesis of 2-input symmetric functions

Gate	Wire Crossing	Gate Used	Regular Clocking	Garbage Output Produced
MV+INV	4	8	No	-
ULG [47]	2	7	No	-
UQCALG [33]	0	3	No	3
AND-NAND [32]	0	3	No	2
Proposed CG	0	1	Yes	0

6. Power Analysis

This section presents the power dissipated by the proposed designs considering both designs (with and without clocking). The widely accepted and used power estimation tool QCAPro has been used for the findings of the results [50]. QCAPro is a tool for the capability of trading with larger cells in number. It utilizes a technique based on fast approximation where non-adiabatic switching power loss is expected for a QCA circuit. The temperature value (QCAPro parameter) 2 Kelvin was considered in this research. The power dissipation of the design (Average of Leakage Energy Dissipation and Average of Switching Energy Dissipation) is evaluated at three levels of tunneling energy (0.5 Ek, 1 Ek, and 1.5 Ek). The energy consumption maps for the proposed design are presented in Fig. 9, with tunneling energy of 0.5 Ek.

A comparative analysis of the energy dissipation at these tunneling energy levels is recorded in Table 4 for the proposed Composite Gate. As the proposed design is first of its kind and no previous design in literature found, the comparison was not feasible.



(a) CG without clocking (b) CG using RES clocking

Fig. 9 Energy Consumption map under tunneling energy 0.5 Ek, at 2K temperature.

Table 4 The Power Dissipation for the proposed composite gate

Design/ **Energy Level**	Average of Leakage Energy Dissipation (meV)			Average of Switching Energy Dissipation (meV)			Total Energy Consumption (meV)		
	0.5Ek	**1Ek**	**1.5Ek**	**0.5Ek**	**1Ek**	**1.5Ek**	**0.5Ek**	**1Ek**	**1.5Ek**
Fig. 6	23.77	76.48	140.59	154.69	135.32	115.62	178.46	211.80	256.21
Fig. 9	78.52	244.14	439.96	429.15	369.58	312.17	507.67	613.72	752.13

The total power consumption of the proposed design in represented graphically in Fig. 10. It can be observed that the regular clock-based design requires more cells compared to the same design without clocking. It may result in higher density (in terms of area) for the design implemented in regular clocking. The graph representing the total power dissipation can also be noticed that the use of regular clocking in QCA design may lead to higher power dissipation. However, considering the practical design perspective and cost-efficiency of the design, it is always preferred to design a circuit embedding regular clocking and not only focus on basic metrics in arbitrary clocking.

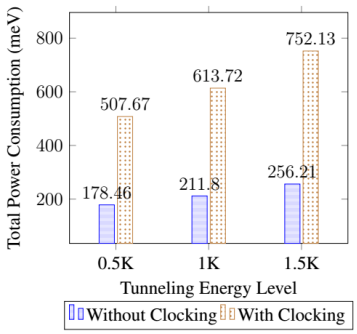


Fig. 10 Total dissipated energy of the proposed circuits design.

7. CONCLUSION

A coplanar design for a cost-efficient composite logic gate is proposed in this paper. The gate is capable of generating all the significant 2-input basic logic operations such as AND, NAND, NOT, OR, NOR, XOR and XNOR. The proposed composite gate is suggested and designed in both forms - with and without regular clocking scheme. This article is the first of its kind to propose a gate to generate all basic logic functions. The outcome in the experimental result supports the claim in compliance with the truth table. Apart from that, the proposed design is best suited for direct implementation of 2-input symmetric functions. A single block of composite gate is sufficient to realize all the functions. It achieves a gain of 33.33% in gate count and a complete waiver of garbage output is observed in comparison with its counterparts. In other words, the experimental study shows that the proposed design has better execution in a complete choice. The composite gate design has also been expanded, augmenting the underlying regular clocking scheme, RES which has serve to make the gate robust, efficient, and scalable. The functionality verification of the circuit has been carried out using the QCADesigner version 2.0.3 tool. Additionally, a comprehensive analysis of dissipated power is presented and QCAPro simulator is utilized in this regard.

We have proposed the design for a combinational circuit only. As a reference to the future study, we are prepared to apply the technique for a sequential circuit.

REFERENCES

[1] C. S. Lent, P. D. Tougaw, W. Porod, et al., "Quantum cellular automata", *Nanotechnology*, vol. 4, no. 1, p. 49, 1993.

[2] N. H. Weste and D. Harris, *CMOS VLSI design: a circuits and systems perspective*. Pearson Education India, 2015.

[3] J. Timler and C. S. Lent, "Power gain and dissipation in quantum-dot cellular automata", *J. Appl. Phys.*, vol. 91, no. 2, pp. 823–831, 2002.

[4] Y. Lu, M. Liu, and C. Lent, "Molecular quantum-dot cellular automata: From molecular structure to circuit dynamics", *J. Appl. Phys.*, vol. 102, no. 3, p. 034311, 2007.

[5] G. L. Snider, A. O. Orlov, I. Amlani, et al., "Quantum-dot cellular automata: Line and majority logic gate", *Jpn. J. Appl. Phys.*, vol. 38, no. 12S, p. 7227, 1999.

[6] S.-S. Ahmadpour, M. Mosleh and S. R. Heikalabad, "The design and implementation of a robust single-layer qca alu using a novel fault-tolerant three-input majority gate", *J. Supercomput.*, vol. 76, pp. 1–31, 2020.

[7] P. D. Tougaw and C. S. Lent, "Logical devices implemented using quantum cellular au- tomata", *J. Appl. Phys.*, vol. 75, no. 3, pp. 1818–1825, 1994.

[8] M. Goswami, M. Roychoudhury, J. Sarkar, et al., "An efficient inverter logic in quantum-dot cellular automata for emerging nanocircuits", *Arab. J. Sci. Eng.*, vol. 45, pp. 1–12, 2019.

[9] C.-K. Wang, I. Yakimenko, I. Zozoulenko, et al., "Dynamical response in an array of quantum-dot cells", *J. Appl. Phys.*, vol. 84, no. 5, pp. 2684–2689, 1998.

[10] Z. Chu, H. Tian, Z. Li, et al., "A high-performance design of generalized pipeline cellular array", *IEEE Comput, Archit. Lett.*, vol. 19, no. 1, pp. 47-50, 2020.

[11] A. Chaudhuri, M. Sultana, D. Sengupta, et al., "A reversible approach to two's complement addition using a novel reversible tcg gate and its 4 dot 2 electron qca architecture", *Microsyst. Technol.*, vol. 25, no. 5, pp. 1965–1975, 2019.

[12] K. Hennessy and C. S. Lent, "Clocking of molecular quantum-dot cellular automata", *J. Vac. Sci. Technol. B: Microelectron. Nanometer Struct. Process. Meas. Phenom*, vol. 19, no. 5, pp. 1752–1755, 2001.

[13] M. Goswami, M. R. Choudhury, and B. Sen, "A realistic configurable level triggered flip-flop in quantum-dot cellular automata", In Proceedings of the International Symposium on VLSI Design and Test, 2019, pp. 455–467.

[14] B. Sen, M. Dutta, D. Saran, et al., "An efficient multiplexer in quantum-dot cellular automata", In Proceedings of the Progress in VLSI Design and Test, 2012, pp. 350–351.
[15] Y. Adelnia and A. Rezai, "A novel adder circuit design in quantum-dot cellular automata technology", *Int. J. Theor. Phys.*, vol. 58, no. 1, pp. 184–200, 2019.
[16] H. R. Roshany and A. Rezai, "Novel efficient circuit design for multilayer qca rca", *Int. J. Theor. Phys.*, vol. 58, no. 6, pp. 1745–1757, 2019.
[17] W. Liu, L. Lu, M. O'Neill, et al., "A first step toward cost functions for quantum-dot cellular automata designs", *IEEE Trans. Nanotechnol.*, vol. 13, no. 3, pp. 476–487, 2014.
[18] C. A. T. Campos, A. L. Marciano, O. P. V. Neto, et al., "Use: A universal, scalable, and ef- ficient clocking scheme for qca", *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 35, no. 3, pp. 513–517, 2015.
[19] M. Goswami, A. Mondal, M. H. Mahalat, et al., "An efficient clocking scheme for quantum-dot cellular automata", *Int. J. Electron. Lett.*, vol. 8, no. 1, pp. 83–96, 2019.
[20] V. Vankamamidi, M. Ottavi, and F. Lombardi, "Two-dimensional schemes for clocking/timing of qca circuits", *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 27, no. 1, pp. 34–44, 2007.
[21] M. Abutaleb, "Robust and efficient quantum-dot cellular automata synchronous counters", *Microelectron. J.*, vol. 61, pp. 6–14, 2017.
[22] M. Raj, L. Gopalakrishnan, and S.-B. Ko, "Design and analysis of novel qca full adder-subtractor", *Int. J. Electron. Lett*, pp. 1–14, 2020.
[23] R. Singh, S. S. Das, and V. Sarada, "Design of a compact negative-edge triggered t flip-flop in qca technology", *J. Electr. Eng. Technol.*, vol. 11, no. 2, pp. 139–146, 2020.
[24] T. N. Sasamal, A. K. Singh, and A. Mohan, "Design of registers and memory in qca", In *Quantum-Dot Cellular Automata Based Digital Logic Circuits: A Design Perspective*, pp. 119– 137, 2020.
[25] A. Shiri, A. Rezai, and H. Mahmoodian, "Design of efficient coplanar comparator circuit in qca technology", *FU Elec. Energ.*, vol. 32, no. 1, pp. 119–128, 2019.
[26] M. N. Divshali, A. Rezai, and S. S. F. Hamidpour, "Design of novel coplanar counter circuit in quantum dot cellular automata technology", *Int. J. Theor. Phys.*, vol. 58, no. 8, pp. 2677–2691, 2019.
[27] Z. Taheri, A. Rezai, and H. Rashidi, "Novel single layer fault tolerance rca construction for qca technology", *FU Elec. Energ*, vol. 32, no. 4, pp. 601–613, 2019.
[28] Y. XianYang and B. Guo, "Further enumerating boolean functions of cryptographic significance", *J. Cryptol.*, vol. 8, no. 3, pp. 115–122, 1995.
[29] D. L. Dietmeyer, "Generating minimal covers of symmetric functions", *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst*, vol. 12, no. 5, pp. 710–713, 1993.
[30] S. Chakrabarti, S. Das, D. K. Das, et al., "Synthesis of symmetric functions for path-delay fault testability", *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst*., vol. 19, no. 9, pp. 1076–1081, 2000.
[31] M. Perkowski, P. Kerntopf, A. Buller, et al., "Regular realization of symmetric functions using reversible logic", In Proceedings of the Euromicro Symposium on Digital Systems Design, Warsaw, Poland, 2001, pp. 245-252.
[32] P. K. Bhattacharjee, "Use of symmetric functions designed by qca gates for next generation ic", *Int. J. Comput. Theory Eng.*, vol. 2, no. 2, p. 211, 2010.
[33] B. Sen, M. Dalui, and B. K. Sikdar, "Introducing universal qca logic gate for synthesizing symmetric functions with minimum wire-crossings", In Proceedings of the International Conference and Workshop on Emerging Trends in Technology, 2010, pp. 828–833.
[34] C. S. Lent and P. D. Tougaw, "A device architecture for computing with quantum dots", *In Proceedings of the IEEE*, vol. 85, no. 4, pp. 541–557, 1997.
[35] P. D. Tougaw and C. S. Lent, "Dynamic behavior of quantum cellular automata", *J. Appl. Phys.*, vol. 80, no. 8, pp. 4722–4736, 1996.
[36] K. Kim, K. Wu and R. Karri, "Quantum-dot cellular automata design guideline", *IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences*, vol. 89, no. 6, pp. 1607–1614, 2006.
[37] R. Devadoss, K. Paul and M. Balakrishnan, "Clocking-based coplanar wire crossing scheme for qca", In Proceedings of 23rd International Conference on VLSI Design, Bangalore, India, 2010, pp. 339-344.
[38] B. Sen, A. Nag, A. De, et al., "Towards the hierarchical design of multilayer qca logic circuit", *J. Comput. Sci.*, vol. 11, pp. 233–244, 2015.
[39] M. N. Divshali, A. Rezai and A. Karimi, "Towards multilayer QCA SISO shift register based on efficient d-ff circuits", *Int. J. Theor. Phys.*, vol. 57, no. 11, pp. 3326–3339, 2018.
[40] B. Sen, R. Mukherjee, K. Mohit, et al., "Design of reliable universal qca logic in the presence of cell deposition defect", *Int. J. Electron.*, vol. 104, no. 8, pp. 1285–1297, 2017.

[41] B. Sen, M. R. Chowdhury, R. Mukherjee, et al., "Reliability-aware design for programmable qca logic with scalable clocking circuit", *J. Comput. Electron.*, vol. 16, no. 2, pp. 473– 485, 2017.

[42] A. N. Bahar, R. Laajimi, M. Abdullah-Al-Shafi, et al., "Toward efficient design of flip-flops in quantum-dot cellular automata with power dissipation analysis", *Int. J. Theor. Phys.*, vol. 57, no. 11, pp. 3419–3428, 2018.

[43] J. Pal, S. Bhattacharjee, A. K. Saha, et al., "Study on temperature stability and fault tolerance of adder in quantum-dot cellular automata", In Proceedings of the 5th International Conference on Signal Processing, Computing and Control (ISPCC), Solan, India, 2019, pp. 69-74.

[44] M. Dalui, B. Sen, and B. K. Sikdar, "Fault tolerant qca logic design with coupled majority-minority gate", *Int. J. Comput. Appl.*, vol. 1, no. 29, pp. 81–87, 2010.

[45] B. Sen, M. Dutta, D. K. Singh, et al., "Qca multiplexer based design of reversible alu", in IEEE International Conference on Circuits and Systems (ICCAS), Kuala Lumpur, Malaysia, 2012, pp. 168-173.

[46] M. Janez, P. Pecar, and M. Mraz, "Layout design of manufacturable quantum-dot cellular automata", *Microelectron. J.*, vol. 43, no. 7, pp. 501–513, 2012.

[47] Y. Xia and K. Qiu, "Design and application of universal logic gate based on quantum-dot cellular automata", In Proceedings of the 11th IEEE International Conference on Communication Technology, Hangzhou, China, 2008, pp. 335-338.

[48] J. Pal, P. Dutta, and A. K. Saha, "Realization of basic gates using universal gates using quantum-dot cellular automata", In Proceedings of the International Conference on Computing and Communication Systems, 2018, pp. 541–549.

[49] K. Walus, T. J. Dysart, G. A. Jullien, et al., "Qcadesigner: a rapid design and simulation tool for quantum-dot cellular automata", *IEEE Trans. Nanotechnol.*, vol. 3, no. 1, pp. 26–31, 2004.

[50] S. Srivastava, A. Asthana, S. Bhanja, et al., "Qcapro-an error-power estimation tool for qca circuit design", in IEEE international symposium of circuits and systems (ISCAS), Rio de Janeiro, Brazil, 2011, pp. 2377-2380.