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Original scientific paper

FORCED STACK SLEEP TRANSISTOR (FORTRAN): A NEW LEAKAGE CURRENT REDUCTION APPROACH IN CMOS BASED CIRCUIT DESIGNING

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Abstract. *Reduction in leakage current has become a significant concern in nanotechnology-based low-power, low-voltage, and high-performance VLSI applications. This research article discusses a new low-power circuit design the approach of FORTRAN (FORced stack sleep TRANsistor), which decreases the leakage power efficiency in the CMOS-based circuit outline in VLSI domain. FORTRAN approach reduces leakage current in both active as well as standby modes of operation. Furthermore, it is not time intensive when the circuit goes from active mode to standby mode and vice-versa. To validate the proposed design approach, experiments are conducted in the Tanner EDA tool of mentor graphics bundle on projected circuit designs for the full adder, a chain of 4-inverters, and 4-bit multiplier designs utilizing 180nm, 130nm, and 90nm TSMC technology node. The outcomes obtained show the result of a 95-98% vital reduction in leakage power as well as a 15-20% reduction in dynamic power with a minor increase in delay. The result outcomes are compared for accuracy with the notable design approaches that are accessible for both active and standby modes of operation.*

Key words: *FORTRAN approach, Submicron region, Standby and Active modes of operation, Power optimization, Sub-threshold leakage current*

1. INTRODUCTION

Power utilization is one of the main issues to be taken care of in VLSI circuit designing, for which CMOS is the most important technology. Today's emphasis on low-power is not only due to traditional smartphone devices, but also due to other issues like an increase in leakage current, high power dissipation and fabrication cost. As even

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before the mobile era, power consumption was a significant problem. To minimize power dissipation, many researchers have proposed different ideas from the device level to the architectural level [1]. There are numerous methods discussed to reduce leakage power in CMOS based circuit designing [2–10]. Each approach delivers a novel way to reduce leakage power, but the shortcomings of each approach limit the claim of each approach to be the best. As the feature sizes of the device go on decreases, threshold voltage also declines, which increases the static power dissipation [11].

Therefore, while in standby mode, the transistor cannot be turned off completely. High power consumption leads to a reduction in battery life if the device is battery powered. It affects the reliability, packing, cooling costs and performance of the device. The primary sources of power dissipation in VLSI circuits are

(1) Dynamic power consumption, which occurs due to charging and discharging of the load capacitance, which is about 90-92% of the technology processes with feature size larger than 1 µm.

(2) Short circuit power consumption, due to the direct path established between the power supply and ground because of the transition in the logic gates.

(3) Leakage current, which arises mainly due to reverse bias diode currents or sub-threshold leakage current. The short circuit power dissipation can be reduced by 10% by designing the circuit having equal rise time and fall time. For minimizing power consumption in deep-submicron region, supply voltage is scaled down due to which dimensions of device changes and delay is increased. To maintain the performance of the CMOS circuit as it is, threshold voltage (V_{th}) of the transistor should be minimized [12]. The scaling down of V_{th} results in an exponential increase in the threshold leakage current. The entire average power dissipation in CMOS circuits can be expressed by the equation. Where α is the node conversion activity factor (the average number of times the node makes a power-consuming changeover in one clock period), C_L is the load capacitance, V_{dd} is the supply voltage, and f_{clk} is the clock regularity.

$$P_{avg} = P_{dynamic} + P_{short\ circuit} + P_{leakage} \tag{1}$$

$P_{dynamic}$ (Switching) is the exchanging component of power dissipation specified by equation 2.

$$P_{dynamic} = \alpha .C_L.V_{dd}^2.f_{clk} \tag{2}$$

In this manuscript, a new low-power reduction approach is proposed, which provides an innovative choice for low-power VLSI designers/engineers to reduce leakage current in a much better way besides increasing in area and delay to a small extent. An unbiased comparison of the proposed approach with previously available low-power approaches is made in estimating the accuracy of the proposed approach. TANNER design tools that are used for this process: S-edit, T-SPICE, and W-Wave is used for schematic capture, SPICE simulation engine, waveform viewer, respectively in this proposed work.

The major pillar of this research works around FORTRON based digital circuits can be pointed as follows:

- We demonstrate the novel FORTRAN (FORced stack sleep TRANsistor), which decreases the leakage power efficiency in the CMOS-based circuit outline in VLSI domain.
- We presented the novel and efficient circuit-level leakage power reduction approach of FORTRAN, which can minimize leakage power as well as dynamic power in a decent amount.

- We implement the FORTRON CMOS based NAND-2 and NOR-2 layout in L-edit 16.0 version.
- We demonstrate the NAND-2 and NOR-2 layout and area results.
- The pre-layout (synthesized or gate-level) and post-layout results of CMOS-NAND-2 and CMOS NOR-2 have passed all verifications of the ASIC design flow.
- We estimate the area of CMOS, NAND-2 and NOR-2 after the DRC result pass.
- We perform the performance comparison of CMOS NAND-2 and NOR-2 with the state-of-the art work.

This paper is organized as below: Section I gives the Introduction of different approaches to minimize the power loss. Section II discusses the previously reported approaches available to deal with leakage current reduction. Section III explains the proposed new approach to the FORTRAN approach. Section IV gives a logic gate implementation using the FORTRAN approach with a table used to select control input signals G1 and G2 in an Active mode of operation. In section V, comparative delay analysis is discussed. Simulation results and discussion is specified in section VI. Finally, the conclusion is given in section VII.

2. PREVIOUS APPROACHES

Numerous methods for minimizing leakage power are reported in the literature [13-20] which are mostly based on modes of operation. They are classified into two categories: (1) Standby/Idle mode (2) Active mode

(1) Standby/idle mode: When the circuit is in the idle state, the circuit is cut off from the power rails and leakage power occurs

(2) Active mode: Leakage is minimized during the run time by stacking the transistor, thereby reducing the overall leakage power

In this section, discussion about previous low-power leakage reduction approaches is done that primarily focused on reducing leakage power consumption of CMOS circuits. MTCMOS, LECTOR, Sleepy Stack, INDEP are some of these types of approaches whose primary goal is to reduce the leakage power at gate-level design. A well-known model of Stacking transistor model in which transistors are connected in series with each other is suggested in [20]. By applying some off-state transistors in series, the leakage power of a logic circuit can be minimized. By attaching more transistors in a stack can save more leakage current. The control of threshold voltage in the stacking approach depends on the gate to source voltage, drain to source voltage and substrate to source voltage of the stacked transistors.

The use of Multiple Threshold voltage CMOS (MTCMOS) technology for leakage control is described as shown in Fig. 1 (a) [21]. A high threshold, sleep transistors are attached between the V_{dd} and Gnd power rails. In Standby mode, high threshold, sleep transistors is turned off to reduce the leakage current dramatically by disconnecting the actual power supply V_{dd} and Gnd from the logic block. A controller is required to control the sleep mode and Active mode of a transistor. Extra processing steps are required to manage the high threshold, sleep transistor controller. Moreover, there is also a performance penalty because of the appearance of the high-threshold voltage transistor in series with all the switching current paths. The dual-V_{th} approach, which uses transistors with two different threshold voltages, is a variation of the MTCMOS approach. Here, additional mask layers for each value of threshold voltage are required for fabricating the transistors selectively according to their assigned threshold values in both MTCMOS and Dual-V_{th} approaches.

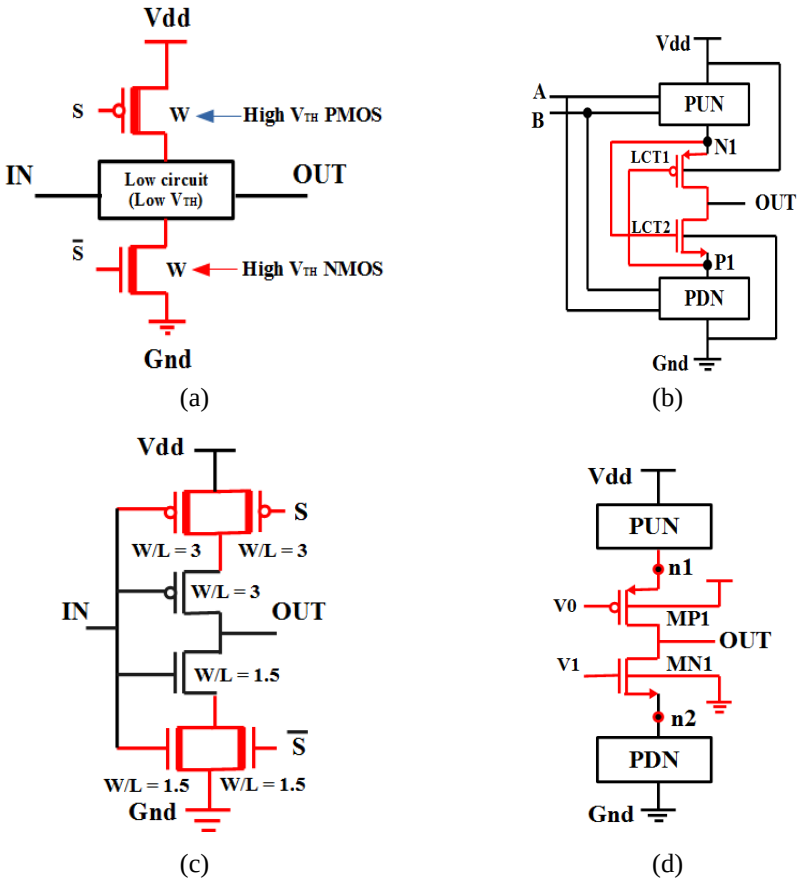


Fig. 1 Leakage power approaches (a) MTCMOS [21] (b) LECTOR [22] (c) Sleepy Stack [23] (d) INDEP [24]

The LEakage Control transisTOR (LECTOR) approach is proposed, as shown in Fig. 1 (b) is a single threshold, input dependent method to reduce leakage current [22]. It requires only two transistors to minimize leakage current, in which two leakage control transistors (LCTs) are used on the same threshold voltage type as a one PMOS transistor between PUN and output and one NMOS transistor between output and PDN. The gate terminal of each leakage control transistor (LCT) is controlled and operated by the source of the other transistor. In this approach, one of its LCTs is always near its cutoff for any combination of input signal. The drawback of the LECTOR approach is that no full output swing is achieved on the output side of the input via logical circuitry, and the propagation delay is also more of this design.

The Sleepy Stack approach is proposed, as shown in Fig. 1 (c) combines the sleep and stack approach [23]. It replaces three transistors in place of one transistor in the CMOS circuit. It divides the existing transistor into three transistors out of which one high V_{th} transistors are in parallel to one of the two transistors, which is itself divided into two half-size transistors like the stack approach. During sleep mode, sleep transistors are

turned off, and stacked transistors suppress leakage current while saving state as well. Here each parallel placed sleep transistor also reduces propagation delay by reducing the resistive path of the circuit during Active mode. However, the penalty in terms of area is the most significant matter in this approach, because three transistors replace every single transistor of CMOS, and additional wiring is also required for each sleep signal operation. Therefore, it requires three times more area compared to the CMOS approach if the same transistors are used in circuit designing.

Another latest approach to decrease leakage power dissipation is INDEP (INput DEPendent) approach, as illustrated in Fig. 1 (d), which is based on the Boolean logic circuit [24]. The gate terminals with additional built-in transistors rely on the main logic circuit input combinations. Therefore, the selections of input gate voltages are very crucial for dropping the leakage current efficiently. The slight increase in the area of the circuit is the negative criterion of this circuit design approach.

In the literature, several works on CMOS circuit designs were directly proposed through MTCMOS, LECTOR, SLEEP STACK, and INDEP. They contained no quantitative architectural comparison with FROTRAN technology. This works were proposed reduction of leakage current, dynamic power and delay within an iteration for the logical inputs using FORTRAN technology. Following the existing works in [21-24], however, we believe that the improvement over the conventional design can verify our proposed FORTRAN based digital CMOS circuit design strategy. We have adopted the FORTRAN technology in the proposed and conventional MTCMOS, LECTOR, SLEEP STACK, INDEP for a fair comparison. The proposed designs such as full adder, a chain of 4 inverters and 4-bit multiplier has analyzed with 180nm, 130nm, 90nm technology node to analyze static power, dynamic power and delay. In this manuscript, CMOS, Sleepy Stack and INDEP approaches are taken for comparison with the proposed circuit design approach of FORTRAN. Sleepy Stack approach saves leakage power in a reasonable amount by considering the state saving of the logic gate using both low threshold and high threshold voltage transistors. INDEP is a new advanced approach that saves leakage power effectively by using only low threshold voltage transistors in its structure. Therefore, the FORTRAN approach is compared with both the advanced approaches (Sleepy Stack and INDEP) as well as the most successful approach available (CMOS) to date for minimizing leakage current.

3. FORTRAN APPROACH

The FORTRAN (FORced stack sleep TRANsistor) approach has a joint structure of forced stack and sleep transistor approach, as presented in Fig. 1. The forced stack transistor structure is generally made by breaking the existing CMOS single transistor structure into two transistors and then forces to take advantage of the stacking effect in which the resistance of the path (from Vdd to Gnd) increases rapidly that decreases the leakage power. The two extra added transistors (P3 and N3) are connected to the forced stack structure in such a way that their drain connection is attached to the substrate of both the forced stack transistors (P1-P2 for PUN, N1-N2 for PDN) as shown in the drawing.

In Standby mode of operation, when these extra added transistors (P3 and N3) are ON, it will automatically increase the threshold voltage of the stack transistors, and then the stack transistors would behave like a high threshold voltage transistors which does not allow much leakage current to pass through them. Therefore, the leakage current will

decrease in a reasonable amount in the Standby mode of operation. These two extra sleep transistors input gates are connected opposite to that of forced stack transistors in PUN and PDN. At this point, when one transistor goes from Active mode to Standby mode, it does not take much time to tackle. The beauty of the proposed approach is that only the lower threshold voltage transistors are being used in the design approach. Therefore, the fabrication problem of implementing high threshold voltage transistors practically, which is somehow challenging and complicated to implement in a real manner, is elucidated. It is difficult and time consuming to fabricate both types (low/high threshold voltage) of transistors on the same IC at the fabrication level.

In the FORTRAN approach, the width of all PMOS transistors is double compared to the width of NMOS transistors. Therefore, in the 180nm Technology node, if one takes an NMOS transistor W/L ratio as 250nm/180nm, subsequently W/L ratio of PMOS transistor should be taken as 500nm/180nm. This is done to maintain the mobility ratio of μn/μp as 2 because in general, the mobility of electron (μn) is 2 times greater than the mobility of holes (μp). The mobility ratio is required to maintain the same amount of charge carriers flow in NMOS (electrons) and PMOS (holes) region at a time.

3.1 Functioning of FORTRAN structure

Fig. 2 shows the structure of the FORTRAN general approach. Two modes of operation are explained here: Active mode and Standby mode.

In active mode of operation, when input signal pulses are applied at the input terminal of the circuit, G1 and G2 should be turned ON. So, the forced stack transistor structure (P1-P2 and N1-N2) will be in ON condition, and parallel transistors (P3, N3) will be OFF due to applying logic 0 at G1 and logic 1 at G2 making transistor P3 and N3 OFF. Due to this arrangement, resistance from Vdd to node X1 will be decreased, making forced stack structure (P1-P2 and N1-N2) to be ON in Active mode. Therefore, the full supply voltage is achieved at node X1. Same as for node X2, the full virtual, Gnd, is achieved when the G2 is ON. The Virtual power supply lines VDDV and GNDV will be established at node X1 and X2. In Active mode of operation, NMOS transistors N1 and N2 will be in Active mode, while N3 will be in a cutoff mode as well as PMOS transistors P1 and P2 will be in Active mode, and P3 will be in a cutoff mode of operation. In sleep/Standby mode, the reverse will happen.

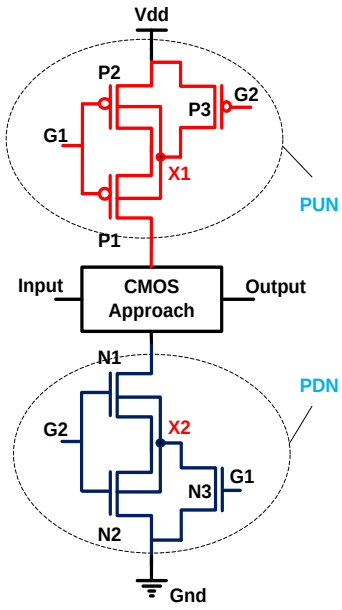


Fig. 2 FORTRAN General Approach

In a standby mode of operation, the advantage of the stacking effect should be taken as sub-threshold leakage current, which flows through a stack of series-connected transistors and reduces the leakage current when more than one transistor in the stack is turned off. This effect is known as the 'stacking effect.' One can explain it by connecting two transistors in series with each other, as shown in Fig. 3. When both transistor P1 and

P2 are turned off, the voltage at in-between node X will be positive due to minor drain current present there.

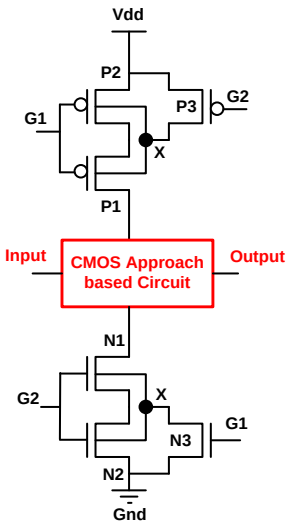


Fig. 3 Working of FORTRAN approach

In the Standby mode of operation, extra transistors of PMOS and NMOS are connected in parallel with the forced stacking structure. The input gate terminals are connected opposite to that of the forced stack structure of PUN and PDN network, which plays a crucial role in the Standby mode of operation. It converts low threshold voltage transistors to high threshold voltage transistors. Table 1 shows the measurement values of different parameters taken in the simulation tool. All the measurement values as listed in Table 1 are important for analyzing the performance of the FORTRAN based digital circuit designs.

Table 1 Set of Simulation Parameters for different technology nodes

Parameters (unit)	180nm Technology node	130nm Technology node	90nm Technology node
Supply Voltage (V)	1.8	1.3	1.1
Frequency (MHz)	25	25	25
NMOS (Width) (µm)	0.25	0.2	0.15
NMOS (Length) (µm)	0.18	0.13	0.1
PMOS (Width) (µm)	0.5	0.4	0.3
PMOS (Length) (µm)	0.18	0.13	0.1
NMOS (V_{th}) (mV)	0.399	0.332	0.26
PMOS (V_{th}) (mV)	-0.42	-0.349	-0.303
Temperature (^{0}C)	25	25	25

Table 2 Comparative analysis of Inverter for Dynamic power, Delay and Static power

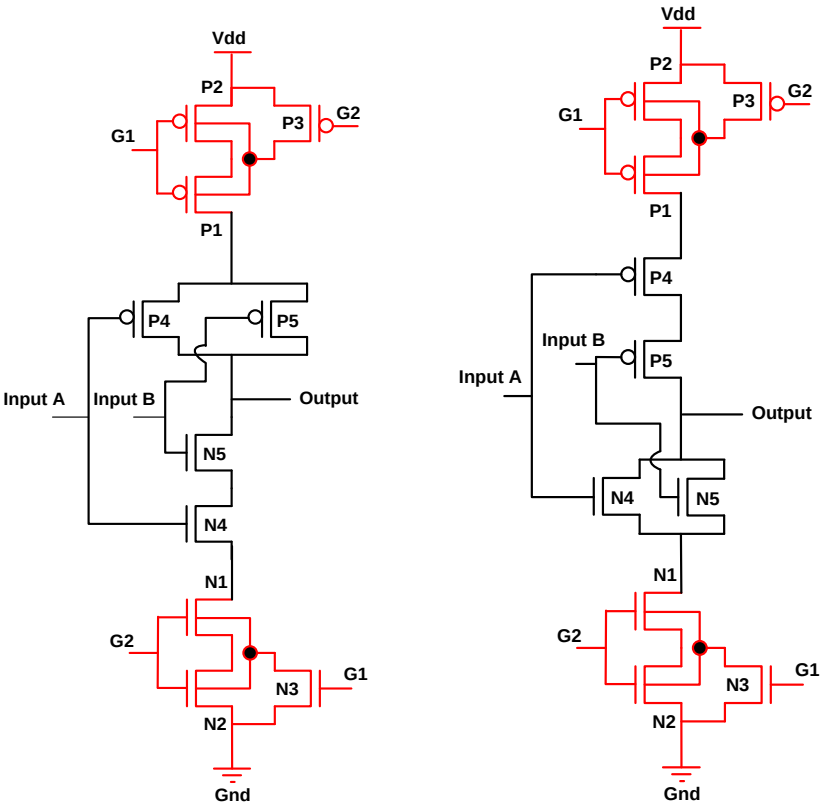
INVERTER	180nm technology node				
	Dynamic (μW)	Delay (ns)	Static power (pw)		Average Static Power (pW)
			0	1	
CMOS	1.85	10.5	382	676	529
Sleepy Stack	1.42	72.6	374	384	379
INDEP	1.56	79.8	11.9	115	63.45
FORTRAN	1.14	97.6	11.36	18.38	14.87
130nm Technology					
CMOS	0.382	6.11	208	399	303.5
Sleepy Stack	0.293	10.6	398	395	396.5
INDEP	0.296	13.1	44.4	41.4	42.9
FORTRAN	0.234	47.67	13.59	3.04	8.315
90nm Technology					
CMOS	0.22	5.77	220	318	269
Sleepy Stack	0.146	8.82	317	315	316
INDEP	0.138	5.76	41.5	19	30.25
FORTRAN	0.104	7.8	2.77	6.13	4.45

The simulation result for an inverter is presented above by comparing the FORTRAN inverter structure with previously available approaches. Here, for comparison, Sleepy Stack approach is considered as it is one of the successful approaches with state saving for effectively decreasing leakage current using forced stack transistor in its design and another approach is INDEP (INput DEPendent) approach because it's the most advance approach to reduce leakage current, as known to the author. The analysis below is done at 180nm, 130nm and 90nm Technology node for a fair comparison between different approaches.

As shown in Table 2, Dynamic Power saving in FORTRAN approach is almost 32% compared to CMOS Approach. However, it is 45% at the 90nm technology node. Therefore, as an observation, leakage power dissipation is decreased in a higher amount in the proposed approach compared to other approaches. Leakage power is almost decreased to 95-98 % compared to CMOS approach, which is very important while taking care into consideration that only low threshold voltage transistors are utilized in the proposed design. This approach will give the VLSI circuit designer a new area of research for minimizing leakage power by effectively utilizing low threshold voltage transistors into the structure. High threshold transistors are best to minimize leakage current, but the problem with high threshold voltage transistors is in its fabrication process, that it has not reached in an effective way to mainstream fabrication process up till now with a proficiency like low threshold voltage transistors. One concern with the proposed approach is a minimal increase in the total circuit area. But, it is not a big concern nowadays, which is to be considered as a primary problem, because high transistor integration density is possible in which millions of transistors can be placed on a single chip effortlessly by applying various advanced fabrication approaches. If we are reducing technology node, then the improvement factor is being seen in dynamic power as per during the simulation study in T-SPICE.

4. FORTRAN LOGIC GATE IMPLEMENTATION

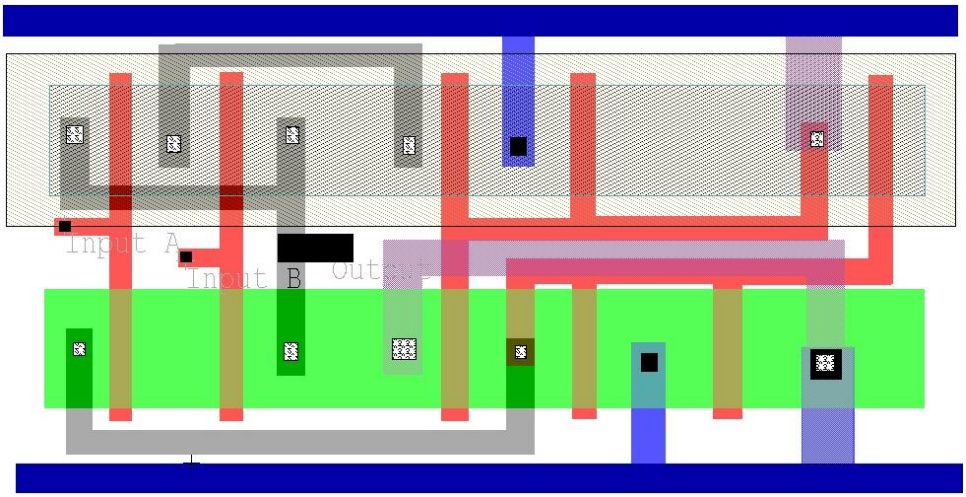
The logic gates as NAND-2 and NOR-2 with FORTRAN approach is described for two inputs and a single output, as displayed in Fig. 4. As shown in Fig 4, node A and B are two inputs, and node Y is the output of the FORTRAN NAND-2 gate, whereas G1 and G2 are the two control inputs that connect the V_{dd} and Gnd with the circuit. The working of FORTRAN approach is considered as, in Active mode of operation, when A and B are same, at that phase, G1 and G2 value will be same as that of A or B, making transistors P4, P5, N4 and N5 to acquire complete logic at the output terminal by connecting either V_{dd} or Gnd to the output. Here the forced stack transistor effect makes the resistor of the path very less in Active mode, and thus, less active power dissipation is obtained compared to the CMOS approach. In Standby mode, as soon as sleep transistors N3 and P3 go in ON condition, it will automatically increase the threshold voltage of forced stack transistor structure which behaves like high threshold voltage transistors and decrease the leakage current by increasing the resistance of the path from V_{dd} to output in PUN and from Gnd to output in PDN.



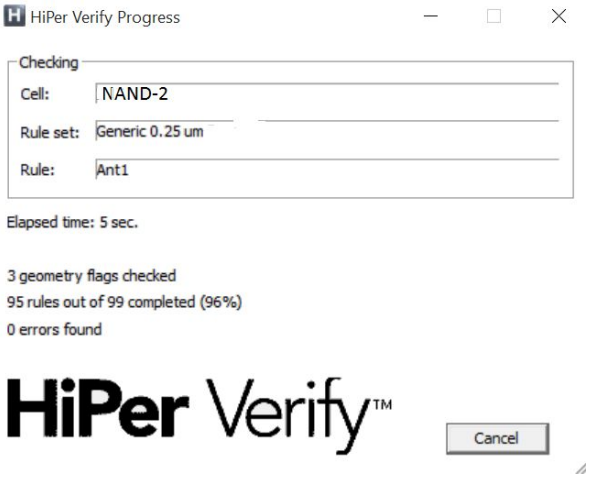
(a) (b)

Fig. 4 FORTRAN (a) NAND-2 and (b) NOR-2 gate

Fig 5a presents the physical layout of FORTRON based NAND-2 using the process libraries of Generic250nm. The physical verification was carried out in L-Edit v16. 0 version of Mentor Graphics tool. The mentioned NAND-2 gate with 10 transistor in which 5 transistor as PMOS and 5 transistor as NMOS have the small area. This is clear in the physical layout of NAND-2 highly symmetric configuration and equal transistor of both NMOs and PMOS of these mentioned designs. The area of NAND-2 is taken into the measure as 67.37 μm^2. The DRC results of the physical layout of FORTRON based NAND-2 are shown in Fig. 5b. The physical layout was carried out in L-Edit considering the net-list found after the physical verification flow as shown in Fig. 6.



(a)



(b)

Fig. 5 Design of FORTRON based NAND-2 (a) Layout (b) DRC results

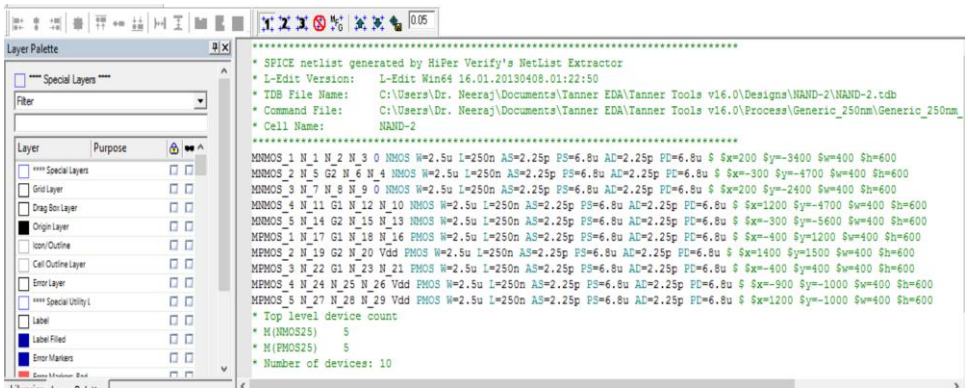


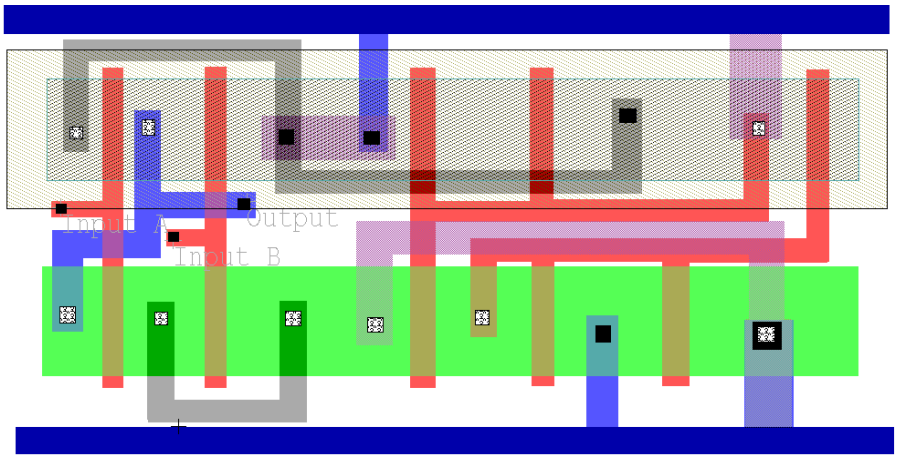
Fig. 6 Netlist extract on the physical layout of NAND-2 cell.

The logic unit of FORTRON based NOR-2 includes 2-input A and B with two control input G_1 and G_2 as shown in Fig 7a. In the synthesis of NOR-2 design operation in the state of 5 NMOS and 5 PMOS are used in the design. Its physical layout of NOR-2 has an area of 68.25 μm^2. The process libraries were taken as Generic250nm for the physical layout of NOR-2. The design of the NOR-2 circuit is connected to power supply and ground and therewith transistors, the design has more swing in the output voltage and driving capability. Design rule check (DRC) is the layout rules of technology and be used for physical (post-layout) verification for ASIC design flow. In the physical layout of NOR-2 results have passed all verifications of the ASIC design flow as shown in Fig 7b. The extracted net-list from the physical layout of NOR-2 is presented in Fig. 8.

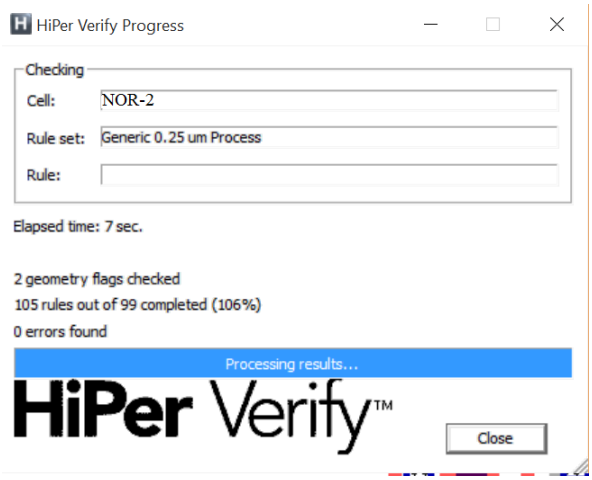
Table 3 gives the complete details of the FORTRAN approach for different input levels in the NAND-2 gate. All the input values are given in the circuit to remain in Active mode of operation. Here different transistors' behavior is shown at different input levels for a fair comparison. From table 3, it can be perceived that the value of the control signal G1 and G2 is same when inputs are identical in NAND gate, but if both the input values are different, then both G1 and G2 values should be taken as logic 0 in NAND gate.

In table 4, the analysis of the NOR-2 gate of different inputs is given. From observation of the table, it can be detected that when input values are same, then both G1 and G2 control transistor value should be same similar to input values, but if both inputs are different, then G1 and G2 would be at logic 1 to keep the circuit in Active mode of operation.

From the above analysis, transistors value at different values of inputs shows which transistors should be ON and OFF at the given input. From this analysis, different modes of transistors can be perceived at various levels of inputs. For Standby mode of operation, a different value for control transistors G1 and G2 should be occupied for Active mode of operation.



(a)



(b)

Fig. 7 Design of NOR-2 (a) Layout (b) DRC results

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********************************************************************************
* SPICE netlist generated by HiPer Verify's NetList Extractor
* L-Edit Version:     L-Edit Win64 16.01.20130408.01:22:50
* TDB File Name:      C:\Users\Dr. Neeraj\Documents\Tanner EDA\Tanner Tools v16.0\Designs\XOR\NOR-2.tdb
* Command File:      C:\Users\Dr. Neeraj\Documents\Tanner EDA\Tanner Tools v16.0\Process\Generic_250nm\Generic_250nm_
* Cell Name:         NOR-2
********************************************************************************
MNMOS_2 N_3 G2 N_2 N_1 NMOS W=2.5u L=250n AS=2.25p PS=6.8u AD=2.25p PD=6.8u $ $x=-300 $y=-4700 $w=400 $h=600
MNMOS_4 N_5 G1 N_6 N_4 NMOS W=2.5u L=250n AS=2.25p PS=6.8u AD=2.25p PD=6.8u $ $x=1200 $y=-4700 $w=400 $h=600
MNMOS_5 N_8 G2 N_9 N_7 NMOS W=2.5u L=250n AS=2.25p PS=6.8u AD=2.25p PD=6.8u $ $x=-300 $y=-5600 $w=400 $h=600
MPMOS_4 N_17 N_18 N_19 0 NMOS W=2.5u L=250n AS=2.25p PS=6.8u AD=2.25p PD=6.8u $ $x=200 $y=-700 $w=400 $h=600
MPMOS_5 N_19 N_20 N_21 0 NMOS W=2.5u L=250n AS=2.25p PS=6.8u AD=2.25p PD=6.8u $ $x=200 $y=-1300 $w=400 $h=600
MNMOS_1 N_3 N_20 N_21 Vdd PMOS W=2.5u L=250n AS=2.25p PS=6.8u AD=2.25p PD=6.8u $ $x=1000 $y=-3000 $w=400 $h=600
MNMOS_3 N_3 N_18 N_21 Vdd PMOS W=2.5u L=250n AS=2.25p PS=6.8u AD=2.25p PD=6.8u $ $x=-700 $y=-2900 $w=400 $h=600
MPMOS_1 N_11 G1 N_12 N_10 PMOS W=2.5u L=250n AS=2.25p PS=6.8u AD=2.25p PD=6.8u $ $x=-400 $y=1200 $w=400 $h=600
MPMOS_2 N_13 G2 N_14 Vdd PMOS W=2.5u L=250n AS=2.25p PS=6.8u AD=2.25p PD=6.8u $ $x=1400 $y=1500 $w=400 $h=600
MPMOS_3 N_17 G1 N_16 N_15 PMOS W=2.5u L=250n AS=2.25p PS=6.8u AD=2.25p PD=6.8u $ $x=-400 $y=400 $w=400 $h=600
* Top level device count
* M(NMOS25)     5
* M(PMOS25)     5
* Number of devices: 10
* Number of nodes:   10
```

Fig. 8 Netlist extract on the physical layout of NOR-2 cell.

Table 3 Input signals in FORTRAN NAND-2 gate

Input		Control Signal		Working Condition of Transistors										Output
A	B	G1	G2	P1	P2	P3	P4	P5	N1	N2	N3	N4	N5	Y
0	0	0	0	1	1	1	1	1	0	0	0	0	0	1
0	1	0	0	1	1	1	1	0	0	0	0	0	1	1
1	0	0	0	1	1	1	0	1	0	0	0	1	0	1
1	1	1	1	0	0	0	0	0	1	1	1	1	1	0

Table 4 Input signals in FORTRAN NOR-2 gate

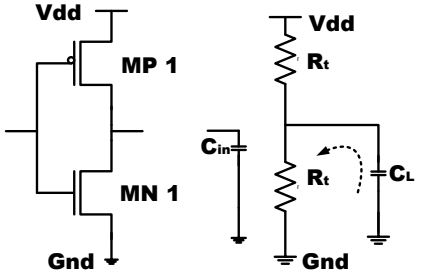
Input		Control Signal		Working Condition of Transistors										Output
A	B	G1	G2	P1	P2	P3	P4	P5	N1	N2	N3	N4	N5	Y
0	0	0	0	1	1	1	1	1	0	0	0	0	0	1
0	1	1	1	0	0	0	1	0	1	1	1	0	1	0
1	0	1	1	0	0	0	0	1	1	1	1	0	1	0
1	1	1	1	0	0	0	0	0	1	1	1	1	1	0

5. COMPARATIVE ANALYSIS OF DELAY

In this section, a systematic delay prototype for an inverter, based on the FORTRAN approach, is clarified and tried to be matched to basic CMOS, INDEP and Sleepy Stack approached. All the approaches are considered as working in an Active mode of operation. Typically, the transistor delay (T_{d0}) of a straight CMOS inverter, as shown in Fig. 9 driving a load of C_L, can be expressed using equation 3.

$$T_{d0} = C_L R_t \tag{3}$$

Where R_t is the transistor resistance, and C_L is the load capacitance. C_{in} indicates the input capacitance. Although the non-saturation mode equation is complicated, it can be predicted the adequate first-order gate delay from the equation (3). At this instant, derivation of delay for other approaches have been achieved one by one and compared with the basic CMOS approach.



(a) (b)

Fig. 9 (a) Inverter Circuit schematic (b) RC equivalent circuit

5.1. INDEP Approach

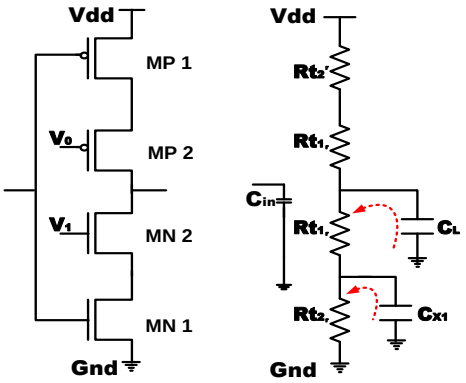
From Fig. 10, delay of INDEP approach can be expressed as

$$T_{d1}= (R_{t1}+R_{t2})\, C_L + R_{t2}C_{X1}$$

Here R_{t1} and R_{t2} both are the resistances of MN2 and MN1 respectively that are connected with forced stack manner, in which the resistance of R_{t1} and R_{t2} will reduce compared to the resistance of R_t of CMOS. The capacitance of C_{X1} is much less than that of $C_{L,}$ as C_{X1} is an internal node capacitance between the two pull-down resistances. Therefore, if $C_{X1} = 0.5C_L$, $R_{t1} = 0.5R_t$, $R_{t2} = 0.5R_t$.

$$\begin{aligned} T_{d1} &= (0.5R_t + 0.5R_t)\, C_L + (0.5R_t)\,(0.5C_L) \\ &= R_tC_L + 0.25R_tC_L \\ &= 1.25R_tC_L \\ &= 1.25T_{d0} \end{aligned} \tag{4}$$

From this, it can be observed that the delay of INDEP approach is almost same as that of CMOS approach.



(a) (b)

Fig. 10 (a) INDEP Inverter Circuit schematic (b) RC equivalent circuit

5.2. Sleepy Stack Approach

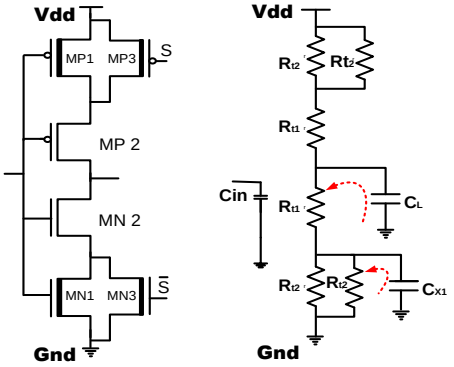
From Fig. 11, delay of the Sleepy Stack approached Inverter can be expressed as

$$T_{d2}= (R_{t1}+0.5R_{t2})\, C_L + 0.5R_{t2}C_{X1}$$

In Sleepy Stack approached, two extra sleep transistors are added as MN1 and MN3 at PDN side, and both are high-Vth transistors that are connected in parallel to each other as shown. Their combined resistance is half of that of R_{t2}. When compared to CMOS, R_{t1} is the resistance of simple transistor, and R_{t2} is high-V_{th} transistor resistance. And the capacitance value of C_{X1} 50% larger to C_L as it is the capacitance connected with three transistors. Therefore, in Sleepy Stack, $R_{t1} = R_t$ and $R_{t2} = 1.25R_t$ and $C_{X1} = 1.5C_L$.

$$T_{d2} = (R_t + 0.5\times1.25R_t)\,C_L + (0.5\times1.25R_t \times 1.5C_L)$$
$$= 1.625R_tC_L + 0.625R_tC_L \quad (5)$$
$$= 2.25R_tC_L$$
$$= 2.25T_{d0}$$

From this, it can be observed that, the delay of Sleepy Stack approach is almost 2.25 times higher compared to CMOS approach.

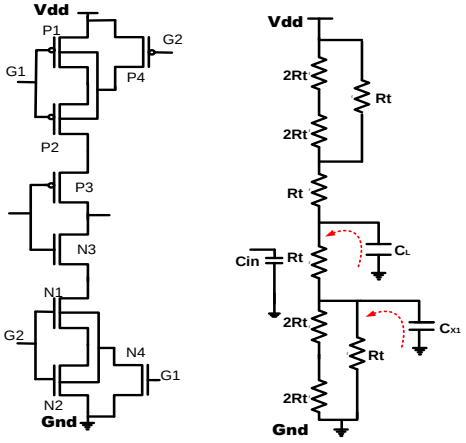


(a) (b)

Fig. 11 (a) Sleepy Stack Inverter Circuit schematic (b) RC equivalent circuit

5.3. FORTRAN Approach

In FORTRAN Approach, to design any circuit, the same low threshold voltage transistor is exploited as utilized in CMOS approach for designing any circuit. Therefore, the resistor value of transistor N_1, N_2 and N_4 in the pull-down network as well as the resistor value of transistor P_1, P_2 and P_4 in the pull-up network will be similar as that of CMOS network's transistors values as shown in Fig 12. Furthermore, transistor N_1 and



(a) (b)

Fig. 12 (a) FORTRAN Inverter Circuit schematic (b) RC equivalent circuit

N_2 are connected in series with each other and combining they are connected parallel with P_4. So, transistors N_1 and N_2 have resistor value double to that of CMOS transistors because these two transistors are connected as forced stack transistors.

The capacitor C_{X1} value is assumed as one-fourth of that of C_L as C_{X1} is the capacitor of two forced stack transistors in series, combining they are parallel with a single transistor. Therefore, the C_{X1} is the value of capacitor for 3 transistors. So, at C_{X1}, three transistors are connected such that two transistors are in series with each other combining there are in series with one transistor. As C_{X1} value of resistances is $(4\times1)/(4+1) = (4/5) = 0.8$ comes. And CX1 is a capacitor connected with four transistors, $C_{X1} = 0.25C_L$.

$$\begin{aligned} T_{d3} &= (0.8)\, R_tC_{X1} + 1.8R_tC_L \\ &= (0.8)\,(0.25R_tC_L) + 1.8R_tC_L \\ &= (10/5)\, R_tC_L \\ &= 2R_tC_L \\ &= 2T_{d0} \end{aligned} \tag{6}$$

From equation 10, it can be observed that the delay of FORTRAN approach is almost two times higher than CMOS approach.

6. Simulation Results

In this section, important simulation results for the FORTRAN approach have been observed. All the experimental data were obtained at 180nm, 130nm and 90nm technology node using TSMC® technology node in Tanner EDA with the bundle of Mentor Graphics. Table 1 shows the values of different parameters taken for measurement purposes in the simulation tool. All the simulation results which are taken from Tanner EDA design tool. All the exhaustive operations are performed on the topology of FORTRAN, which is a verified result.

Table 5 and 6 presents the comparative analysis of NAND-2 and NOR-2 gates. The Average static power has less value as compared to the CMOS, Sleepy stack, INDEP and FORTRON based designs respectively. Table 7 presents the area of the NAND-2 and NOR-2 gates. The leakage power dissipation for NAND and NOR gates for two inputs have been observed. The leakage power is measured at a static phase of the circuit by applying all the possible combinations of inputs. Total leakage power dissipation is the summation of all the leakage power dissipation components for all input combinations. Leakage power dissipation of different benchmark circuits like full adder and a chain of 4 inverters has been measured for proper investigation of the proposed circuit design approach. A comparison of the FORTRAN approach with the conventional CMOS approach is made by considering it at different frequency ranges. From the result illustrated in table 8 and table 9, it can be observed that up to 95-98% of leakage power is saved compared to the standard CMOS technology-based gate.

Table 5 Comparative analysis of NAND-2 Gate

NAND-2	180nm technology node						
	Dynamic Power (µW)	Delay (ns)	Static power (pw) (0,0)	(0,1)	(1,0)	(1,1)	Average Static Power (pW)
CMOS	1.35	138	669	665	684	693	677.75
Sleepy Stack	1.59	170	14.4	384	304	135	209.35
INDEP	1.28	124	2.77	14.1	9.98	154	45.21
FORTRAN	1.16	185	8.57	5.12	3.47	9.46	6.65
	130nm Technology						
	Dynamic Power (µW)	Delay (ns)	(0,0)	(0,1)	(1,0)	(1,1)	Average Static Power (pW)
CMOS			636	208	198	798	460
Sleepy Stack	0.26	100	396	404	417	391	402
INDEP	0.23	71.1	24.81	39.9	41.55	34.75	35.25
FORTRAN	0.19	77.08	18.57	19.19	17.71	10.1	16.39
	90nm Technology						
	Dynamic Power (µW)	Delay (ns)	(0,0)	(0,1)	(1,0)	(1,1)	Average Static Power (pW)
CMOS			483.7	435.8	377.17	637.87	483.63
Sleepy Stack	0.12	62.68	316.5	311.7	325.95	311.27	316.35
INDEP	0.11	45.15	28.71	48.09	43.81	68.39	47.25
FORTRAN	0.09	59.68	18.55	25.28	25.31	21.3	22.61

Table 6 Comparative analysis of NOR-2 Gate

NOR-2	180nm technology node						
	Dynamic Power (µW)	Delay (ns)	Static power (pw) (0,0)	(0,1)	(1,0)	(1,1)	Average Static Power (pW)
CMOS	1.86	5.05	672	676	684	674	676.5
Sleepy Stack	2.3	5.07	764.43	676.9	654.89	141.95	536.43
INDEP	1.73	5.09	18.5	119	115	77.4	64.39
FORTRAN	1.43	5.08	8.82	15.46	13.67	13.92	12.96
	130nm technology node						
	Dynamic Power (µW)	Delay (ns)	(0,0)	(0,1)	(1,0)	(1,1)	Average Static Power (pW)
CMOS			427.24	386.23	395.58	391.75	400.19
Sleepy Stack	0.37	4.97	417.7	400.15	317.21	19.07	288.53
INDEP	0.33	4.96	57.48	18.21	19.01	9.94	26.16
FORTRAN	0.25	5.02	21.31	8.26	10.63	8.17	12.09
	90nm Technology node						
	Dynamic Power (µW)	Delay (ns)	(0,0)	(0,1)	(1,0)	(1,1)	Average Static Power (pW)
CMOS			868	316.02	281.82	41.96	376.95
Sleepy Stack	0.17	4.89	316.71	306.64	315.05	311.5	312.47
INDEP	0.13	4.89	74.1	44.32	41.56	23.28	45.815
FORTRAN	0.11	4.9	25.82	22.88	21.56	19.08	22.33

Table 7 Area comparison of the NAND-2 and NOR-2

Design	CMOS area in mm2	Sleepy Stack	INDEP	FORTRAN
Area (in $\mu m^{2)}$ comparison of the NAND-2	26.92	53.84	65.23	67.37
Area (in $\mu m^{2)}$ comparison of the NOR-2	28.57	56.488	68.59	68.25

Table 8 Comparative analysis of Dynamic power for an inverter at different frequency range

Sr. No.	Fre-quency (MHz)	180nm technology node at 25^0 C		130nm technology node at 25^0 C		90nm technology node at 25^0 C		180nm technology node at 110^0 C		130nm technology node at 110^0 C		90nm technology node at 110^0 C	
Power (µW)		Dynamic power (µW)		Dynamic power (µW)		Dynamic power (µW)		Dynamic power (µW)		Dynamic power (µW)		Dynamic power (µW)	
		CMOS	FORTRAN	CMOS	FORTRAN	CMOS	FORTRAN	CMOS	FORTRAN	CMOS	FORTRAN	CMOS	FORTRAN
1	10	0.22	0.2	0.04	0.03	0.02	0.02	0.25	0.23	0.05	0.04	0.03	0.03
2	20	0.678	0.54	0.12	0.09	0.06	0.05	0.72	0.56	0.14	0.1	0.08	0.06
3	50	1.12	0.86	0.2	0.14	0.1	0.09	1.2	0.9	0.235	0.16	0.12	0.1
4	100	2.25	1.72	0.4	0.29	0.19	0.18	2.39	1.75	0.46	0.31	0.24	0.19
5	200	4.51	3.47	0.79	0.68	0.38	0.37	4.78	3.5	0.9	0.66	0.47	0.39
6	500	11.29	8.38	1.98	1.44	0.96	0.87	11.92	8.7	2.25	1.51	1.15	0.91

Table 9 Comparative analysis of full adder at 180nm technology node

Full Adder Analysis	180nm Technology					
Approach	Dynamic power (µW)	% Saving of Power	Delay (ns)	% Saving of Delay	Leakage Power (nW)	% Saving of leakage Power
CMOS	8.53	_	0.16	_	2.88	_
Sleepy Stack	8.32	+2.46	0.19	-14.72	2.5	13.19%
INDEP	8.21	+3.75	0.18	-08	1.95	32%
FORTRAN	7.25	+15.01	0.18	-12.27	1.84	36%

Table 8 shows the comparative analysis of dynamic power for an inverter circuit at different frequency ranges. From the table, it can be observed that as the temperature and frequency go higher, dynamic power of the FORTRAN approach does not increase in a high amount similar to the CMOS approach. Table 8 shows a comparative analysis of full adder design at the 180nm technology node. From the table, it can be easily understood that dynamic power and leakage power are much more saved in FORTRAN approach compared to other approaches with little increase in delay. We have achieved in Full adder design better saving of power (+36%) but the delay has not found optimal value.

The simulation result of a chain of 4 inverters is shown in Table 9. From the result, one can observe that the static power is effectively reduced in FORTRAN approach compared to all other low-power approaches. Static power is reduced as approximately 98% in the proposed FORTRAN approach compared to the CMOS approach, while Dynamic power is also reduced by almost 19% compared to the CMOS approach increasing the delay by 67%. The general approach for the chain of 4 inverters is given as in Fig. 13. We have taken a simple inverter which is cascaded in 4 chains and the VDD and ground has been kept common in the design. In the case, the chain of 4 inverters we have only achieved 47% delay and 97.99% savings of static power. This shows that there

is a trade off in static power and delay we cannot gain optimal value together. The result of the 4-bit multiplier circuit is compared in Table 11, which shows the superiority of the FORTRAN approach over CMOS approach.

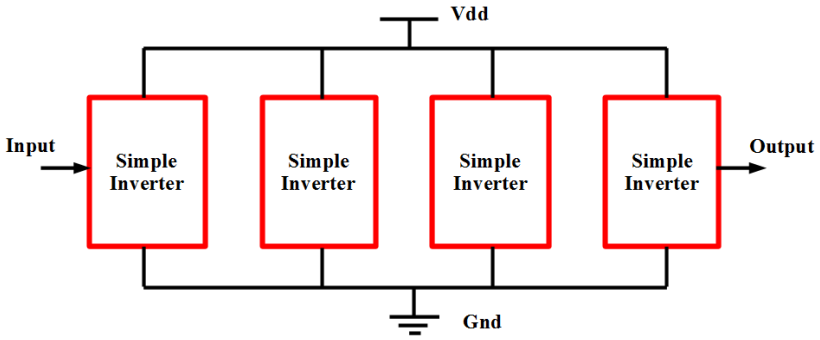


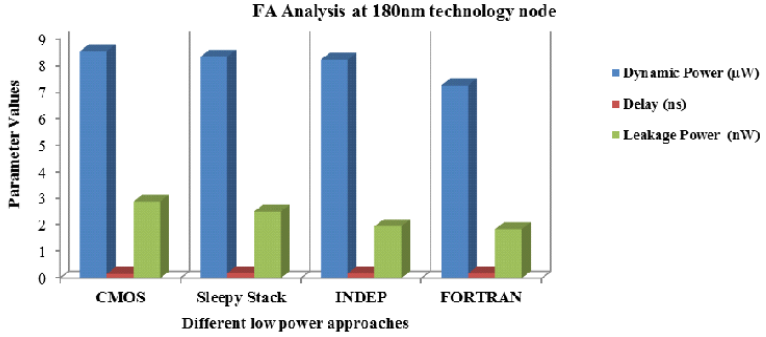
Fig. 13 General approach for a chain of 4 Inverters

Table 10 Comparative analysis of Chain of 4 Inverters

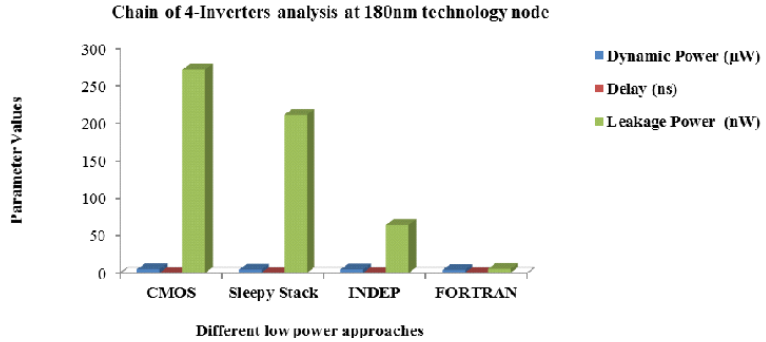
Chain of 4 INVERTER	180nm technology node					
	Dynamic power (µW)	% Saving of Dynamic Power	Delay (nS)	% Saving of Delay	Average Static Power (pW)	% Saving of Static Power
CMOS	5.22		0.28		2721.50	
Sleepy Stack	4.60	11.88	0.40	-40.57	2115.50	22.27
INDEP	4.97	4.79	0.39	-37.01	644.98	76.30
FORTRAN	4.23	18.97	0.47	-66.90	54.66	97.99

Table 11 Comparative analysis of 4-bit Multiplier

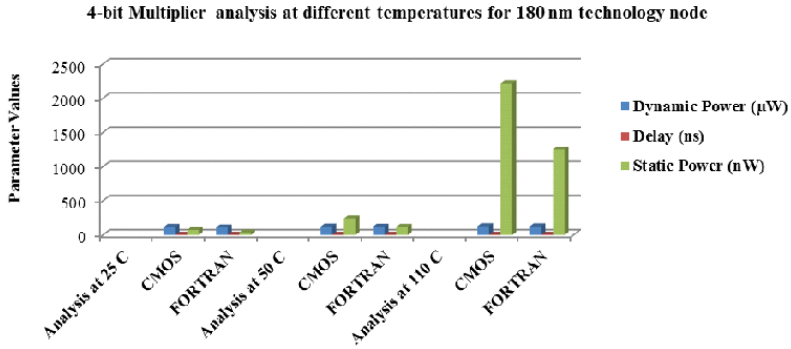
Analysis of 4-bit Multiplier	Analysis at 25^0 C									
Approach	Dynamic Power (10^{-4}) µW	% Saving of Dynamic power	Delay (ns)	% Saving of Delay	Static Power (nW) A=(0000) B=(0000)	A=(0011) B=(1100)	A=(1100) B=(0011)	A=(1111) B=(1111)	Average Static Power (nW)	% Saving of Static power
CMOS	1.18	~	4.11	~	59.75	71.91	72.24	88.75	73.16	~
FORTRAN	1.11	5.93	3.81	7.3	36.21	36.12	36.13	36	36.11	50.64
Analysis at 50^0 C										
CMOS	1.23	~	4.05	~	197.43	236.22	237.67	286.2	239.38	~
FORTRAN	1.21	1.62	3.73	7.9	115.39	115.03	133.14	114.02	119.395	50.12
Analysis at 110^0 C										
CMOS	1.29	~	3.9	~	1871.08	2201.11	2221.82	2563.06	2214.26	~
FORTRAN	1.26	2.32	3.55	8.97	1302	1127.36	1295.94	1272.98	1249.57	43.56



(a)



(b)



(c)

Fig. 14 Comparison of proposed FORTRAN approach with reported approaches, (a) & (b) comparison with different approaches and (c) comparison at different temperature ranges

In figure 14, three types of temperature are considered such as 25^0C, 50^0C and 110^0C. Two technologies, CMOS and FORTRAN technology have been considered to get the dynamic power, static power, and delay. Figure 14 shows the simulation graph of the proposed FORTRAN approach with various reported approaches for FA, a chain of 4-

inverters and 4-bit multiplier designs. From Fig. 14 (a) and 14 (b), it can be perceived that the dynamic power, delay and static power consumed is very less in FORTRAN approach compared to other approaches. Same as the functionality of the proposed FORTRAN approach is also checked against CMOS approach at different temperature ranges, as depicted in Fig. 14 (c) at 180nm technology node for 4-bit Multiplier. It can be observed that as the temperature goes high, the dynamic power and static power increases in CMOS approach, but in FORTRAN approach, dynamic as well as static power does not increase in such a high proportion similar to the CMOS approach. Therefore, the FORTRAN approach gives decent results compared to other approaches at a nanoscale regime.

7. CONCLUSION

In a deep-0.1sub-micron regime, sub-threshold leakage power dissipation is almost equal to a dynamic power dissipation, which requires to be minimized effectively with great care. Furthermore, in battery-operated devices specifically, for which battery life is of prime concern, leakage power has become a more critical issue to be solved. In this paper, a novel and efficient circuit-level leakage power reduction approach of FORTRAN is presented, which can minimize leakage power as well as dynamic power in a decent amount. The main advantage of the FORTRAN approach is that only low threshold voltage transistors are used in its circuit design structure, which is also the mainstream requirement of the current VLSI industry. Various types of circuits like full adder, a chain of 4 inverters and 4-bit Multiplier have been analyzed for comparative analysis of the FORTRAN approach with the other well-known leakage power reduction approaches available for leakage current reduction. FORTRAN approach decreases leakage power from 95 to 98%, dynamic power from 15 to 20% with a slight increase in the delay. The delay can be compensated, considering that one wants to implement the proposed circuit design approach predominantly for battery-operated devices.

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