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INTRODUCING AN OPTIMAL QCA CROSSBAR SWITCH FOR BASELINE NETWORK

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Abstract. *Crossbar switch is the basic component in multi-stage interconnection networks. Therefore, this study was conducted to investigate performance of a crossbar switch with two multiplexers. The presented crossbar switch was simulated using quantum-dot cellular automata (QCA) technology and QCA Designer software, and was studied and optimized in terms of cell number, occupied area, number of clocks, and energy consumption. Using the provided crossbar switch, the baseline network was designed to be optimal in terms of cell number and occupied area. Also, the number of input states was investigated and simulated to verify accuracy of the baseline network. The proposed crossbar switch uses 62 QCA cells and the occupied area by the switch is equal to $0.06\mu m^2$ and its latency equals 4 clock zones, which is more efficient than the other designs. In this paper, using the presented crossbar switch, the baseline network was designed with 1713 cells, and occupied area of $2.89\mu m^2$.*

Key words: *QCA, Crossbar switch, MUX, Baseline Network, Multi-stage interconnection networks, Energy dissipation*

1. INTRODUCTION

Today, density of devices, power consumption, and speed of response are among challenges of designing electronic circuits. Sizes of semiconductor devices have reached sub microns, increasing level of complexity in design of chips. According to Moore's Law, the number of transistors in a chip doubles every 18 months, meaning an increase in circuit density and power consumption in the chips [1]. The increase in density of the circuits means shrinking of the transistors inside the chips, and this shrinkage in complementary metal-oxide-semiconductor (CMOS) technology increases leakage current and creates a short channel effect [2].

Problems in downsizing CMOS technology have led to introduction of new emerging technologies, such as Fin field-effect transistor (FinFET), carbon nanotube field-effect transistor (CNTFET), and quantum-dot cellular automata (QCA), among which QCA technology can be the best alternative to CMOS in designing of digital circuit [3-5]. QCA cells are quantum cells that in binary state consist of four quantum wells and two electrons forming stable states of electrons for polarization in QCA [6-8].

In QCA cells, transfer of current from one cell to another is zero because electrons can only tunnel inside each cell, and information can only be transmitted through transfer of state from one cell to another. This technology has the least energy consumption due to the lack of current transfer between cells. The advantages of QCA technology include high response speed, low occupied area, and low energy consumption, which will make this technology a leader in designing the future digital circuits [9]. Among the circuits designed using QCA, one can mention to design of adder circuits [10], serial-parallel converter [11], counter [12], serial-in to serial-out (SISO) shift register [13], multiplier [14], and comparator circuit [15].

Another advantage of using QCA is design of complex digital systems. Parallel communication systems, multiprocessors, and design of network communication systems within chips can be mentioned as examples of complex digital systems [16-17]. In multiprocessor systems, communication between processors is required from input to output; this connection can be established through nodes in the network [18-20]. Using control lines in each switch used in each node, path of data transfer from the desired input to output is specified.

Interconnection networks that can be implemented using QCA technology include butterfly, dragonfly, beyond network, etc. In this study, an optimal crossbar switch is presented considering occupied area, the number of cells, and the amount of latency in the switch. Then, interconnection structure of the baseline network will be presented using the proposed crossbar switch.

In rest of the paper, section 2 describes the QCA. The proposed crossbar switch and baseline network will be presented in section 3 and section 4. Finally, section 5, concludes the paper.

2. QCA

The QCA cell was first proposed by Lent [21] and was developed in 1997 [22]. Each QCA cell contains four potential wells and two electrons enclosed in a square [23-25]. Two electrons inside each square can freely tunnel between the quantum-dots in each cell, but electrons cannot leave the enclosed square and tunnel from one cell to another.

Data transfer in QCA cells from one cell to another is done through external electrostatic energy and in fact, information is not transmitted through current. Two stable states are formed based on placement of electrons in each QCA cell creating -1 and +1 polarizations in the QCA (steady state occurs in QCA cells at the greatest distance between the electrons in each cell) [26-31]. Fig. 1 depicts structure of the QCA cell.
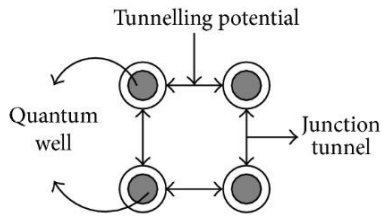
Fig. 1 QCA cell structure

The QCA uses clocks to control tunneling and data synchronization. The clock in QCA has four phases: switch, hold, release, and relax [19, 25, 27]. Fig. 2 illustrates phase clock in the QCA.
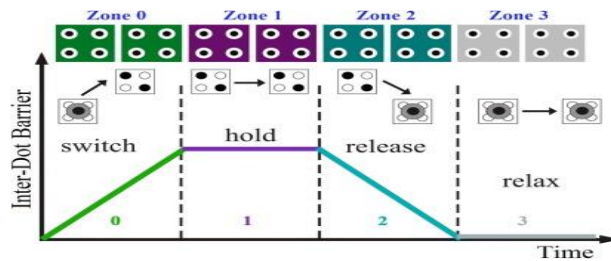
Fig. 2 Phase clock in QCA

In the switch phase, the potential of barrier slowly increases, and kinetic energy of the electrons decreases. After the switch phase, the cell will enter the hold phase, in which the barrier potential reaches the highest level and kinetic energy in this phase is almost zero. After the hold phase, the release phase occurs, in which the potential of barrier slowly begins to decrease, electrons are slowly released, and kinetic energy begins to increase. The next phase is the relax phase. In this phase, the potential level reaches its lowest point and electrons can tunnel freely inside the cell [19, 25, 27].

As mentioned, the QCA cell has two polarizations of -1 and 1, which can be attributed to logic levels of 0 and 1, respectively, and basic gates of binary logic can be implemented by these polarizations in QCA [6-8]. Fig. 3 shows the basic gates in QCA.
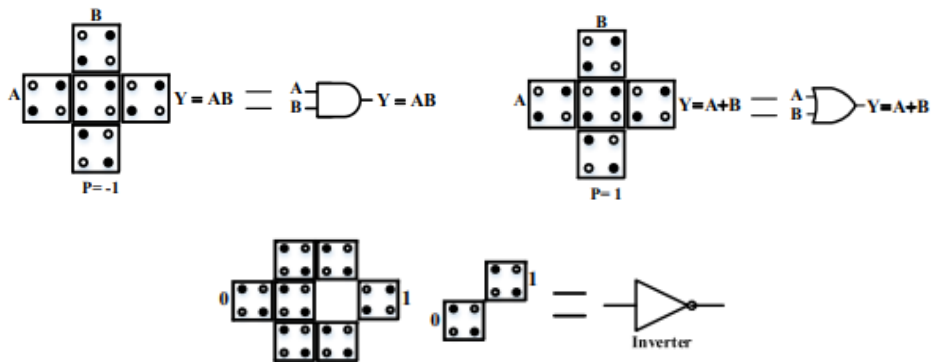
Fig. 3 Basic gates in QCA

3. PROPOSED CROSSBAR SWITCH

In this section, at first, crossbar switch is designed and implemented and then, application of switch crossbar will be reviewed in the baseline network.

In this study, QCA Designer software version 2.0.3 was used to simulate circuit and QCAPro software was used to calculate energy consumption. The parameters used in QCA Designer software are as follows:

Number of samples: 50000
Convergence Tolerance: 0.001000
Radius of Effect (nm): 65
Relative permittivity: 12.9
Clock High: 9.8 e-22
Clock Low: 3.8 e-23
Clock Shift: 0
Clock Amplitude Factor: 2.000000
Layer Separation: 11.500000
Maximum Literation's Per Sample: 100

3.1. Crossbar switch

A crossbar switch is a digital system connecting an input to an output using a control line with respect to a pattern. This pattern is created using the control line, for example, if the control line is equal to 0, the Input 1 information is transferred to Output 1 and Input 2 to Output 2, or if the control line is equal to 1, Input1 is transferred to Output 2 and Input 2 to Output 1 as shown in Fig. 4. Using the crossbar switch, the connection between nodes can be created crosswise, and the control line is used to create a connection between the nodes in the form of a bar and cross. Fig. 4 shows the two states of bar and cross configured using the control line.
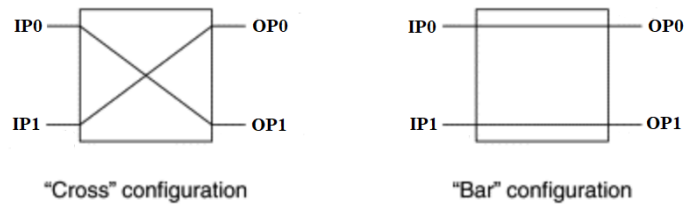
Fig. 4 Crossbar switch configuration

Table 1 shows truth table of a crossbar switch, which can be simplified by Karnaugh map to provide a relationship between input and output of a crossbar switch. Eqs. 5 and 6 are related to crossbar switches, and each of the outputs OP0 and OP1 shows a 2:1 multiplexer relationship, and each multiplexer (MUX) is controlled across the control line.

Table 1 Truth table for crossbar switch

| Control line	IP1	IP0	OP1	OP0
0	0	0	0	0
0	0	1	0	1
0	1	0	1	0
0	1	1	1	1
1	0	0	0	0
1	0	1	1	0
1	1	0	0	1
1	1	1	1	1

$$OP_0 = IP_0.\overline{C} + IP_1.C \qquad (1)$$

$$OP_1 = IP_0.C + IP_1.\overline{C} \qquad (2)$$

Fig. 4 shows the states created in data transfer in a crossbar switch, which uses Eqs. 1 and 2 to design such a switch. These two equations indicate the existence of two multiplexers in the crossbar switch, which can be used to create states in the crossbar switch using the control line. Fig. 5 shows wiring of a crossbar switch by two multiplexers, using Eqs. 1 and 2.
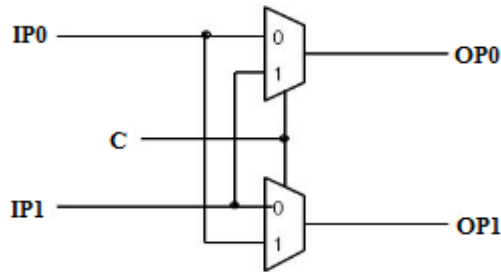
Fig. 5 Crossbar switch using two multiplexers

Fig. 6 shows the MUX circuit used in this study. Fig. 7 shows simulation results of the MUX. In the used MUX, if C=0, the output will be equal to IP1 and if C=1, the output will be equal to IP0.
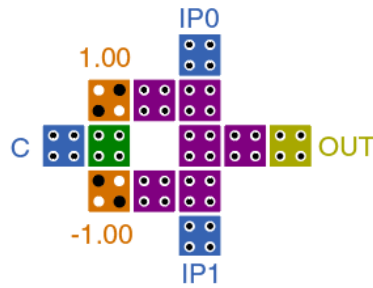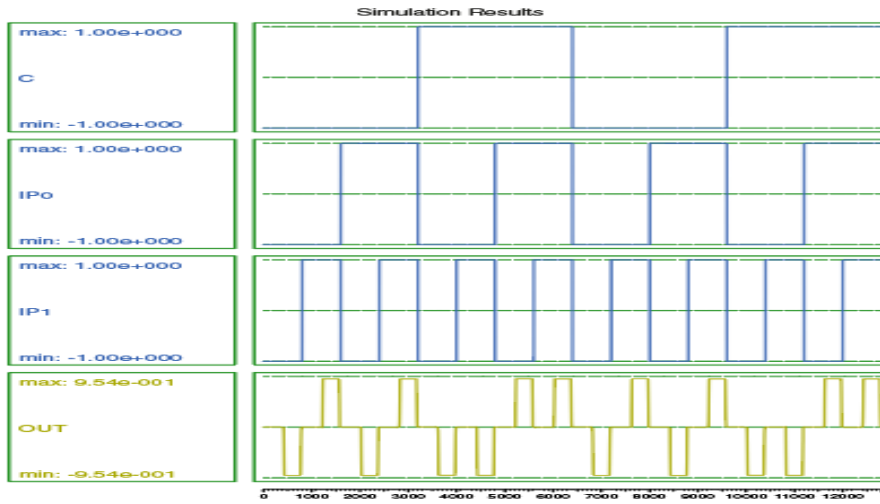

Fig. 6 MUX circuit

Fig. 7 MUX simulation result

In the following, design of the crossbar switch using QCA is presented. Fig. 8 shows implementation of the crossbar switch using QCA technology, and Fig. 9 illustrates the simulation results for the crossbar switch. In Table 2, the values obtained from measuring number of cells, occupied area, and latency in the proposed crossbar switch are compared with those reported by the other previous works.
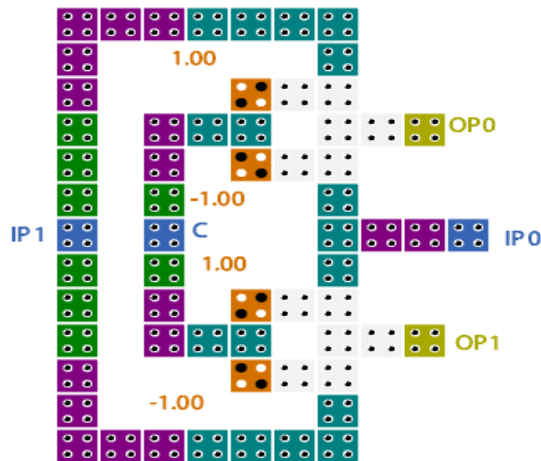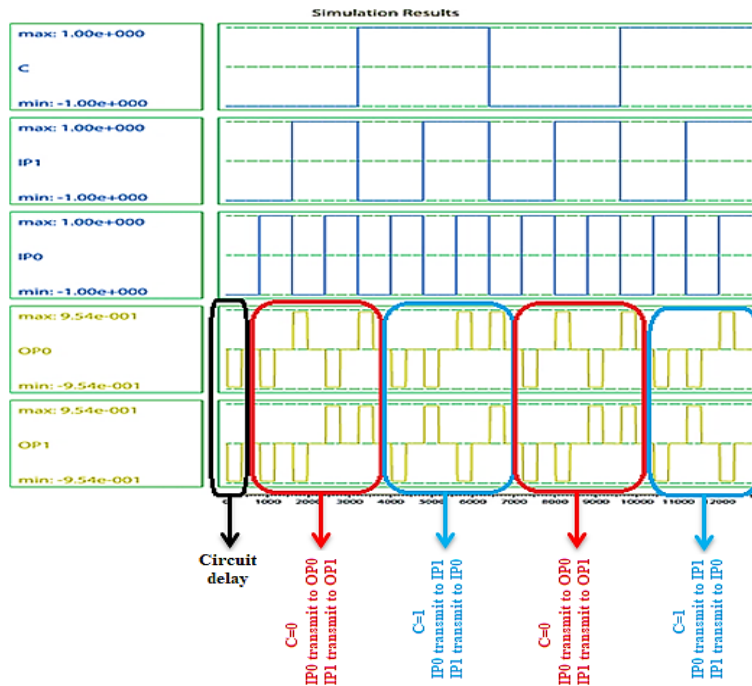

Fig. 8 Crossbar switch with QCA

Fig. 9 Result simulation for crossbar switch

Fig. 9 illustrates transfer of input to output, where for C=0 the IP0 and IP1 data are transferred to OP0 and OP1, respectively (shown with a red square in Fig. 9). For C=1, IP0 data are transferred to OP1 and IP1 data are transferred to OP0, as shown in Fig. 9 with a blue square.

Table 2 Compare crossbar switch with other work

Structure	Parameters		
	Cell count	Total Area (μm^2)	Latency (Clock zone)
crossbar switch [18]	101	0.096	8
crossbar switch [19]	157	0.25	6
crossbar switch [20]	123	0.137	8
crossbar switch [36]	81	0.08	4
crossbar switch this work	62	0.06	4

According to Table 2, the proposed crossbar switch has an optimized design in terms of cell number, occupied area, and latency. In the circuit designed in this study, 62 cells were used with an occupied area of $0.06\mu m^2$ and latency equal to 4 zone clocks or one clock pulse.
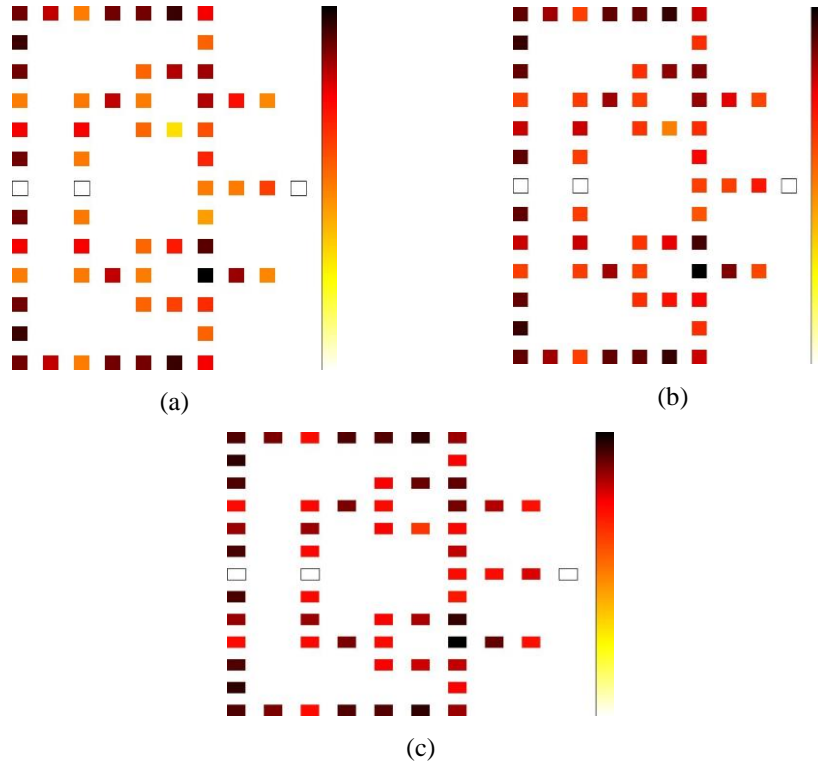
3.2. Energy dissipation on crossbar switch

In this section, energy in the proposed crossbar switch designed using QCA cell will be investigated. In calculation of the consumed energy, the Hamiltonian matrix is needed, which is obtained using the Hartree-Fock approximation. Eq. 7 shows the Hamiltonian

matrix in QCA [32, 33]. In Eq. 3, P is the polarization value in binary QCA that is equal to 1 or -1; E_k is the kinetic energy, and γj is the tunneling energy in QCA.

$$H(j) = \begin{bmatrix} -\dfrac{E_k}{2} P_j & -\gamma j \\ -\gamma j & \dfrac{E_k}{2} P_j \end{bmatrix} \tag{3}$$

Energy value of the QCA cell can be measured by calculating the Hamiltonian matrix and quantum measurement in the QCA.

Herein, the amount of dissipated energy was calculated using QCA Pro software. Energy dissipation was calculated for the values of $0.5E_k$, $1 E_k$ and $1.5 E_k$, as shown in Table 3. Fig.10 depicts thermal layout of crossbar switch circuit for energy dissipation.

(a)   (b)

(c)

Fig. 10 Thermal Layout for average energy dissipated in Crossbar switch circuit. a) Thermal Layout for $0.5E_k$. (b) Thermal Layout for $1E_k$. (c) Thermal Layout for $1.5E_k$

**Table 3** Energy dissipation for Crossbar switch circuit

γ/EK	0.5	1	1.5
Avg E_{diss} (meV)	109.19	133.85	166.17
Max E_{diss} (meV)	219.46	227.44	244.82
Min E_{diss} (meV)	17.14	55.24	100.20

4. BASELINE NETWORK

In the previous section, a crossbar switch was simulated using two multiplexers and was studied in terms of cell number, occupied area, latency, and consumed energy. Now, the baseline network is simulated using the proposed crossbar switch, and the proposed baseline network is investigated for several selected states.

Baseline network is one of various types of multistage interconnection networks (MINs) and a subset of delta network, consisting of several layers, and each layer includes several 2×2 switches [34, 35]. Each baseline network consists of 2^q rows and $q+1$ set, and each node contains a 2×2 switch. The baseline network is presented in the form of 2×8, which has eight inputs and eight outputs, as designed using a crossbar switch. Fig. 11 shows the building block of baseline network.
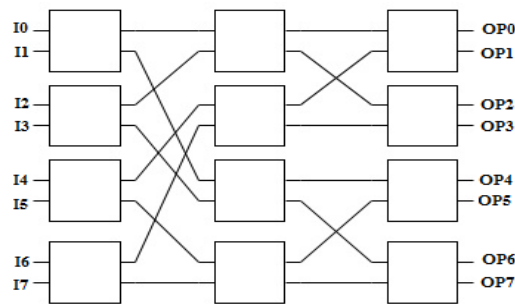
Fig. 11 Baseline network diagram

4.1. Implementation of Baseline Network by QCA

The aim of the present study was presenting and implementing a baseline network optimally in terms of the number of cells and occupied area, simulating the target baseline network using QCA technology and QCA Designer software. In this simulation, the proposed baseline network has eight inputs, eight outputs, and 12 crossbar switches. Fig. 12 illustrates the designed baseline network by QCA technology. In the simulated baseline network, 1713 QCA cells were used, the occupied area by the baseline network was equal to 2.89µm^2 and the latency was equal to 5 clocks or 20 clock zones. Table 4 presents the parameterized results in the baseline network and compares the results.

Table 4 Baseline network comparison results

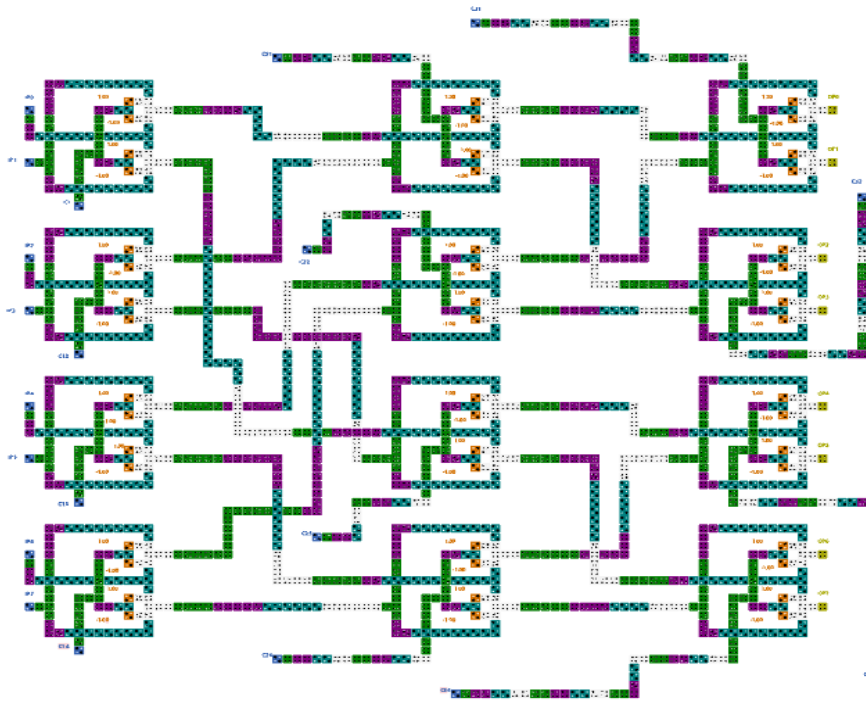| Structure	Parameters		
	Cell count	Total Area (µm^2)	Latency (Clock zone)
Baseline network [19]	2491	3.85	18
Baseline network with this work	1713	2.89	20

Fig. 12 Designed baseline network with QCA

4.2. Simulation scenarios

In simulation of the baseline network, eight input lines and 12 control lines were used. A large number of inputs and control lines cause the displayed waveform to be distorted, for this reason, vector table setup of the QCA Designer software was used to display the waveforms. In this regard, vector table setup forms were used to display inputs and control lines. In the first scenario, all the control inputs are equal to 0. The simulation results are shown in Fig. 13, in which the input data have been transported in the output. Table 5 shows the input-to-output transmissions done by control lines. Fig. 13 illustrates latency of the baseline network with the purple box. Latency was equal to 5 clock pulses as shown in Fig. 13. The baseline network outputs are shown with the red box.

Table 5 State of input to output transport in the first scenario

INPUT	OUTPUT
I0	OP0
I1	OP4
I2	OP2
I3	OP6
I4	OP1
I5	OP5
I6	OP3
I7	OP7

Fig. 13 Output result for input state of first scenario

According to Fig. 13 and Table 5, for all control lines to be zero, information I0 to OP0, I1 to OP4, I2 to OP2, I3 to OP6, I4 to OP1, I5 to OP5, I6 to OP3, I7 will be transferred to OP7.

In the second scenario, all control inputs are 1 and the results are shown in Fig. 14. Table 6 shows the input-to-output transmissions.
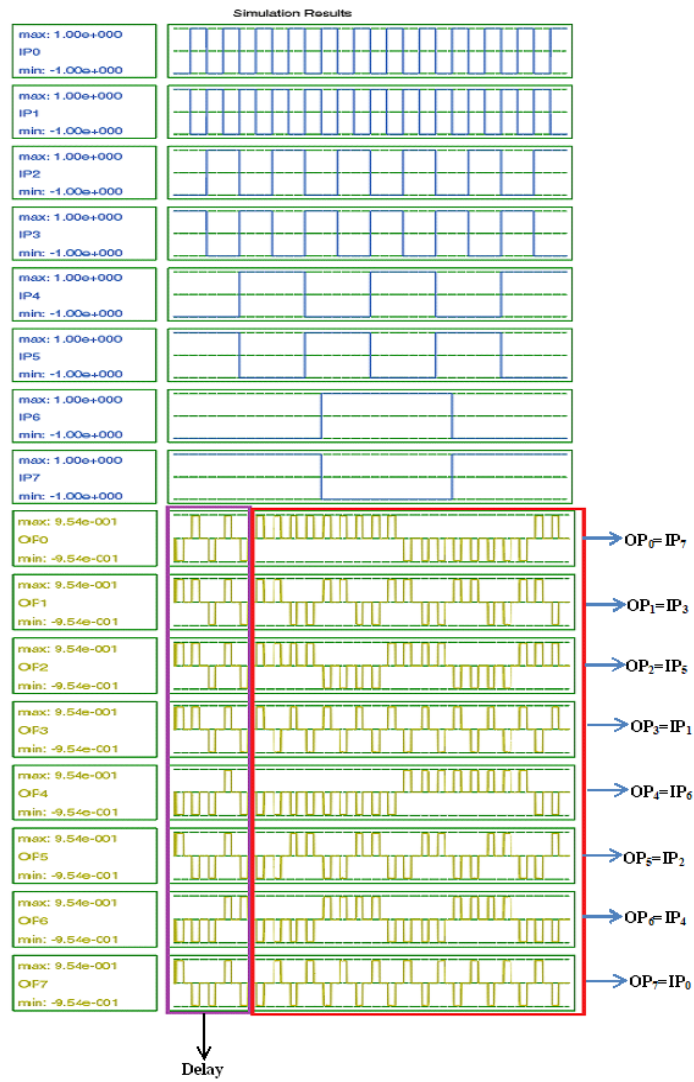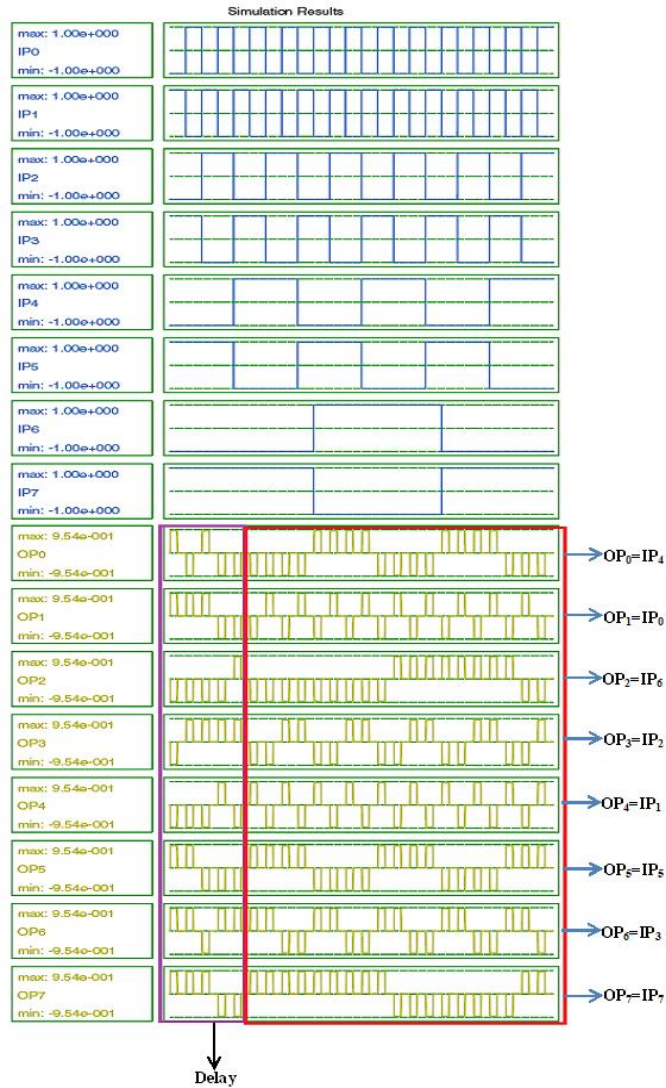
Fig. 14 Output result for input state of second scenario

Table 6 State of input to output transport in the second scanrio

INPUT	→	OUTPUT
I0	→	OP7
I1	→	OP3
I2	→	OP5
I3	→	OP1
I4	→	OP6
I5	→	OP2
I6	→	OP4
I7	→	OP0

According to Fig. 14 and Table 6, for all control lines to be 1, information I0 to OP7, I1 to OP3, I2 to OP5, I3 to OP1, I4 to OP6, I5 to OP2, I6 to OP4, I7 will be transferred to OP0.

Fig. 15 Output result for input state of third scenario

In the third scenario, control input C31 and C32 are 1 and other control lines are 0 and simulation results are shown in Fig. 15. Table 7 depicts the input-to-output transmissions that are done by control lines. Fig. 15 illustrates the latency of the baseline network and the outputs of baseline network. In the simulation results of Fig. 15, the latency is equal to 5 clock pulses.

Table 7 State of input to output transport in the third scenario

INPUT	OUTPUT
I0 ⟶	OP1
I1 ⟶	OP4
I2 ⟶	OP3
I3 ⟶	OP6
I4 ⟶	OP0
I5 ⟶	OP5
I6 ⟶	OP2
I7 ⟶	OP7

According to Figs. 15 and Table 7, control lines C31 and C32 are 1 and other control lines are 0, and information will be transferred as Table 7.

5. CONCLUSION

In this paper, an optimized crossbar switch was studied in terms of cell number, occupied area, number of clocks, and energy consumption. The switch uses 62 QCA cells and the occupied area by the switch is equal to $0.06\mu m^2$ and latency is equal to 4 clock zones, which is more efficient than the other designs presented in the literature. In the provided switch, the amount of consumed energy for 0.5Ek, 1Ek, and 1.5Ek was calculated by QCA Pro software. Then, the baseline network was designed with 1713 cells and occupied area of $2.89\mu m^2$ using the presented crossbar switch. For validating data transfer in the simulated baseline network, three scenarios were considered. In the first scenario, all the control lines are equal to 0 where the information from I0 to OP0, I6 to OP3, I7 will be transferred to OP7. In the third scenario, control input C31 and C32 are equal to 1 and other controls are equal to 0 where information from I0 to OP1, I1 to OP4, I2 to OP3, I3 to OP6, I7 will be transferred to OP7.

The baseline network was optimized in terms of the number of cells and occupied area, but the amount of zone clock was increased and for correct operation of the designed baseline network, states such as input and control lines were applied to the baseline network, and the input corresponding to the control lines was transferred to the output. Therefore, it can be concluded that the proposed crossbar switch can be used in optimizing other networks.

REFERENCES

[1] G.E. Moore, McGraw-Hill New York, NY, USA, 1965.
[2] T.J.K. Liu, K. Kuhn, CMOS and beyond: logic switches for terascale integrated circuits, Cambridge University Press, 2015.
[3] S. Garg, T.K. Gupta, "A 4: 1 multiplexer using low-power high-speed domino technique for large fan-in gates using FinFET", *Circuit World*, 2020.
[4] D.K. Nandhaiahgari, R.P. Somineni, C.R. Kumari, "Design and analysis of different full adder cells using new technologies", *International Journal of Reconfigurable and Embedded Systems*, vol. 9, p. 116, 2020.
[5] R. Sabbaghi-Nadooshan, Z. Shahosseini, D. Rezaeipour, "Design of new QCA LFSR and NLFSR for Grain-128 stream cipher", *Journal of Circuits, Systems and Computers*, vol. 25, p. 1650005, 2016.

[6] S. Zoka, M. Gholami, "Two Novel D-Flip Flops with Level Triggered Reset in Quantum Dot Cellular Automata Technology", *International Journal of Engineering - Transactions C: Aspects*, vol. 31, no. 3, pp. 415–421, 2017.

[7] J. Iqbal, F. Khanday, N. Shah, "Design of Quantum-dot Cellular Automata (QCA) based modular 2^n-1-2^nMUX-DEMUX", IN Proceedings of the IMPACT-2013, 2013, pp. 189–193.

[8] S. Kamrani, S.R. Heikalabad, "A unique reversible gate in quantum-dot cellular automata for implementation of four flip-flops without garbage outputs", *International Journal of Theoretical Physics,* vol. 57, pp. 3340–3358, 2018.

[9] F. Ahmad, "An optimal design of QCA based 2n: 1/1: 2n multiplexer/demultiplexer and its efficient digital logic realization", *Microprocessors and Microsystems,* vol. 56, pp. 64–75, 2018.

[10] H.R. Roshany, A. Rezai, "Novel efficient circuit design for multilayer QCA RCA", *International Journal of Theoretical Physics*, vol. 58, pp. 1745–1757, 2019.

[11] L.E. Arani, A. Rezai, "Novel circuit design of serial–parallel multiplier in quantum-dot cellular automata technology", *Journal of Computational Electronics*, vol. 17, pp. 1771–1779.

[12] M.N. Divshali, A. Rezai, S.F.H. Samidpour, "Design of novel coplanar counter circuit in quantum dot cellular automata technology", *International Journal of Theoretical Physics*, vol. 58, pp. 2677–2691.

[13] M.N. Divshali, A. Rezai, A. Karimi, "Towards multilayer QCA SISO shift register based on efficient D-FF circuits", *International Journal of Theoretical Physics*, vol. 57, pp. 3326–3339, 2018.

[14] S.M. Mohaghegh, R. Sabbaghi-Nadooshan, M. Mohammadi, "Design of a ternary QCA multiplier and multiplexer: a model-based approach", *Analog Integrated Circuits and Signal Processing*, vol. 101, no. 1, pp. 23–29, 2019.

[15] A. Shiri, A. Rezai, H. Mahmoodian, "Design of efficient coplanar comparator circuit in QCA technology", *Facta Universitatis, Series: Electronics and Energetics*, vol. 32, 119–128, 2019.

[16] R. Sabbaghi-Nadooshan, M. Modarressi, H. Sarbazi-Azad, "The 2D digraph-based NoCs: attractive alternatives to the 2D mesh NoC", *The Journal of Supercomputing*, vol. 59, no. 1, pp. 1–21, 2012.

[17] R. Sabbaghi-Nadooshan, A. Patooghy, "Analytical performance modeling of de Bruijn inspired mesh-based network-on-chips", *Microprocessors and Microsystems*, vol. 39, no. 1, pp. 27–36, 2015.

[18] J.C. Das, D. De, "Design of single layer banyan network using quantum-dot cellular automata for nanocommunication", *Optik,* vol. 172, pp. 892–907, 2018.

[19] M.A. Tehrani, F. Safaei, M.H. Moaiyeri, K. Navi, "Design and implementation of multistage interconnection networks using quantum-dot cellular automata", *Microelectronics Journal,* vol. 42, pp. 913–922, 2011.

[20] J.C. Das, D. De, "Circuit switching with quantum-dot cellular automata", *Nano communication networks,* vol. 14, pp. 16–28, 2017.

[21] C.S. Lent, P.D. Tougaw, W. Porod, G.H. Bernstein, "Quantum cellular automata", *Nanotechnology*, vol. 4, p. 49, 1993.

[22] A. Orlov, I. Amlani, G. Bernsten, C. Lent, G. Snider, "Realization of a functional cell for quantum-dot cellular automata", *Science,* vol 277, pp. 928–930, 1997.

[23] Z. Mohammadi, K. Navi, R. Sabbaghi-Nadooshan, "Design of testable reversible latches by using a novel efficient implementation of Fredkin gate", *International Journal of Electronics*, vol. 107, no. 6, pp. 859–878, 2020.

[24] Z. Taheri, A. Rezai, H. Rashidi, "Novel Single Layer Fault tolerance RCA Construction for QCA Technology", *Facta Universitatis, Series Electronics and Energetics*, vol. 32, no. 4, pp. 601–613, 2019.

[25] R. Kianpour, R. Sabbaghi-Nadooshan, "Novel Design of n-bit Controllable Inverter by Quantum-dot Cellular Automata", *International Journal Nanoscience and Nanotechnology*, vol. 10, no. 2, pp. 117–126, 2014.

[26] J.R. Monfared, A. Mousavi, "Design and simulation of nano-arbiters using quantum-dot cellular automata", *Microprocessors and Microsystems*, vol. 72, p. 102926, 2020.

[27] M. Abutaleb, "A novel QCA shuffle-exchange network architecture with multicast and broadcast communication capabilities", *Microelectronics Journal*, vol. 93, 104640, 2019.

[28] R. Kianpour, R. Sabbaghi-Nadooshan, "Optimized Design of Multiplexor by Quantum-dot Cellular Automata", *International Journal Nanoscience and Nanotechnology*, vol. 9, no. 1, pp. 15–24, 2013.

[29] J.C. Das, D. De, "Nanocommunication network design using QCA reversible crossbar switch", *Nano communication networks*, vol. 13, pp. 20–33, 2017.

[30] L. Silva, L. Sardinha, M. Vieira, L. Vieira, O.V. Neto, "Robust serial nanocommunication with QCA", *IEEE Trans. Nanotechnol.*, vol. 13, no. 3, pp. 464–472, 2015.

[31] H.A. Mousavi, P. Keshavarzian, A.S. Molahosseini, "A novel fast and small XOR-base full-adder in quantum-dot cellular automata", *Appl Nanosci*, vol. 10, pp. 4037–4048, 2020.

[32] S. Srivastava, S. Sarkar, S. Bhanja, "Power dissipation bounds and models for quantum-dot cellular automata circuits", In Proceedings of the Sixth IEEE Conference on Nanotechnology, 2006, vol. 1, pp. 375-378.

[33] J. Timler, C.S. Lent, "Power gain and dissipation in quantum-dot cellular automata", *Journal of applied physics,* vol. 91, pp. 823–831, 2002.

[34] J. Duato, S. Yalamanchili, L.M. Ni, "Interconnection Networks: An Engineering Approach", Morgan Kaufmann, 2003.

[35] D. Tutsch, M. Marcus Brenner, "MIN simulate. A multistage interconnection network simulator", In Proceedings of the 17th European Simulation Multiconference: Foundations for Successful Modelling & Simulation, 2003, pp. 211–216.

[36] A. Chandrasekaran, K. Senthil Kumar, K. Hemalatha, K.S. Tamilselvan, P. Umarani, "Design of Coplanar Circuit Switching Network in Quantum Dot Cellular Automata", *International Journal of Recent Technology and Engineering*, vol. 8, no. 4, pp. 10611–10619, 2019.