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DESIGN AND PERFORMANCE ANALYSIS OF FULL ADDER USING 6-T XOR–XNOR CELL

K Srinivasa Rao, Marupaka Aditya, B.S.D. Karthik Raja, CH. Manisai, M. Tharun Sai Reddy, K. Girija Sravani

Department of ECE, Koneru Lakshmaiah Education Foundation, Vaddeswaram, India

Abstract. *In this paper, the design and simulation of a high-speed, low power 6-T XOR-XNOR circuit is carried out. Also, the design and simulation of 1-bit hybrid full adder (consisting of 16 transistors) using XOR-XNOR circuit, sum, and carry, is performed to improve the area and speed performance. Its performance is being compared with full adder designs with 20 and 18 transistors, respectively. The performance of the proposed circuits is measured by simulating them in Microwind tool using 180 and 90nm CMOS technology. The performance of the proposed circuit is measured in terms of power, delay, and PDP (Power Delay Product).*

Key words: *XOR-XNOR circuit, Hybrid full adder*

1. INTRODUCTION

Logic gates are the basic building blocks of any digital system design. It is an electronic circuit having at least one input and only one output. Logic gates are primarily executed utilizing diodes or transistors acting as electronic switches. Logic circuits include devices such as multiplexers, registers, arithmetic logic units (ALUs), and computer memory, all the way up through complete microprocessors, which may contain in excess of 100 million gates. At present, most gates are made from MOSFETs. The basic circuits we are more familiar at are adders.

There are two types of adders namely half adder and full adder. Half adder which is having two inputs and two outputs are not used in practical applications. Full adders, which are having three inputs and two outputs are being mostly used in applications, like, generating memory addresses inside a computer and to make the Program Counter point to next instruction, the ALU makes use of this adder, FFT algorithms, FIR and IIR filters etc. [1] The conventional full adders used in ALU contains around 28 transistors, which results

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Corresponding author: K Srinivasa Rao
Department of ECE, Koneru Lakshmaih Education Foundation (Deemed to be University), Vaddeswaram, India
E-mail: srinivasakarumuri@gmail.com

in more power consumption, delay in output and area. But people today are keener on using technology, which is simple, small, easily carriable, and more reliable for longer time and can be used in more applications. All the above aspects have led to the development of hybrid technology. The building of low power hybrid VLSI systems has emerged as a significant performance goal because of the fast growing technology in mobile communications and computation. [2] Hybrid technology is the combination of two or more different logic styles. Mainly the hybrid 1-bit full adder is a combination of CMOS logic design style, transmission gate logic and pass transistor logic. [3] Most of the hybrid adders are lacking with poor driving capability and power delay product (PDP) when operated at lower voltages.

In [3], hybrid logic full adder using 10 transistors XOR-XNOR circuit is proposed and performance parameters like power consumption, delay, PDP and driving capabilities are simulated in Cadence virtuoso tool using 90-nm CMOS technology. The proposed XOR–XNOR circuit is based on CPL and cross-coupled structure. A full adder was also proposed using the same XOR-XNOR circuit, sum and carry as shown in Fig.1.

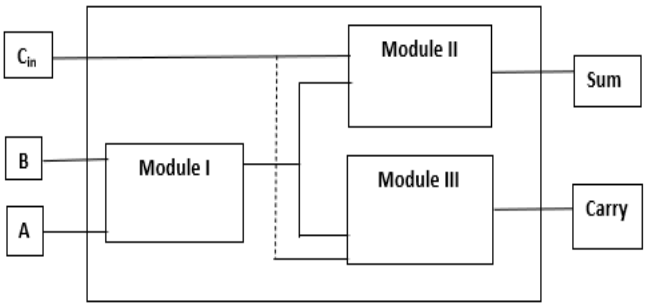

Fig. 1 Block diagram of hybrid logic FA circuit [3]

In [4], circuits of XOR/XNOR and simultaneous XOR-XNOR circuits are proposed. The proposed XOR-XNOR circuit has 12 transistors and not having a NOT gate on its critical path shows good performance on terms of power consumption, delay, low output capacitance, driving capability and robustness. The proposed XOR–XNOR circuit is saving almost 16.2%–85.8% in PDP, and it is 9%–83.2% faster than the other circuits. In [5], a technique is proposed to access the timing behavior of hybrid full adder, made of both CMOS and FinFET technologies of size 32-nm, and compare their performance in multistage circuits in HSPICE tool. The circuits include transistor function full adder (TFA), transmission gate full adder (TGA), New-HPSC (Hybrid Pass Static CMOS), New-14T full adder and a CCMOS full adder (Conventional CMOS).

In this proposed method, three parameters have been considered for timing behavior namely speed, driving capability and input capacitance. In [6], a design of hybrid full adder using Pass transistors, transmission gates and CMOS logic is proposed. The full adder is implemented in 45-nm technology in Cadence simulation tool. Performance parameters of the proposed full adder is compared with performance of twenty existing full adders with supply voltage ranging from 0.4V to 1.2V. In [7], a 1-bit hybrid full adder using modified XNOR gates is proposed to improve the area & speed and compare its performance with conventional full adder. Performance analysis of the proposed design is simulated in 90-

nm technology with 1.2 V supply voltage. The research is still going on to get a full adder which is applicable for practical applications and at the same time providing good performance in all aspects.

In this paper, our focus is to reduce transistor count and delay of a full adder and then to compare it with the 20 and 18 transistor full adder. First, we tried to present the proposed logic in Xilinx software, which is taking a long time. Then we had the option to do in Tanner software, but the software was not licensed and was not compatible to make circuit with 90-nm and lower nm technologies. Finally, we have constructed the circuit in DSCH tool, converted this into a Verilog file and simulated in Microwind tool.

The rest of the paper is organized as follows: In Section II, the two input 6-T XOR-XNOR Cell is proposed and the full adder (FA) using the proposed XOR–XNOR circuit is also proposed in the same section. In Section III, the performance of the proposed XOR–XNOR cell and full adder in terms of power, speed, and PDP is compared with those of available XOR–XNOR circuits and FAs. Section IV concludes the paper.

2. PROPOSED DESIGN

2.1. XOR-XNOR Circuit

XOR-XNOR circuits are the basic building block of many arithmetic and encryption circuits. The proposed XOR-XNOR circuit consists of six transistors as shown in Fig.2. It consists of three PMOS and three NMOS transistors. Here we are using two inverter circuits, one for getting the inverted input of A and other to get inverted output of XOR operation, that is XNOR output. This circuit provides full swing outputs simultaneously.

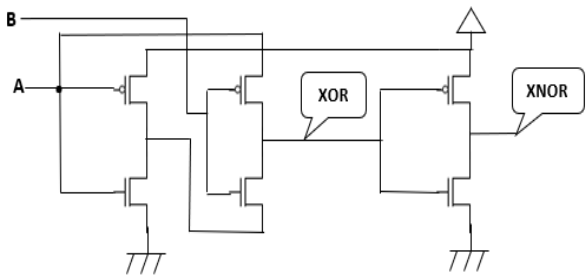

Fig. 2 Proposed XOR–XNOR circuit

2.2. Full Adder Circuit

For hybrid logic design, full adder is designed using XOR-XNOR, sum and carry circuits. Here we shall be considering the sum (Fig.3) and carry (C_{out}) (Fig.4) circuits with the following expressions (1) & (2):

$$\text{Sum} = (A \oplus B)C' + (A \oplus B)'C = (A \oplus B \oplus C) \quad (1)$$

$$C_{out} = (A \oplus B)C + AB \quad (2)$$

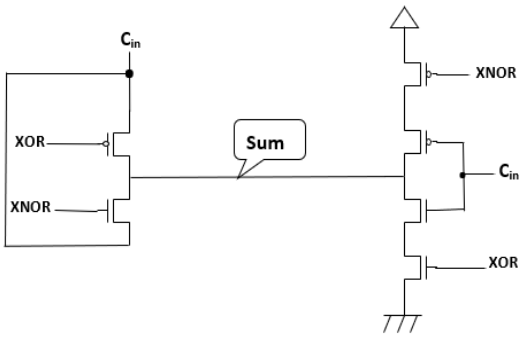

Fig. 3 Sum Module

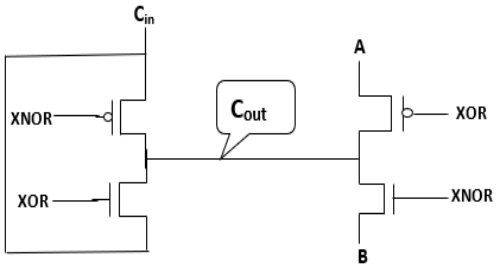

Fig. 4 Carry Module

Both sum and carry circuits are constructed using CMOS logic wherein, sum circuit uses six transistors and provides good driving capability and high robustness and carry circuit uses four transistors and consumes lesser power while providing better delay. The proposed XOR-XNOR circuit in Section 2.1, sum (Fig.3) and carry (Fig.4) circuits discussed above are combined to form a full adder of 16 transistors as shown in Fig. 5.

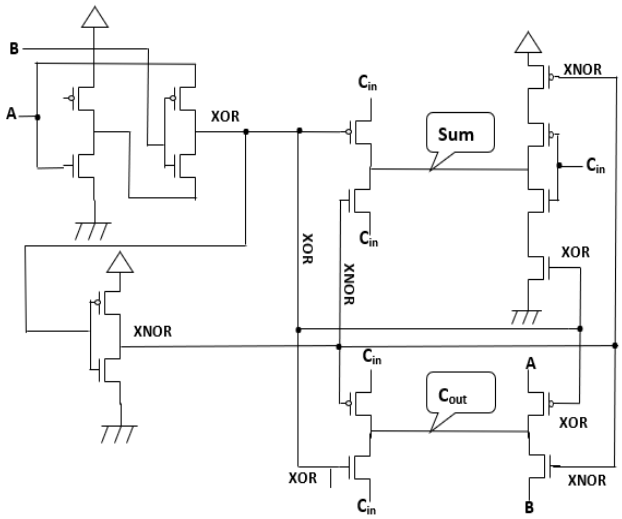

Fig. 5 Proposed Full Adder circuit

Using the logical expressions (1) and (2), truth table for this full adder can be derived as follows:

Table 1 Truth Table of Full-adder

Inputs			Outputs	
A	B	Cin	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

3. Results and Discussion

All the circuits which were discussed in previous section are built in DSCH tool and converted into a Verilog file and then compile this file in Microwind tool to get the required circuits as shown in Fig.6 and Fig.8 and verified the performance parameters such as delay, power, and PDP at various supply voltages ranging from 0.5 V to 1.2 V at random frequencies.

3.1. XOR-XNOR Circuit

In the XOR-XNOR circuit only two inputs A and B are required which are taken as piecewise linear (pwl) input signal. Fig. 6 shows the circuit design in Microwind tool and Fig.7 shows the applied input pattern to the corresponding XOR–XNOR circuit. In output graph, there are small glitches, but they do not have more affect and we get full swing at the output. Hence, we get the XOR-XNOR outputs simultaneously, which is required for full adder design.

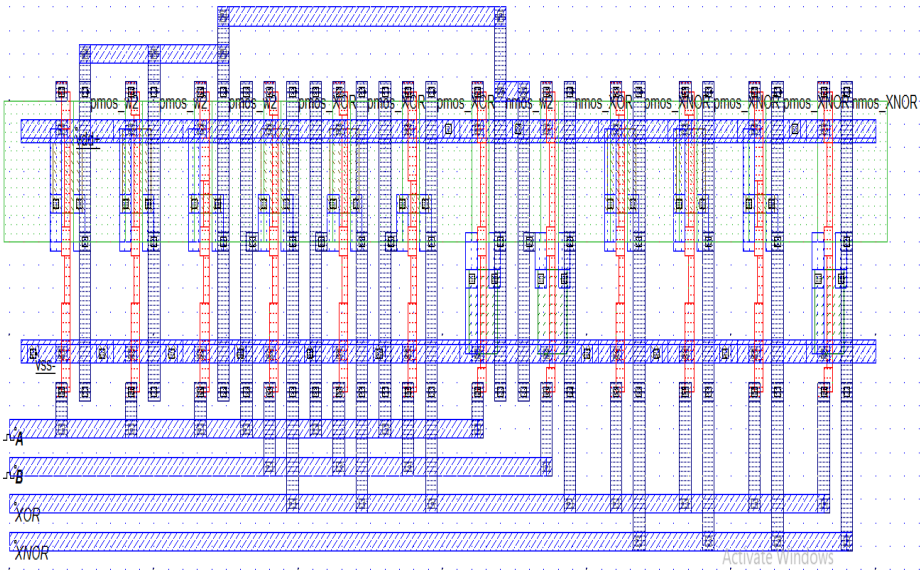

Fig. 6 Proposed XOR–XNOR circuit in Microwind

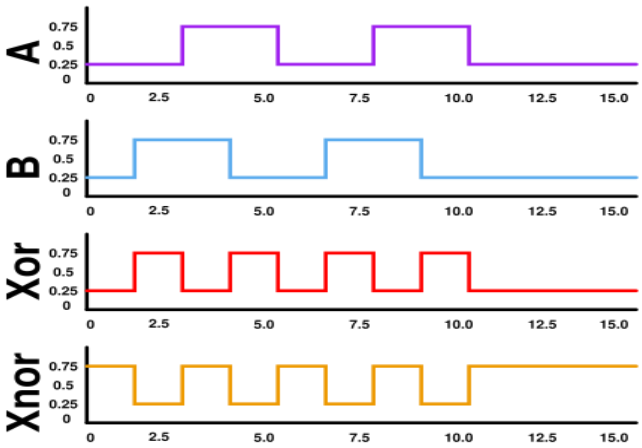

Fig. 7 Input–output waveforms for the proposed XOR–XNOR circuit

Performance of the same XOR-XNOR circuit is compared at in two different CMOS technologies, i.e., 180 and 90 nm, respectively. For calculation of PDP the worst-case delay of XOR and XNOR outputs is taken. In Table I, XOR circuit delay, in Table II, XNOR circuit delay, in Table III power consumption and in Table IV PDP values are compared.

Table 2 XOR Circuit Delay (ps)

	Technologies	
Input Voltages	180 nm	90 nm
0.5 V	31	11
0.6 V	35	13
0.7 V	40	16
0.8 V	52	19
0.9 V	86	23
1.0 V	86	30
1.1 V	105	36
1.2 V	120	49

Table 3 XNOR Circuit Delay (ps)

	Technologies	
Voltages	180 nm	90 nm
0.5 V	0	0
0.6 V	15	15
0.7 V	42	24
0.8 V	65	25
0.9 V	83	37
1.0 V	98	43
1.1 V	115	55
1.2 V	126	62

Table 4 XOR Power Consumption of XOR-XNOR Circuit (uW)

	Technologies	
Voltages	180 nm	90 nm
0.5 V	6	2
0.6 V	10	4
0.7 V	11	5
0.8 V	12	6
0.9 V	13	7
1.0 V	15	7
1.1 V	15	8
1.2 V	16	9

Table 5 PDP of XOR-XNOR Circuit

	Technologies	
Voltages	180 nm	90 nm
0.5 V	186	22
0.6 V	350	26
0.7 V	440	72
0.8 V	624	75
0.9 V	1118	100
1.0 V	1204	150
1.1 V	1725	325
1.2 V	1712	650

As the technology is scaled down, the power as well the PDP values, have a good improvement, when operated in between 0.7 V-1 V. From the above values it can be concluded that whether the delays may have been very high, still the power and PDP values will be suitable for practical use at lower supply voltages.

3.2. Full Adder Circuit

Fig. 8 shows the full adder circuit design in Microwind tool and Fig.9 shows the applied input pattern and the corresponding full adder circuit. The circuit provides full swing outputs with small glitches.

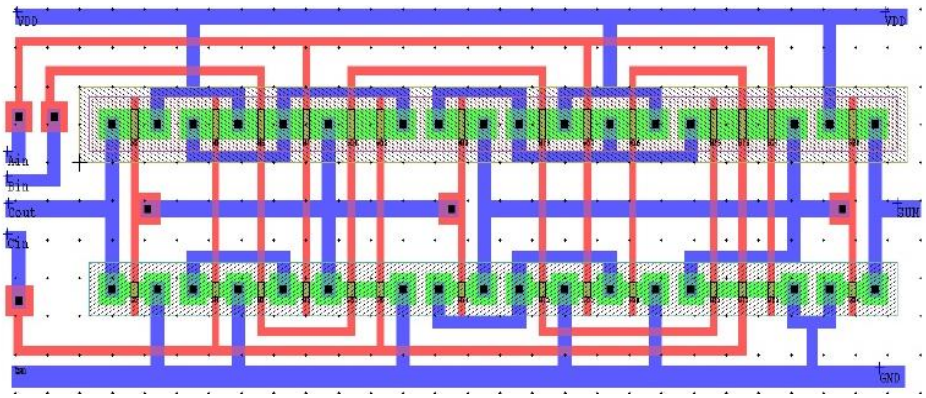

Fig. 8 Proposed FA circuit in Microwind

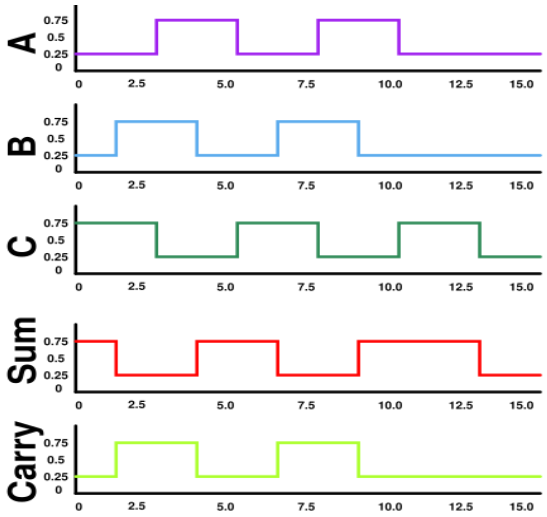

Fig. 9 Input–output waveforms for the proposed FA circuit

Performance of the same full adder circuit is compared with two different CMOS technologies, i.e., 180 and 90 nm, respectively. For delay calculation, C_{in} to C_{out} delay is considered as this delay is crucial for most of the high-level designs. In Table 6, delay, in Table 7 power consumption and in Table 8 PDP values are compared.

Table 6 Full Adder Circuit Delay (ps)

	Technologies	
Voltages	180 nm	90 nm
0.5 V	1120	1021
0.6 V	1062	1023
0.7 V	1074	1026
0.8 V	1081	1029
0.9 V	1088	1030
1.0 V	1094	1029
1.1 V	1098	1030
1.2 V	1120	1031

Table 7 Power Consumption of Full Adder Circuit (uW)

	Technologies	
Voltages	180 nm	90 nm
0.5 V	6	6
0.6 V	21	7
0.7 V	32	9
0.8 V	38	10
0.9 V	43	12
1.0 V	48	16
1.1 V	53	35
1.2 V	58	75

Table 8 PDP of Full Adder Circuit

	Technologies	
Voltages	180 nm	90 nm
0.5 V	6720	6126
0.6 V	22302	7161
0.7 V	34368	9234
0.8 V	41078	10290
0.9 V	46784	10360
1.0 V	52512	16464
1.1 V	58194	36050
1.2 V	68032	77325

A comparison of the full adder designs with 20T [3] and 18T full adder is done in the form of graphs considering each parameter both in 180 and 90nm technologies, for supply voltages from 0.5 V to 1.2V as shown in Fig. 10.

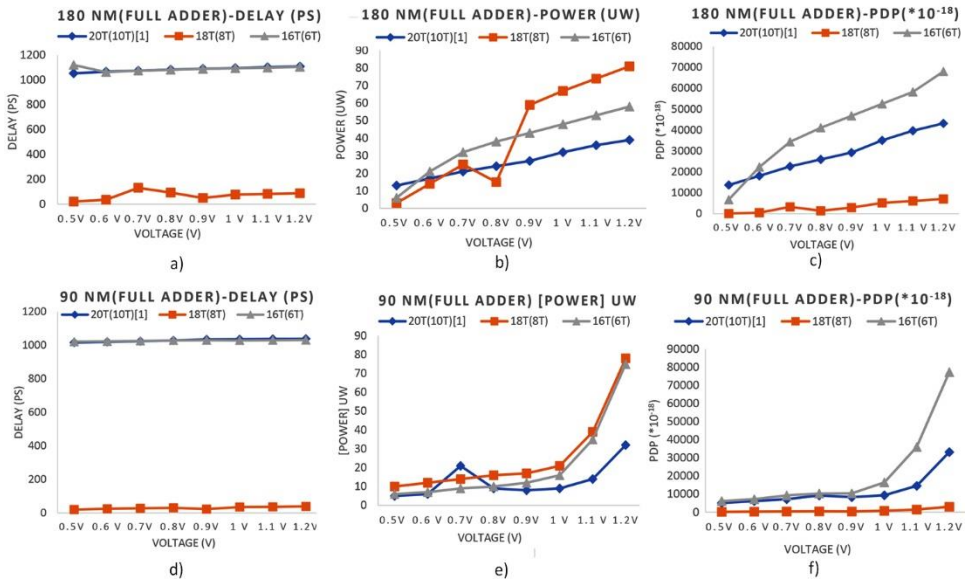

Fig. 10 (a) Delay, (b) Power, (c) PDP [180nm] and (d) Delay, (e) Power, (f) PDP [90nm] comparison utilizing different supply voltages 0.5V-1.2V

The delay of the proposed circuit is compared in Fig. 10(a) and Fig. 10(d), power is compared in Fig. 10(b) and Fig. 10(e), PDP is compared in Fig.10(c) and Fig. 10(f). The proposed circuit shows good performance in terms of power and PDP. Although, the delay values are high, but can be applicable for practical uses because the circuit uses least number of transistors.

The approach presented here, faces the challenge in reducing power consumption and delay. This can be controlled by replacing the MOSFETs with the FinFETs.

Table 9 Overall Comparison of 180-nm technology

Parameters	180nm Full Adders			
	Voltage (V)	**20T**	**18T**	**16T**
Delay	**0.7V**	1075	131	1074
	0.8V	1082	93	1081
	0.9V	1089	49	1088
	1V	1095	77	1094
Power	**0.7V**	21	25	32
	0.8V	24	15	38
	0.9V	27	59	43
	1V	32	67	48
PDP	**0.7V**	22575	3275	34368
	0.8V	25968	1395	41078
	0.9V	29241	2891	46784
	1V	35040	5159	52512

Table 10 Overall Comparison of 90-nm technology

Parameters	90nm Full Adders			
	Voltage (V)	**20T**	**18T**	**16T**
Delay	**0.7V**	1024	28	1026
	0.8V	1029	31	1029
	0.9V	1034	23	1030
	1V	1035	35	1029
Power	**0.7V**	21	14	9
	0.8V	9	16	10
	0.9V	8	17	12
	1V	9	21	16
PDP	**0.7V**	7168	392	9234
	0.8V	9261	496	10290
	0.9V	8272	391	10360
	1V	9315	735	16464

Table 9 and Table 10 represent the overall comparison of the performance parameters using 180 nm and 90 nm technology, respectively.

Here both the 20T and 18T full adder designs used for comparison of parameters were again designed in Microwind software and obtained different values and compared with our 16T full adder. The previous work was done on cadence tool [4], since we were unable to get same software hence, we performed again using Microwind software.

Table 11 Comparison of Performance parameters of proposed architecture and existing architectures

Architecture	Power (mW)
Proposed	21
[27]	53
[28]	25
[29]	40
[30]	71

Table 11 gives the performance comparison of different architectures in terms of Power. As can be seen that the power consumed of the proposed adder is lower in comparison to that of existing architectures.

4. CONCLUSION

In this paper, a new XOR-XNOR circuit consisting of six transistors is proposed which reduces complexity of the circuit and provides full swing outputs simultaneously. This circuit is combined with sum and carry circuits to form a 16-T full adder circuit. The performance of the proposed XOR-XNOR circuit and the full adder are tested by simulating them using Microwind tool using 180 and 90 nm CMOS technology. The proposed circuits show good performance in terms of power and PDP at lower supply voltages between 0.7 V-1 V. The proposed full adder circuit at 90 nm technology is applicable for higher order cascaded full adder circuits and practical applications at lower supply voltages. It the same circuit is tested in another software, then result could have been much better, and this circuit can be used in applications like digital signal processing, microprocessors etc.

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