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A NON-ISOLATED HIGH STEP-UP CONVERTER WITH LOW RIPPLE INPUT CURRENT AND REDUCED VOLTAGE STRESS

Asghar Salehi, Mohammad Hossein Ershadi, Mehdi Baharizadeh

Department of Electrical Engineering, Khomeinishahr Branch, Islamic Azad University, Khomeinishahr/Isfahan, Iran

Abstract. *In this paper a new non-isolated high step-up interleaved cascade converter is presented. In comparison with the conventional cascade boost converter, the proposed converter has a higher voltage gain, lower input current ripple and reduced voltage stress for the switches and diodes. Besides, unlike the conventional cascade boost converter, in the proposed converter the input current is shared between inductors and hence the converter can be implemented with lower current rated inductors. Thus, the converter size and conduction losses are reduced and the efficiency is increased. The proposed converter is analyzed and experimental results of a 200W laboratory prototype are presented.*

Key words: *DC-DC converters, soft switching, high step up, voltage stress.*

1. INTRODUCTION

Nowadays, DC microgrid systems due to their self-sustainability in small areas have been receiving attention and are expected to be the next generation of power systems. Renewable energy sources, such as wind and solar, are increasingly being integrated into the electric power grid, while the power system becomes more tightly intertwined with other systems, such as buildings, natural gas pipelines, and the transportation sector. In microgrid systems, renewable energy sources including photovoltaic (PV), wind turbine, waves, and geothermal sources are utilized for generating DC power and batteries, ultra-capacitors, and fuel cells are adopted as backup power sources for the renewable energy sources [1]-[3]. However, since these power sources usually generate a low voltage, a high step-up DC–DC converter is required to supply high operating voltages loads [4].

For step-up applications, a conventional boost converter can be applied due to its simple circuit and low cost. However, it is not suitable for high step-up applications due to high duty cycle for the converter switch, high voltage stress of the power devices, reverse recovery problems, high conduction losses, stability problems in control and efficiency limitation [5]-[8].

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Corresponding author: Mohammad Hossein Ershadi
Department of Electrical Engineering, Khomeinishahr Branch, Islamic Azad University, Khomeinishahr/Isfahan, Iran
E-mail: ershadi@iaukhsh.ac.ir

To reach a high voltage gain, two or more boost converters can be connected in series. These converters are called cascade converters [9]. To reduce the number of required components, quadratic boost converters are proposed in [10]-[12]. In these converters, the two series boost converters are integrated and the converter needs only one switch. However, since the input voltage is low and all the input current flows from the first stage inductor, the size, volume and conduction losses of this inductor increase drastically as the output power increases. To solve this problem, interleaved technique can be used in order to share current between modules [13]. However, the voltage gain of two stage cascade boost converter is still limited and more than two stage cascade boost converters suffer from low efficiency, complex circuit and control, and high cost [10].

In recent years various interleaved high step up converters are presented in which the input current of the converter is shared between the interleaved phases. In [14] and [15], switched capacitor technique is applied to the interleaved boost converter and the voltage gain has increased. Although in these converters the voltage gain is higher than conventional boost converter, it is still limited and the voltage stress of semiconductor devices are high. In [16]-[19], coupled inductors are used instead of main inductors in interleaved boost converter and the turn ratio of the coupled inductors is employed to adjust the voltage gain. However, because a high turn ratio is required to obtain a high voltage gain higher than 15, the size of the coupled inductor and the conduction loss of the winding and the core loss increase. Moreover, a snubber circuit or clamping circuit is needed due to the leakage inductance from the coupled inductor [19]-[23]. Besides, in [18] the input current of the converter is pulsating and its ripple is high. To decrease the input current ripple, three coupled inductors are adopted in [20] and [21] which increase the converter size and complexity.

To solve the problems of conventional cascade boost converter and avoid using coupled inductors, in this paper a new non-isolated high step-up interleaved cascade converter is presented. The proposed converter has a higher voltage gain in comparison to the two stage cascade boost converter and interleaved boost converter. Moreover, the voltage stress of the switches in the proposed converter is reduced and the input current is shared between converter inductors. Besides, the input current ripple in the converter has decreased compared to the conventional cascade boost converter. Hence, the converter can be implemented with lower current rated inductors, and the converter size and conduction losses are reduced and efficiency is increased.

The rest of the paper is organized as follows. The proposed converter operation principals are described in Section II. In section III, converter analysis and design considerations are discussed in details. Experimental results of a prototype converter are presented in Section IV and conclusions are given in Section VI.

2. PROPOSED CONVERTER OPERATION PRINCIPLE

Fig. 1 shows the proposed interleaved high step-up converter. In order to indicate the operation of the proposed converter, some assumptions are made:

1) All semiconductor components are ideal;

2) The output capacitor C_O and capacitors C_1~C_3 are large enough and can be considered as voltage sources;

3) The inductors L_1, L_2 and L_3 are large enough and the converter operates in continuous-current-mode (CCM);

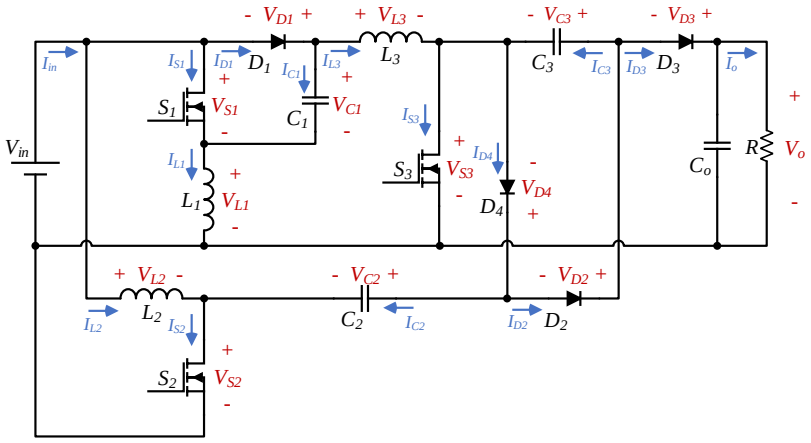

Fig. 1 Proposed interleaved high-step up converter.

With respect to above assumptions, each switching period can be divided into four modes and the key operating waveforms of the proposed converter and equivalent circuits are shown in Fig. 2 and Fig. 3, respectively. Likewise, the two-phase interleaved converters, switches S_2 and $S_3$are driven with the phase shift angle of 180ºand duty cycles of them are equal. The gate pulse of switch S_1 is similar to S_2 as it is shown in Fig. 2.

Interval I, [t_0-t_1]: Fig. 3(a) shows the equivalent circuit of the converter in this interval and as it is shown in the figure, switches S_1 and S_2 are turned off and S_3 is turned on. In this interval inductors L_1 and L_2 are discharged through pathsV_{in}-D_1-C_1-L_1 and V_{in}-L_2-C_2-D_2-C_3-S_3, respectively. In addition, inductor L_3 is charged through V_{in}-D_1- S_3-L_3. The equations of converter elements in this interval are as follows:

$$I_{L1}(t) = I_{L1}(t_0) - \frac{V_{C1} - V_{in}}{L_1} \times (t - t_0) \tag{1}$$

$$I_{L2}(t) = I_{D2}(t) = I_{L2}(t_0) - \frac{V_{C3} - V_{in} - V_{C2}}{L_2} \times (t - t_0) \tag{2}$$

$$I_{L3}(t) = \frac{V_{in}}{L_3} \times (t - t_0) + I_{L3}(t_0) \tag{3}$$

$$I_{D1}(t) = I_{L1}(t) + I_{L3}(t) \tag{4}$$

$$I_{S3}(t) = I_{L2}(t) + I_{L3}(t) \tag{5}$$

Interval II, [t_1-t_2]: This interval begins when switches S_1 and S_2 turn on. As it is shown in Fig. 3(b), in this interval all of the switches are turned on and inductors L_1, L_2 and L_3 are charged through V_{in}-S_1-L_1, V_{in}-S_1-C_1-L_3-S_3 and V_{in}-L_2-S_2, respectively. Important equations of converter elements are as follows:

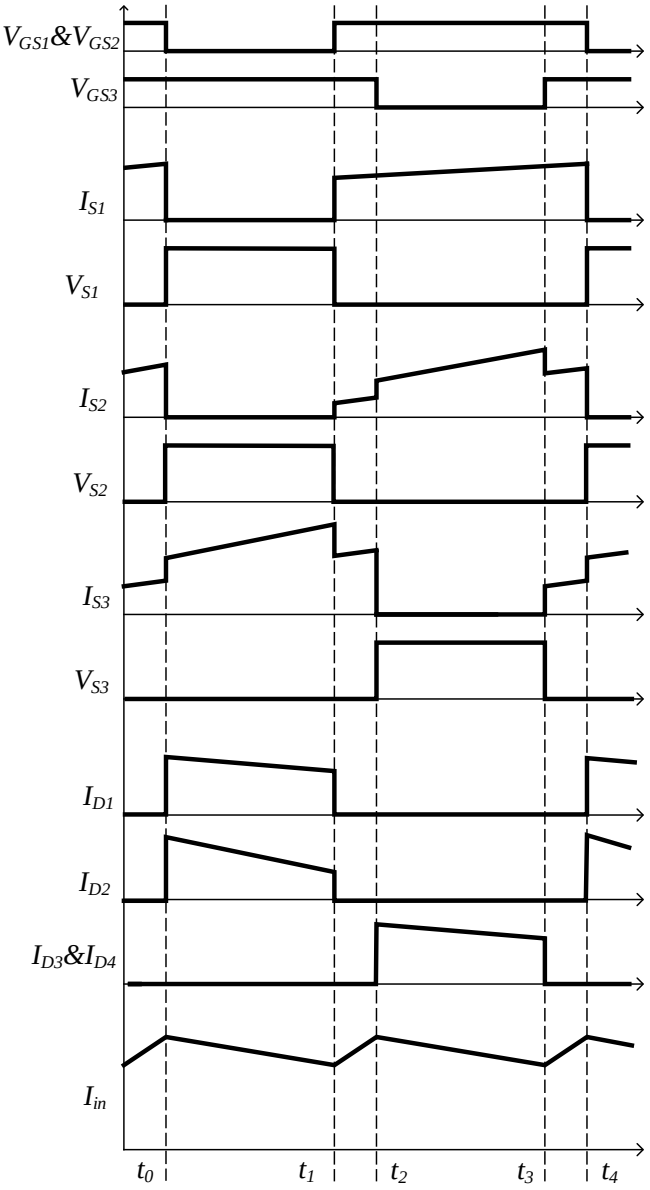

Fig. 2 Typical key waveforms of the proposed converter.

$$I_{L1}(t) = I_{L1}(t_1) + \frac{V_{in}}{L_1} \times (t - t_1) \tag{6}$$

$$I_{L2}(t) = I_{S2}(t) = I_{L2}(t_1) + \frac{V_{in}}{L_2} \times (t - t_1) \tag{7}$$

$$I_{L3}(t) = I_{L3}(t_1) + \frac{V_{in} + V_{C1}}{L_3} \times (t - t_1) \tag{8}$$

$$I_{S1}(t) = I_{L1}(t) + I_{L3}(t) \tag{9}$$

Interval III, [t_2-t_3]: At t_2, S_3 turns off and this interval begins. When S_3 turns off, L_3 continues its current and turns D_3 and D_4 on. Part of L_3 current flows through V_{in}-S_1-C_1-L_3-C_3-D_3-C_o and the other part of L_3 current runs through V_{in}-S_1-C_1-L_3-D_4-C_2-S_2. Hence, C_1 and C_3 are discharged and C_o and C_2 are charged in this interval. L_1 and L_2 are charged similar to the pervious interval. Important equations of the converter elements are:

$$I_{L1}(t) = I_{L1}(t_2) + \frac{V_{in}}{L_1} \times (t - t_2) \tag{10}$$

$$I_{L2}(t) = I_{L2}(t_2) + \frac{V_{in}}{L_2} \times (t - t_2) \tag{11}$$

$$I_{L3}(t) = I_{L3}(t_2) - \frac{V_o - V_{in} - V_{C1} - V_{C3}}{L_3} \times (t - t_2) \tag{12}$$

$$I_{S1}(t) = I_{L1}(t) + I_{L3}(t) \tag{13}$$

Interval IV, [t_3-t_4]: Fig. 3(b) shows the equivalent circuit of the converter in this interval. The converter operation and its important equations are similar to the second interval.

3. Converter Analysis and Design Considerations

3.1. Voltage Conversion Ratio

Following equations can be obtained from Volt-Second-Balance of L_1, L_2 and L_3, respectively.

$$V_{in}DT = (V_{C1} - V_{in})(1 - D)T \tag{14}$$

$$V_{in}DT = (V_{C3} - V_{C2} - V_{in})(1 - D)T \tag{15}$$

$$(V_{in} + V_{C1})(2D - 1)T + V_{in}(1 - D)T = (V_{C2} - V_{C1} - V_{in})(1 - D)T \tag{16}$$

From, (14), (15) and (16) following equations are obtained.

$$V_{in} = (1 - D)V_{C1} \tag{17}$$

$$V_{in} = (1 - D)(V_{C3} - V_{C2}) \tag{18}$$

$$V_{in} = (1 - D)V_{C2} - D.V_{C1} \tag{19}$$

From (17), (18) and (19), V_{C1}, V_{C2} and V_{C3} can be obtained as,

$$V_{C1} = \frac{V_{in}}{(1 - D)} \tag{20}$$

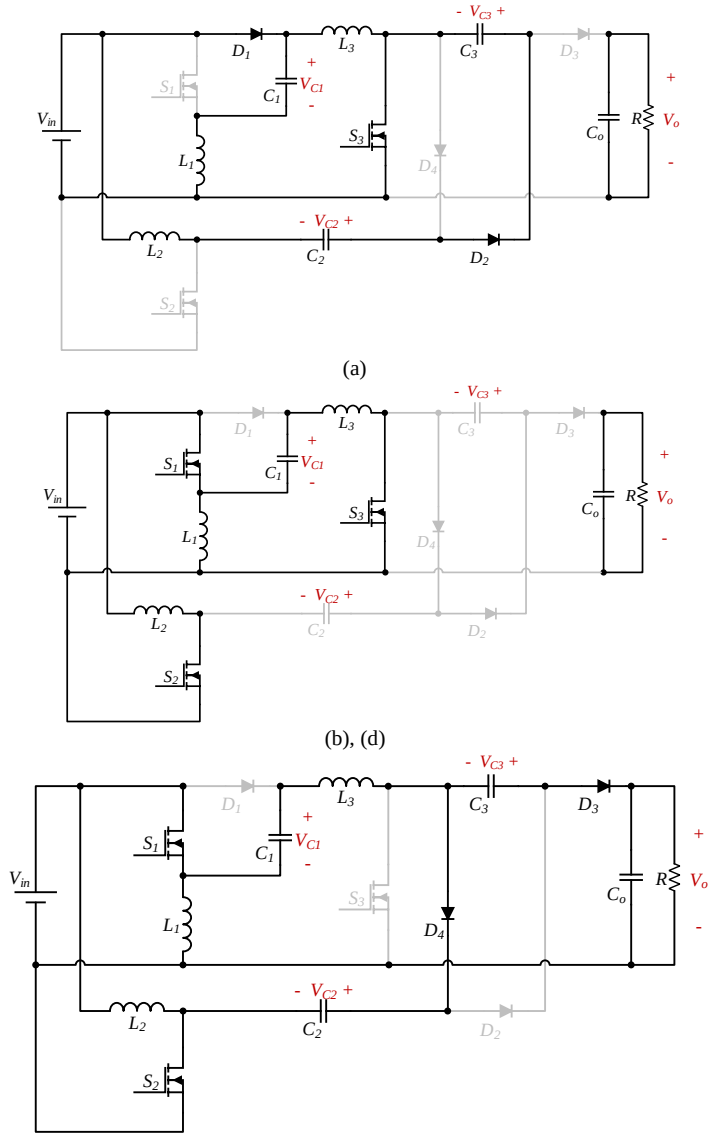

Fig. 3. Equivalent circuits of the proposed converterČ (a) Interval I [t_0-t_1], (b) Interval II [t_1-t_2], (c) Interval III [t_2-t_3] (d) Interval IV [t_3-t_4].

$$V_{C2} = \frac{V_{in}}{(1-D)^2} \tag{21}$$

$$V_{C3} = \frac{(2-D).V_{in}}{(1-D)^2} \tag{22}$$

From *Interval III*,

$$V_{C2} = V_o - V_{C3} \tag{23}$$

By substituting V_{C2} and V_{C3} from (21) and (22) in (23), the voltage gain G of the proposed converter can be obtained as follows:

$$G = \frac{V_o}{V_{in}} = \frac{3-D}{(1-D)^2} \tag{24}$$

Relation (24) shows that the proposed converter has a high step up voltage gain. Fig. 4 shows a comparison between the voltage gains of the proposed converter, the conventional cascade boost converter and the converters presented in [14] and [15]. As it can be observed from the figure, the proposed converter has a higher voltage gain.

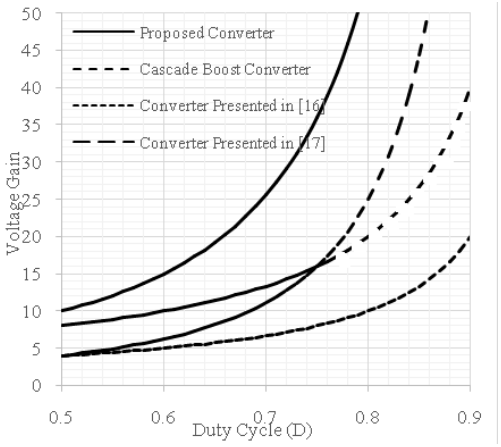

Fig. 4. Voltage gain comparison of the proposed converter with conventional cascade boost converter and the converters presented in [14] and [15].

3.2. Inductors average current

In the proposed converter, input current is sum of the L_1, L_2 and L_3 currents. Hence, the average value of input current is as follows:

$$I_{in\_avg} = I_{L1\_avg} + I_{L2\_avg} + I_{L3\_avg} \tag{25}$$

From the current-second-balance of C_3 and C_o, following equation can be obtained

$$\frac{I_{L2\_avg}}{2}(1-D)T = I_{L3\_avg}(1-D)T \tag{26}$$

$$I_{L3\_avg}(1-D)T = I_{o\_avg}T \tag{27}$$

From (26) and (27),

$$I_{L2\_avg} = 2I_{L3\_avg} \tag{28}$$

$$I_{L3\_avg} = \frac{I_{o\_avg}}{(1-D)} \tag{29}$$

The following equation can be obtained by assuming ideal condition:

$$P_{in} = I_{in\_avg}V_{in} = (I_{L1\_avg} + I_{L2\_avg} + I_{L3\_avg})V_{in} = P_o = I_{o\_avg}V_o \tag{30}$$

So,

$$(I_{L1\_avg} + I_{L2\_avg} + I_{L3\_avg}) = \frac{V_o}{V_{in}} I_{o\_avg} \tag{31}$$

By substituting I_{L2_avg},$I_{L3_avg}$and V_o/V_{in} from (28), (29) and (24) into (31), average current of inductors are:

$$I_{L1\_avg} = \frac{2DI_{o\_avg}}{(1-D)^2} = \frac{2D}{3-D} I_{in\_avg} \tag{32}$$

$$I_{L2\_avg} = \frac{2I_{o\_avg}}{1-D} = \frac{2(1-D)}{3-D} I_{in\_avg} \tag{33}$$

$$I_{L3\_avg} = \frac{I_{o\_avg}}{1-D} = \frac{(1-D)}{3-D} I_{in\_avg} \tag{34}$$

The proposed converter is compared with the conventional cascade boost and converters presented in [14] and [15] in Table 1. From this table, it is obvious that in the proposed converter, unlike the conventional cascade boost converter, the input current is shared between all the inductors.

4. SEMICONDUCTOR STRESS ANALYSIS

Based on the converter operating intervals and equivalent circuits, the voltage stress of S_1, S_2 and D_1 is:

$$\overline{V_{S1}} = \overline{V_{S2}} = \overline{V_{D1}} = \frac{V_{in}}{(1-D)} = \frac{(1-D)}{(3-D)}.V_o \tag{35}$$

Also, the voltage stresses of S_3, D_3, D_2 and D_4 are as follows:

$$\overline{V_{S3}} = \overline{V_{D3}} = \frac{V_{in}}{(1-D)^2} = \frac{V_o}{(3-D)} \tag{36}$$

$$\overline{V_{D2}} = \overline{V_{D4}} = \frac{(2-D).V_{in}}{(1-D)^2} = \frac{(2-D).V_o}{(3-D)} \tag{37}$$

The voltage stress of the semiconductor components in the proposed converter are compared with some other transformer-less high step up converters in Table 1 and as it can be seen, in the proposed converter the voltage stresses of the components are reduced.

When S_1 is on, the currents of L_1 and L_2 flow through this switch and when it turns off its current passes through D_1, hence the current stresses of S_1 and D_1 can be obtained as:

$$\overline{I_{S1}} = \overline{I_{D1}} = I_{L1\_avg} + I_{L2\_avg} + \frac{1}{2}\left(\frac{(V_{in} - V_{C1})(1-D).T}{L_1}\right) + \frac{1}{2}\left(\frac{(V_{in} + V_{C1})DT}{L_2}\right) \tag{38}$$

The current stresses of other switches and diodes are as follows:

$$\overline{I_{S2}} = I_{L3\_avg} + I_{L2\_avg} + \frac{1}{2}\left(\frac{(V_{in} + V_{C2} - V_{C3})(1-D)T}{L_3}\right) + \frac{1}{2}\left(\frac{(V_{in} + V_{C1})DT}{L_2}\right) \quad (39)$$

$$\overline{I_{S3}} = I_{L3\_avg} + \frac{1}{2}\left(\frac{V_{in}DT}{L_3}\right) + \frac{1}{2}\left[I_{L2\_avg} + \frac{1}{2}\left(\frac{(V_{in} + V_{C1} - V_{C2})(1-D)T}{L_2}\right)\right] \quad (40)$$

$$\overline{I_{D2}} = I_{L3\_avg} + \frac{1}{2}\left(\frac{V_{in}DT}{L_3}\right) \quad (41)$$

$$\overline{I_{D3}} = \overline{I_{D4}} = \frac{1}{2}\left[I_{L2\_avg} + \frac{1}{2}\left(\frac{(V_{in} + V_{C1})DT}{L_2}\right)\right] \quad (42)$$

Table 1 Comparison of the proposed converter with the conventional cascade boost converter and converters presented in [14] and [15].

Items	Conventional Cascade boost converter	Converter presented in [14]	Converter presented in [15]	Proposed Converter
Voltage Gain (V_o/V_{in})	$\frac{V_o}{V_{in}} = \frac{1}{(1-D)^2}$	$\frac{V_o}{V_{in}} = \frac{2}{1-D}$	$\frac{V_o}{V_{in}} = \frac{4}{1-D}$	$\frac{V_o}{V_{in}} = \frac{3-D}{(1-D)^2}$
Voltage Stress of Switches	$\overline{V_{S1}} = (1-D).V_o$ $\overline{V_{S2}} = V_o$	$\overline{V_{S1}} = \overline{V_{S2}} = \frac{1}{2}.V_o$	$\overline{V_{S1}} = \overline{V_{S2}} = \frac{1}{4}.V_o$	$\overline{V_{S1}} = \overline{V_{S2}} = \frac{(1-D)}{(3-D)}.V_o$ $\overline{V_{S3}} = \frac{1}{(3-D)}.V_o$
Voltage Stress of Diodes	$\overline{V_{D1}} = (1-D).V_o$ $\overline{V_{D2}} = V_o$	$\overline{V_{D1}} = \overline{V_{D2}} = \frac{1}{4}.V_o$ $\overline{V_{D3}} = \overline{V_{D4}} = V_o$	$\overline{V_{D1}} = \frac{1}{4}.V_o$ $\overline{V_{D2}} = \overline{V_{D3}} = \overline{V_{D4}} = \frac{1}{2}.V_o$	$\overline{V_{D1}} = \frac{(1-D)}{(3-D)}.V_o$ $\overline{V_{D2}} = \overline{V_{D4}} = \frac{(2-D).V_o}{(3-D)}$ $\overline{V_{D3}} = \frac{V_o}{(3-D)}$
Inductors average current	$I_{L1\_avg} = I_{in\_avg}$ $I_{L2\_avg} = (1-D).I_{in\_avg}$	$I_{L1\_avg} = \frac{1}{2}I_{in\_avg}$ $I_{L2\_avg} = \frac{1}{2}I_{in\_avg}$	$I_{L1\_avg} = \frac{1}{2}I_{in\_avg}$ $I_{L2\_avg} = \frac{1}{2}I_{in\_avg}$	$I_{L1\_avg} = \frac{2.D}{3-D}.I_{in\_avg}$ $I_{L2\_avg} = \frac{2.(1-D)}{3-D}.I_{in\_avg}$ $I_{L3\_avg} = \frac{(1-D)}{3-D}.I_{in\_avg}$

5. INPUT CURRENT RIPPLE AND INDUCTORS

From equations (6), (7) and (8), the input current ripple is obtained as follows:

$$\Delta I_{in} = \frac{V_{in} DT}{2L_1} + \frac{V_{in} DT}{2L_2} + \frac{(V_{in} + V_{C1} - V_{C2})DT}{2L_3} \tag{43}$$

By replacing V_{C1} and V_{C2} from (20) and (21) in (43):

$$\Delta I_{in} = \frac{V_{in} DT}{2L_1} + \frac{V_{in} DT}{2L_2} + \frac{(1 + \frac{1}{1-D} - \frac{1}{(1-D)^2})V_{in} DT}{2L_3} \tag{44}$$

By assuming $L = L_1 = L_2$,

$$\Delta I_{in} = \frac{V_{in} DT}{L} + \frac{(1 + \frac{1}{1-D} - \frac{1}{(1-D)^2})V_{in} DT}{2.L_3} = V_{in} DT(\frac{1}{L} + \frac{(1 + \frac{1}{1-D} - \frac{1}{(1-D)^2})}{2L_3}) \tag{45}$$

From (45), if

$$L_3 = \frac{1}{2}(\frac{D}{(1-D)^2} - 1)L \tag{46}$$

, the input current ripple of the converter would be zero. In the case that V_{in}=40Vand V_o=400V, the converter operating duty cycle from (24) is 0.5 and from (46),L_3 is

$$L_3 = \frac{1}{2}L \tag{47}$$

By substituting L_3 from (47) and V_{in} from (24) in (45), the input current ripple of the proposed converter is obtained as:

$$\Delta I_{in} = \frac{V_{in} DT}{L}(\frac{1}{(1-D)^2} - \frac{1}{1-D} - 2) \tag{48}$$

The equation of input current ripple in the conventional cascade converter is:

$$\Delta I_{in} = \frac{V_{in} DT}{2L} \tag{49}$$

Comparing (48) with (49) shows that the proposed converter has a lower input current ripple in comparison to conventional cascade boost converter. The proposed converter operates under continuous current mode (CCM) and the design equation of L_1, L_2 and can be obtained from (30) and (31) as:

$$L_1 = L_2 = \frac{(1-D)^4 TR_{o\_\min}}{4(3-D)} \tag{50}$$

$$L_3 = \frac{1}{2}(\frac{D}{(1-D)^2} - 1)L_1 \tag{51}$$

6.CAPACITORS

The values of the proposed converter capacitors can be obtained from following equations:

$$C_1 = \frac{2DTI_{o\_avg}}{(1-D)\Delta V_{C1}} \tag{52}$$

$$C_2 = \frac{TI_{o\_avg}}{2\Delta V_{C2}} \tag{53}$$

$$C_3 = \frac{2TI_{o\_avg}}{\Delta V_{C3}} \tag{54}$$

$$C_o = \frac{TI_{o\_avg}}{2\Delta V_o} \tag{55}$$

Where, ΔV_{C1}, ΔV_{C2}, ΔV_{C2} and ΔV_{Co} are the voltage ripple of C_1, C_2, C_3 and C_o, respectively.

7. EXPERIMENTAL RESULTS

In order to verify the performance of the proposed converter and the presented key waveforms, a 200 W laboratory prototype is implemented. The component specifications of the proposed converter are summarized in Table2.In order to show the ability of providing high voltage gain, input voltage and output voltages are selected 40V and 400 V, respectively. The switching frequency and duty ratio of the gate signals of all switches are 100 kHz and approximately 0.5, respectively. The experimental waveforms of the converter are shown in Fig. 5. In Fig. 5(a), (b) and (c) the current and voltage waveforms of S_1, S_2 and S_3 are represented, respectively. As shown in the figures, the maximum voltage across S_1, S_2 and $S_3$for 40V input and 400V output are about 80V, 80V and 160V, respectively. As a result, low voltage rated switches can be adopted to reduce the conduction loss and to achieve high efficiency. In Fig. 5(d), (e), (g) and (h) the current and voltage of D_1, D_2, D_3 and $D_4$are illustrated, respectively. The voltage stress of D_1, D_2, D_3 and $D_4$for 400V output voltage is about 80V, 250V, 160V and 250V, respectively. As can be seen, the voltage stresses of diodes are sufficiently lower than the output voltage.

Fig. 6 shows the measured efficiency of the proposed converter compared with the conventional cascade converter. For a fair comparison, the conventional cascade boost converter is designed with the same switching frequency. Other important parameter of the conventional cascade boost converter is mentioned in Table 2. As it can be observed form Fig. 6, the proposed converter has higher efficiency and as the load increases, efficiency drop in the conventional converter is higher compared with the proposed converter. Fig. 7 shows the input and output voltages of the converter.

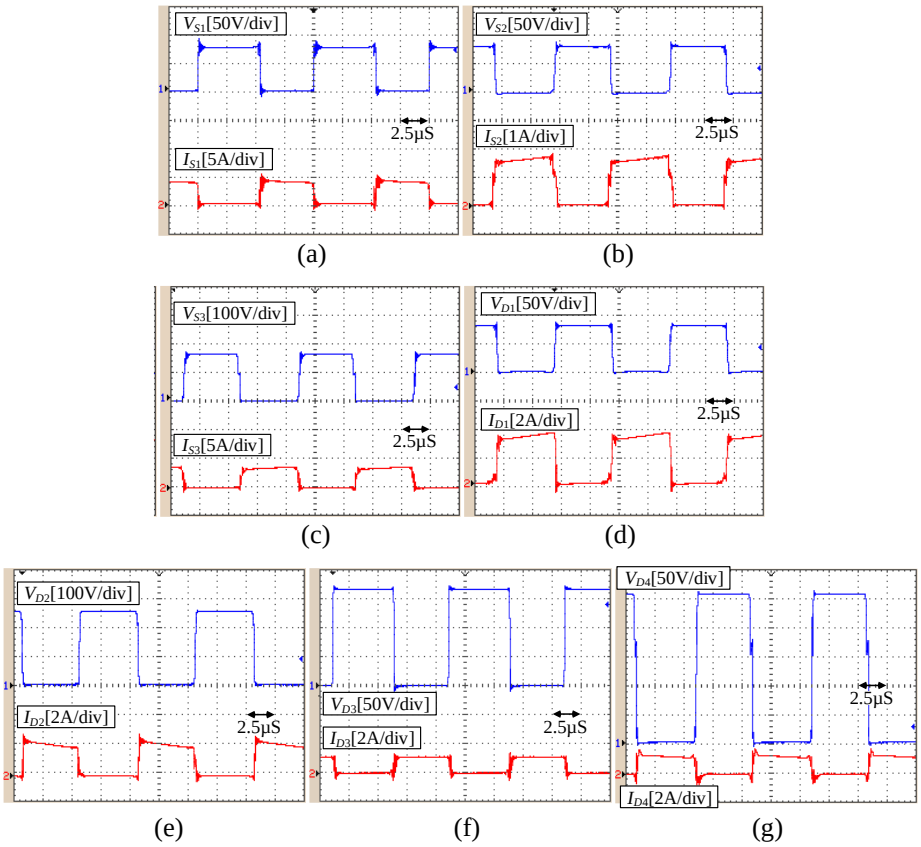

Fig. 5. Experimental voltage and current waveforms of the proposed converter semiconductor components (a) S_1, (b) S_2, (c) S_3, (d) D_1, (e) D_2, (f) D_3 and (g) D_4.

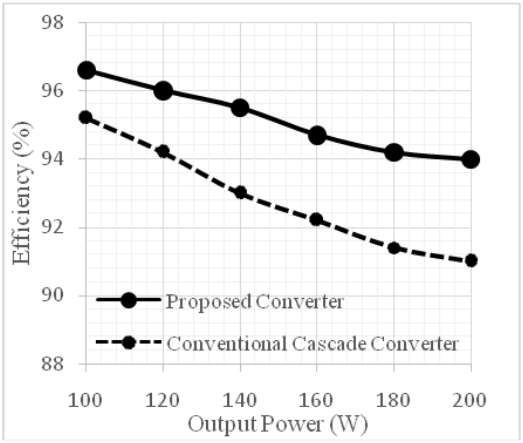

Fig. 6 Measured efficiency of the proposed converter.

Table 2 Components value and specification of the implemented converters

Parameter	Value	
	Proposed Converter	Conventional Cascade Converter
Switching frequency	100 kHz	100 kHz
Switches	S_1~S_3 (IRF640)	S_1 (IRFP260) S_2(IRFP460)
Diodes	D_1~D_4 (MUR460)	D_1 (BYV32-200) D_2 (MUR460)
Inductors	L_1 and L_2 (500 µH) L_3(250 µH)	L_1 (1mH) L_2(500 µH)
Capacitors	C_1 (10µF/ 100V) C_2 (10µF/ 200V) C_3 (10µF/ 450V) C_o(47µF/ 450V)	C_1 (22µF/ 200V) C_o(100µF/ 450V)

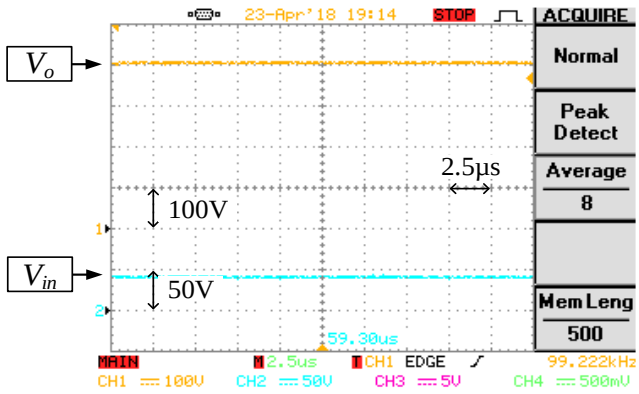

Fig. 7 Input and output voltage waveforms of the sample converter

8.CONCLUSIONS

A new interleaved cascade boost DC–DC converter with an improved voltage gain is presented in this paper. In the proposed converter, the input current is continuous with low ripple and the converter does not need additional filter in the input. Besides, unlike the conventional cascade boost converter, the input current is shared between all the inductors and hence the proposed converter can be implemented with lower current rated inductors. Moreover, the voltage stress of the converter power devices is reduced in comparison with conventional cascade boost converters and the converters presented in [14] and [15]. Thus, the efficiency of the converter is improved.

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