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Original scientific paper

INFLUENCE OF OXIDE THICKNESS VARIATION ON ANALOG AND RF PERFORMANCES OF SOI FINFET

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Abstract. *This paper focuses on the impact of variation in the thickness of the oxide (SiO_2) layer on the performance parameters of a FinFET analysed by varying the oxide layer thickness in the range of 0.8nm to 3nm. While varying the oxide layer thickness, the overall width of the FinFET is fixed at a value 30nm, and the FinFET parameters are analysed for structures with different oxide layer thickness. The parameters like drain current, transconductance, transconductance generation factor, parasitic capacitances, output conductance, cut-off frequency, maximum frequency, GBW, energy and power consumption are calculated to study the influence of FinFET oxide (SiO_2) layer thickness variation. It is detected from the result and analysis that the drain current, transconductance, transconductance generation factor, gain bandwidth and output conductance improve with decrement in oxide layer thickness whereas, the parasitic capacitances, cut-off frequency and maximum frequency degrade when there is a reduction in oxide (SiO_2) layer thickness. The parameters like energy and consumed power of FinFET get better when the oxide (SiO_2) layer thickness increases.*

Key words: *FinFET, oxide layer thickness, transconductance generation factor, maximum frequency*

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INTRODUCTION

The demand of highly compact and denser ICs have created the interest amongst the researchers to downscale the regular silicon MOS field effect transistor, which results in the evolution of compact ICs but, as a consequence Short-Channel Effects (SCE) are developed in the device which degrades the device parameters immensely. So, multiple gate-based devices are considered a solution to continue downscaling. These devices possess improved controllability over lower leakage currents, SCEs and better yield. The performance can also be improved by varying the thickness of the oxide layer [1-5]. FinFET is one of the evolutionary techniques for application based less-power consuming circuits as it displays commendable performance to nullify the short-channel problems due to the fact that multiple gates are monitoring a single channel [6-11].

Fin type silicon on insulator-based field effect transistor is the newly evolved technology which is presently used in ICs. FinFETs encompass a triple-gate construction to suppress the major performance problems, such as the SCEs. The silicon on insulator (SOI) technique insulates the internal active area from the lower part of the substrates, which internally reduces the leakage current, parasitic capacitance, and the power dissipation of Circuits. Hence, SOI based FinFETs are the center of attraction nowadays**.** Detailed studies of SOI based FinFETs are presented in [12-18].

Constructing tri-gate FinFETs different approaches has been followed in recent years like SOI based FinFETs, bulk FinFET [6-18]. The inverted-T structure FinFET [19] is also designed which provides better drain current compared to the SOI based FinFET. A multi-level logic design concept is adopted in place of complex gates to reduce the process variability and radiation effects. But it is very important to study the impact of the oxide layer thickness on the performance of the device. The oxide layer thickness variation is studied in [1], where the thickness is varied from 3 nm to 10 nm. But, in general the thickness of the oxide layer should not exceed 3nm for a FinFET of channel length 30nm.

Here, the 3-dimensional construction of FinFET is analyzed by altering the oxide layer (SiO_2) thickness, keeping the total dimension of the FinFET fixed. To realize the physical mechanism of the device, various performance parameters are evaluated based on the mathematical expressions and finally simulated to get a comparative analysis.

In section II the theory is explained. The result and discussion are presented in Section III. Section IV summarizes the total work done in the paper.

DEVICE STRUCTURE AND SIMULATION SETUP

The core of the FinFET i.e. the fin, is placed vertically making an angle of 90º to the FinFET body and is responsible for the flow of current. Gate material with higher work function covers the silicon fin from three sides to reduce the SCEs by increasing the control over the device [20].

The 3-dimensional cross-sectional view of the SOI-based FinFET structure is represented in Fig. 1. Here the oxide (SiO_2) layer placed between the fin and the gate is the central point of the discussion. As mentioned in the Table 1, the thickness of this layer is varied from 0.8nm to 3nm, keeping the total dimension of the FinFET as a constant, i.e. 30nm. The fin height and width are taken to be 20nm and 10nm with a channel length of 30nm. The length of the device is kept as 110nm which is shown in Table 1.

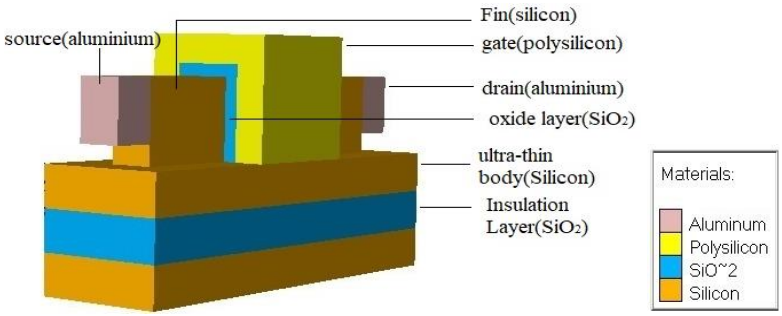

Fig. 1 A 3d cross-sectional view of the SOI-based FinFET

Table 1 Device Specifications of FinFET

Parameters	Measurements
Channel Length	30 nm
Fin Height	20 nm
Fin Width	10 nm
Fin Angle	90º
Equivalent Oxide Thickness	0.8 nm - 3 nm
Ultra-thin Body Thickness	10 nm
Total Device Length	110 nm
Total Device Width	30 nm

The simulation process was carried out using the standard TCAD simulation tool Silvaco ATLAS (2016). To achieve better accuracy, the 3D quantum transport equations and the drift-diffusion equations are included. The Bohm Quantum Potential (BQP) model is used for the simulation process in order to take care of the quantum effect produced in the nano scale devices. To account for the leakage currents that occur due to thermal generation process, the Auger recombination/generation and Shockley–Read–Hall (SRH) model are used. For junctionless transistors, Quantum confinement effect is not significant, so it is not considered. Gummel-Newton method is used for mathematical calculations in this study. During the whole simulation process the temperature is set at 300K. The calibration of the simulation model has been performed with the published experimental data [21] and is represented in Fig. 2.

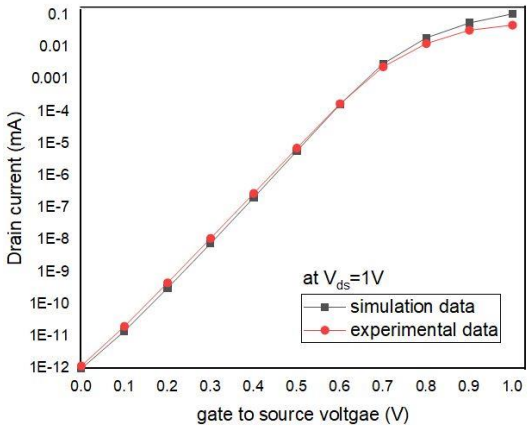

Fig. 2 The calibration of the I_D–V_{GS} characteristics of the FinFET against experimental data [22]

RESULTS AND DISCUSSION

To investigate the effect of oxide (SiO_2) layer thickness, the Silicon dioxide (SiO_2) material thickness was altered in the range of 0.8 nm to 3 nm, while preserving the overall dimension of the FinFET static at 30 nm. To perceive the influence of the oxide layer thickness on numerous vital performance parameters like drain current, transconductance, transconductance generation factor, parasitic capacitances, cut-off frequency, maximum frequency, gain bandwidth, energy and power consumption [22-24], etc., SOI FinFETs were simulated and investigated for structures with different oxide layer thickness.

The drain current of a device is the major parameter to be observed. The circuit is said to be more desirable if it produces more drain current for a specific gate voltage. In Fig. 3 the drain current vs gate to source voltage curve is plotted for FinFETs with variation in SiO_2 layer thickness and it can be observed from the graph that the drain current increases for lesser oxide layer thickness. By decreasing the SiO_2 thickness, the oxide capacitance (C_{ox}) enhances, which internally rises the drain current as it is directly proportional to the C_{ox}.

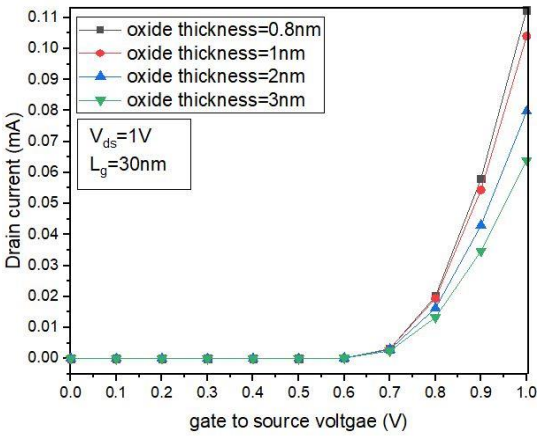

Fig. 3 $I_D \sim V_{GS}$ curve with varying oxide layer thickness

For operations at higher frequencies, the transconductance (g_m) plays a dynamic part as it implies the exaggeration capability of the FinFET. It is mathematically denoted as [25]

$$g_m = \partial I_D / \partial V_{GS} \tag{1}$$

Fig. 4 shows the $g_m \sim V_{GS}$ curve for the FinFETs with different SiO_2 layer thickness, which displays that the lower value of oxide layer thickness provides better transconductance value. This happens due to the fact that the transconductance is proportional to drain current, and the drain current is increasing with reduction in oxide layer thickness.

To analyze the impact of both transconductance and drain current on the device, the transconductance generation factor needs to be examined. The transconductance generation factor is defined as the ratio of the transconductance to the drain current and mathematically defined as [25]

$$TGF = g_m / I_D \tag{2}$$

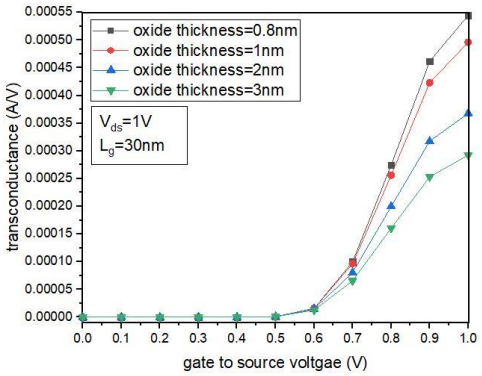

Fig. 4 $g_m \sim V_{GS}$ curve with varying oxide layer thickness

Fig. 5 shows the TGF ~ V_{GS} curve for the FinFETs with different SiO_2 layer thickness, which displays that the lower value of oxide layer thickness provides better transconductance generation factor value.

The next parameter which should be analyzed is the output conductance (g_{ds}) which determines the overall gain of the device. The $g_{ds} \sim V_{GS}$ curve is plotted in Fig. 6 by varying the SiO_2 layer thickness from 0.8 nm to 3 nm and it is clear from the graphical analysis that the structure with lesser oxide layer thickness possesses maximum output conductance. The output conductance is proportional to the rate of change in drain current. As the drain current increases for device with lower oxide thickness, the output conductance also increases when the thickness of the oxide layer reduces.

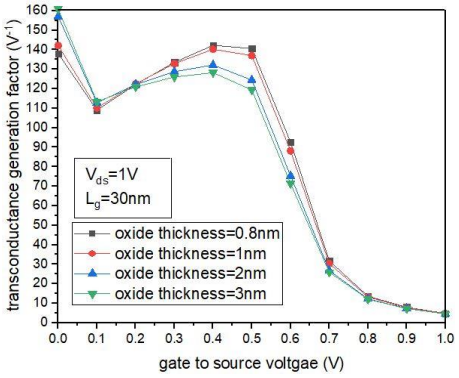

Fig. 5 TGF ~ V_{GS} curve with varying oxide layer thickness

The parasitic capacitances play a vital role in the radiofrequency (RF) performances of any device. The different parasitic capacitances are plotted in Fig. 6. The $C_{gd} \sim V_{GS}$, $C_{gs} \sim V_{GS}$ and $C_{gg} \sim V_{GS}$ curves are shown in Fig.7(a), Fig.7(b) and Fig.7(c) respectively. In each case the thickness of the SiO_2 layer is altered in the range of 0.8nm to 3nm and the behavior of each structure is analyzed. It is found in all cases that the parasitic capacitance values get reduced for increase in oxide layer thickness. The dependency of parasitic capacitances, i.e. gate-to-drain capacitance, gate-to-source capacitance and gate-to-gate

capacitance on the variation of SiO_2 layer thickness is displayed in Fig. 7(d). It is observed that the parasitic capacitance values get better due to increase in oxide layer thickness.

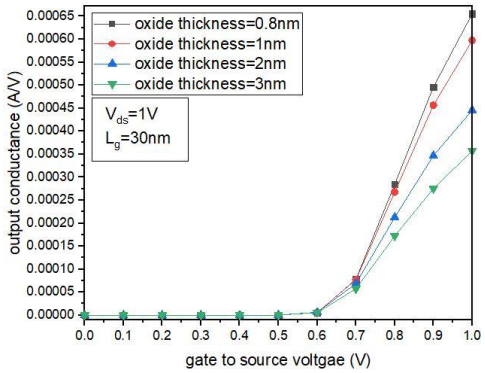

Fig. 6 g_{ds} ~ V_{GS} curve with varying oxide layer thickness

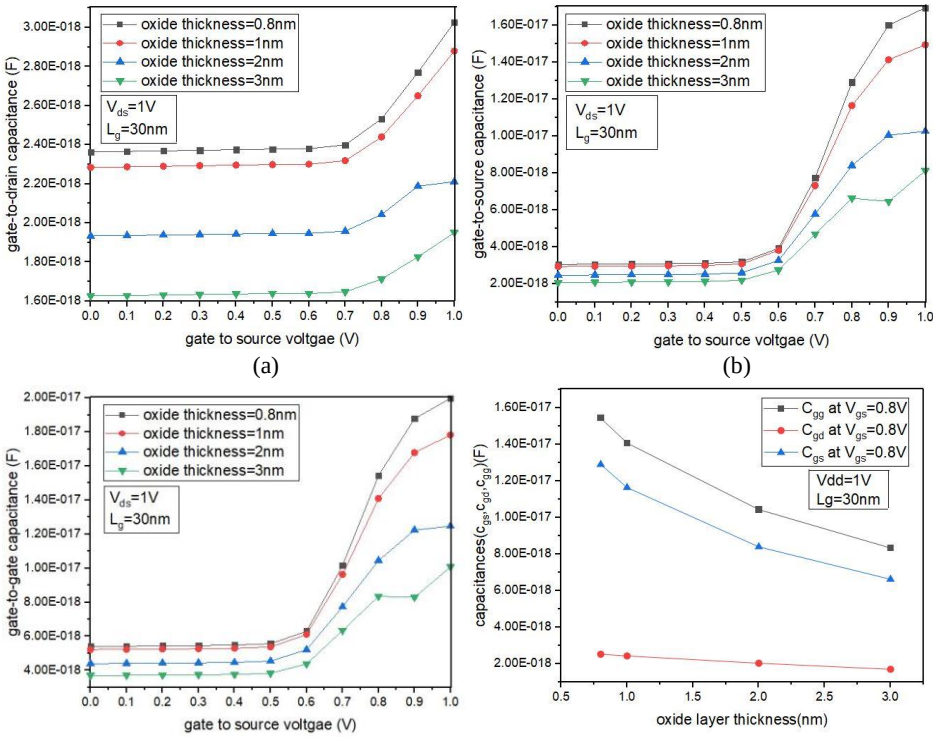

Fig. 7 (a) C_{gd} ~ V_{GS} curve with varying oxide layer thickness; (b) C_{gs} ~ V_{GS} curve with varying oxide layer thickness; (c) C_{gg} ~ V_{GS} curve with varying oxide layer thickness; (d) capacitance ~oxide layer thickness curve at V_{GS}=0.8V

The cutoff frequency (f_T) is treated as the most important component to be studied when it comes to RF applications. It is the frequency value for which the device attains the current gain value as '1' and is denoted as [11]

$$f_T = g_m / (2*pi*C_{gg}) \quad \text{and } C_{gg} = C_{gd} + C_{gs,} \tag{3}$$

where C_{gd} and C_{gs} are the gate to source and gate to drain capacitances respectively.

The cut-off frequency ~V_{GS} curve is analyzed in Fig. 8 by varying the SiO_2 thickness ranging from 0.8 nm to 3 nm and it is observed that, the device with higher oxide layer thickness achieves better cutoff frequency. From equation (3) it is clear that the cutoff frequency is inversely proportional to the capacitance which increases for lower oxide layer thickness. So, the device with lower values of oxide layer thickness possesses lesser cutoff frequency compared to the device with higher oxide layer thickness.

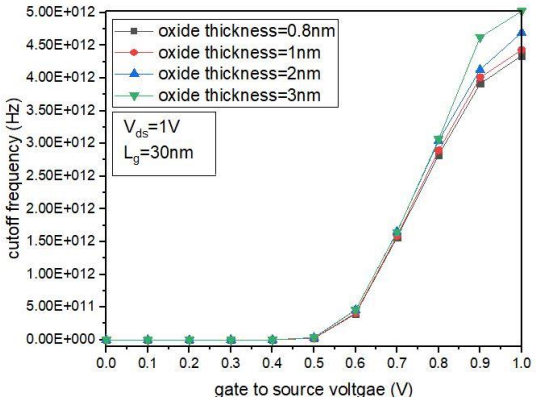

Fig. 8 f_T ~ V_{GS} curve with varying oxide layer thickness

The maximum frequency of a device is defined as the frequency at which the power gain becomes unity. It is mathematically defined as [11]

$$f_{max}=g_m / (2*pi*C_{gs}*(\sqrt{(4*(R_s+R_i+R_g)*(g_{ds}+g_m*(C_{gd}/C_{gs}))))}) \tag{4}$$

where Rg, Rs, and Ri are the gate, source and channel resistances respectively [26].

The dependency of the maximum frequency on the oxide layer thickness variation is analyzed through Fig. 8. The f_{max} ~ V_{GS} curve is represented in Fig.9 where the maximum frequency of structures with varying SiO_2 thickness is analyzed and it is found that the maximum frequency improves with rise in oxide layer thickness. From equation (4) it is clear that the maximum frequency is inversely proportional to the parasitic capacitance which increases for lower values of oxide layer thickness. So, the device with lower values of oxide layer thickness possesses lesser maximum frequency compared to the device with higher oxide layer thickness.

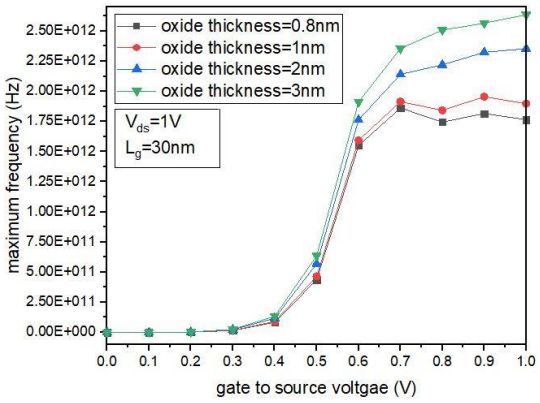

Fig. 9 f_{max} ~ V_{GS} curve with varying oxide layer thickness

The trade-off between gain and bandwidth is calculated by Gain Bandwidth Product (GBW) [27,28]. For semiconductor devices it is defined as

$$GBW = g_m / (20*pi* C_{gd}) \quad (5)$$

GBW ~ V_{GS} curve is represented in Fig. 10 with variation in SiO_2 thickness. It is observed from the graph that the gain bandwidth is reduced with the rise in thickness of the oxide layer. From equation (5) it is clear that the gain bandwidth is inversely proportional to the gate to drain capacitance and directly proportional to transconductance. The transconductance being the more dominant parameter helps to improve the gain bandwidth for device with lower value of oxide layer thickness.

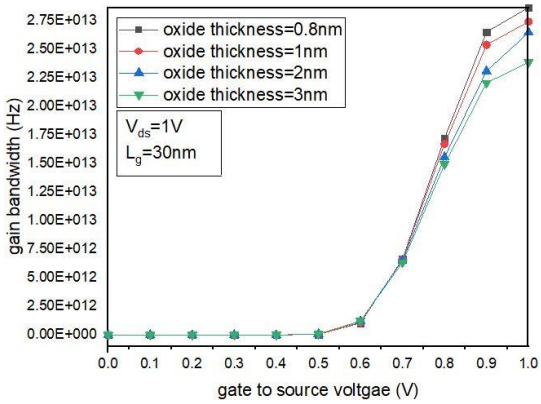

Fig. 10 GBW ~ V_{GS} curve with varying oxide layer thickness

Along with the above discussed analog and RF performance parameters the two major parameters i.e., energy and total power consumption also need to be studied from the application point of view. Hence, the below discussion will give a clear view of the above said parameters.

The energy ~ V_{GS} curve for structures with different oxide layer thickness is displayed in Fig.11. It is quite understandable from the two graphs that the energy gets better for higher oxide layer thickness. This happens due to the fact that the energy (CV^2) is mainly dependent on the capacitance as the supply voltage is fixed and previously it is already discussed that the capacitive effects get reduced for higher oxide layer thickness which improves the energy of the device.

The power consumption of any device is proportional to its energy. Hence, the power consumption also gets better for the structures with higher oxide layer thickness which is shown in Fig.12. Power ~ V_{GS} curve is shown in Fig. 12 with variation in SiO_2 thickness and power ~ oxide thickness is analyzed in Fig. 12(b) at constant. It is detected that the FinFET consumes more power for lesser oxide layer thickness.

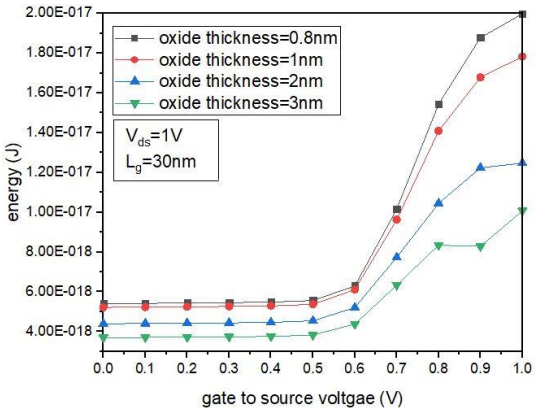

Fig. 11 energy ~ V_{GS} curve with varying oxide layer thickness

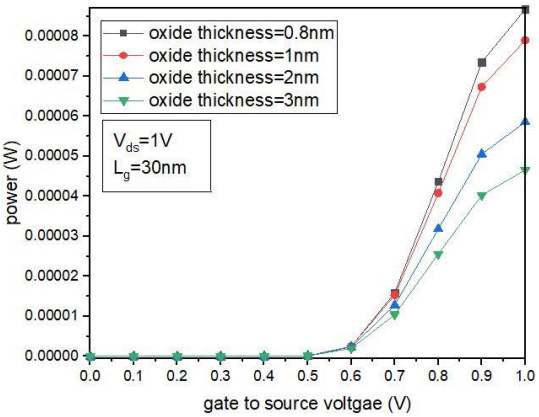

Fig. 12 power ~ V_{GS} curve with varying oxide layer thickness

CONCLUSION

In this paper, the basic FinFET structure has been analysed by varying the oxide layer thickness while maintaining the total dimension of the FinFET a constant. Different analog and radio frequency performance parameters of the device like the drain current, transconductance, transconductance generation factor, parasitic capacitances, output conductance, cut-off frequency, maximum frequency, gain bandwidth product, energy and power consumption are determined. From the analysis it is observed that the drain current, transconductance, transconductance generation factor, gain bandwidth and output conductance degrade with increase in oxide layer thickness. Whereas the parasitic capacitances get better when the oxide layer thickness rises, due to which the cut-off frequency and maximum frequency improves at higher oxide layer thickness. Hence, it can be concluded that the increase in oxide layer thickness improves the radio frequency parameters whereas it degrades the analog parameters. Finally, the parameters like the energy and power dissipation of FinFET are determined by varying the SiO_2 thickness and it is concluded that these parameters improve with rise in SiO_2 thickness.

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