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REALIZATION OF A VARIABLE RESOLUTION MODIFIED SEMIFLASH ADC BASED ON BIT SEGMENTATION SCHEME

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Abstract. *A modified variable resolution semiflash ADC, based on 'bit segmentation scheme', is presented. Its speed and comparator count are identical to a normal flash ADC. An 8-bit ADC has 256 different bit combinations. Sixteen consecutive bit combinations from the MSB side – beginning with the first one, remain unaltered for such an ADC. It continues this way till the last group of sixteen bits. In the designed circuit, the four MSB and four LSB bits are determined in the first and second part of the clock. Following the same logic, the bits in a 16-bit ADC can be found out in only two clock cycles by employing only fifteen comparators. It implies that a higher resolution ADC can easily be determined with low power and small die area. It is tested in P-SIM Professional 9 for an 8-bit ADC and curves drawn to establish the validity of the proposal.*

Key words: *Bit segmentation scheme (BSS), bit swap logic (BSL), least significant bit (LSB), semiflash ADC, half flash ADC, modified full flash ADC (MFFADC)*

1.INTRODUCTION

Different types of ADC architectures are used to meet various application needs like resolution, accuracy and faster operation. A flash or parallel ADC is fastest among the various types of ADCs available in the market. Comparator count for a Flash ADC increases exponentially with resolution. This limits the use of flash ADCs to 8-bit resolution. Over the years, researchers have designed various versions of flash ADCs like half flash, semi flash, simplified half flash, multi-step flash etc. These different types have their own advantages and disadvantages compared to a flash or full flash ADC.

A modified 8-bit semiflash ADC, using only fifteen comparators, is reported in [1] whose speed is same as that of a full flash ADC. Since only fifteen comparators are

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required, its power and die area requirement are thus significantly reduced. In [2], [3] hybrid flash-hybrid ADC architectures were used. In the former, a sampling switch was used to get reduced settling time for DAC and parallel capacitors used to reduce high frequency noise jitters while in the case of the latter, a segmented split capacitor charge redistribution DAC was employed to achieve less area and power and higher speed. A two-step 8-bit flash ADC and an 8-bit semiflash ADC, both of which used 15 comparators and a charge redistribution technique, were reported in [4], [5]. A bit swap logic (BSL) based bubble error correction (BEC) technique was applied in [6], while in [7] flash ADC performance was evaluated in presence of offset using hot code generator and bit swap logic (BSL).In [8], an encoder with reduced power was used for threshold inverter quantization based flash ADC. A statistically-driven two-step flash sub-ADC was constructed [9] having applications in high-speed time-interleaved ADCs in wire line communications. In [10], 8-bit and 10-bit ADCs were designed using fewer number of comparators and resistors which resulted in less area and power consumption. In [11], [12] a low power 4-bit flash ADC and a 9-bit two step flash ADC were respectively realized using standard cells. In [13], a flash ADC was used which increased the input dynamic range of ADC by using 5-input logic gates. A simplified half flash ADC, having the same speed as that of a flash ADC was designed in [14], but with reduced comparator count and less die area. A two-step flash ADC was reported in [15] which can be used in communication fields. OTA based comparators were used to realize a 3-bit high speed flash ADC [16] having applications in wireless LAN. Active data and clock distribution trees [17] were used to realize a 4-bit flash ADC. Bubble errors were taken care of in [18] by using a low power Wallace tree encoder for flash ADCs. A low power fault resistant flash ADC which finds applications in instrumentation fields was reported in [19]. A 6-bit low power flash ADC was reported in [20] which used an online offset cancellation technique.

2. PREVIOUS ARCHITECTURES

Relationship between resolution and number of comparators for a flash ADC [10], [14] is given by

$$N_c(N) = 2^N - 1 \tag{1}$$

From (1), it is evident that number of comparators increases exponentially [10] with increase in resolution.

A two-step or half flash [4,9] ADC accomplishes the bits in two clock cycles. For a half flash ADC, comparator count and resolution carries the following relationship.

$$N_c(N) = 2.2^{N/2} - 2 \tag{2}$$

A semiflash ADC [5] is very simple in nature which consumes less power and die area. An 8-bit semiflash ADC uses only 15 comparators for both fine and coarse conversions leading to a drastic reduction in the number of comparators used. Number of comparators for a semiflash ADC follows the relationship [5]

$$N_c(N) = 2^{N/2} - 1 \tag{3}$$

A simplified half flash ADC [14] employs a voltage estimator (VE) and a modified full flash ADC (MFFADC). Its requirement of power and die area are very small and has a

speed almost thrice that of a normal half flash ADC. Requirement of the number of comparators for a simplified half flash ADC bears the following relationship [14]

$$N_c(N) = 2^{(N/2-2)} + 2 \tag{4}$$

Speed of a multistep 10-bit ADC [10] is identical to a conventional half flash ADC. Its die area and power needs are low due to small number of comparators required. Number of comparators needed in case of [10] bears the relationship.

$$N_c(N) = 2^{(\frac{N}{2}-1)} \tag{5}$$

3. The Bit Segmentation Scheme (BSS)

A normal flash or full flash ADC, as it is called, has an exponential relationship between the number of comparators used and the resolution. Thus, with increasing resolution, number of comparators needed for such an ADC becomes unmanageable. For instance, for a 16-bit flash ADC, number of comparators needed is 2^16 - 1 = 65535. In the present case, a modified 8-bit semiflash ADC is presented which is based on BSS.

The designed modified 8-bit semiflash ADC determines the 8 bits in a single clock. It implies that its speed is same as that of a normal flash ADC. A look at the bit combinations of an 8-bit flash ADC shows that it has 256 bit combinations. The combinations are segregated into sixteen fields as shown in Fig .1. It is observed from the figure that the four MSB bits in each field are same. As an example, in field 2 of the figure, the four MSB bits 0001 remain unchanged. The designed circuit identifies this 4 MSB bits in the first half of the clock cycle, i.e., during this time the particular field in which the unknown analog signal belongs, is identified. The rest four bits (LSB bits) in the field is determined in the second half of the clock cycle. Thus, for the designed circuit, all the 8-bits are determined in a single clock – implying that its speed is identical to a normal flash ADC. Also, it will be seen only fifteen comparators would be required to evaluate the 8-bits.

By the same logic, a 16-bit ADC of identical architecture would require only two clock cycles, but number of comparators needed for evaluation of the 16 bits would still remain at 15. Thus, savings in the number of comparators would be 65535/15 = 4369 times compared to a normal flash ADC. Thus, both power and die area would be drastically reduced.

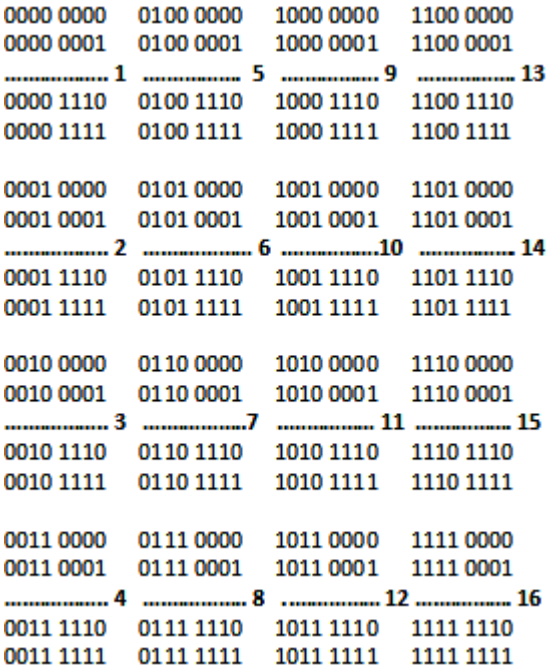


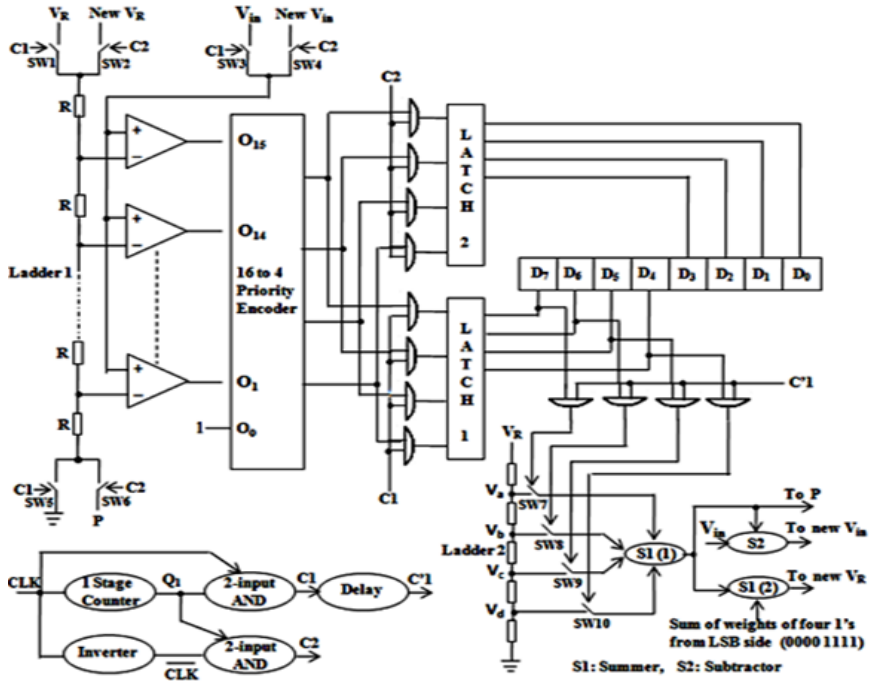
Fig. 1 The sixteen fields for an 8-bit ADC

4. REALIZINGTHE MODIFIED 8-BITSEMIFLASH ADC BASED ONBSS

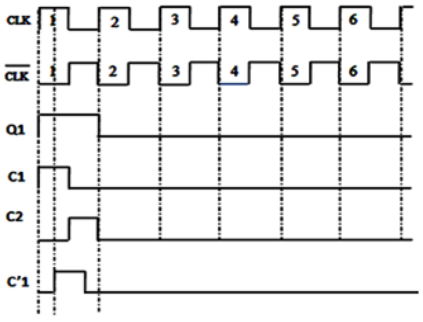
Fig. 2a) below shows the details of the designed modified 8-bit semiflash ADC while Fig. 2b) shows its timing diagram. The explanation of the designed circuit is given below.

The bottom left part of Fig. 2a) shows the manner of generation of pulses C1, C2 and C^11. C1, C2 remain active during first and second half of the clock, while C^11 is a delayed version of C1.

V_R and V_{in} are respectively the reference voltage and unknown analog input voltage applied during the first half of the clock, while during the second half of the clock, they are replaced by 'New V_R' and 'New V_{in}'. Also, during the second half of the clock, the bottom of the ladder is fed with a voltage available at point 'P' shown in Fig. 2a). This voltage represents the voltage value of the four MSB bits corresponding to the particular field detected during first half of the clock.



(a)



(b)

Fig. 2 a) Realization of a modified 8-bit semiflash ADC b) Timing diagram for realization of different pulses

During the first half of the clock, pulse C1 makes sure that the switches SW1, SW3 and SW5 remain in the closed condition. The positive inputs of the fifteen comparators are all connected to V_{in} while their negative inputs are connected to voltages from the ladder as shown in the figure. The fifteen outputs O_{15}-O_1 from the comparators along with O_0 (which is always 1) are fed to a 16-to-4 priority encoder. Its four outputs are connected to two sets of AND gates. A set of four AND gates are controlled by C1 while the other set by C2. During the first half of the clock, since C1 is active, thus encoder outputs are latched by latch1. These four bits are stored in the 1-byte register as D7-D4 bits. They are also ANDed with C`1 pulse. Outputs of ANDing operation act as control inputs to switches SW7-SW10. The inputs to SW7-SW10 are respectively connected to D7-D4 bits, represented by V_a, V_b, V_c and V_d as shown in the figure. The outputs of switches act as inputs to the summer S1(1). Output of summer S1(1) is a representation of the sum of weights of the four bits from the MSB side of the input analog signal. For example, if during C1, the output from the priority encoder is 1011, the output of summer S1(1) will represent a value equal to 1011. Summer S1(2) sums the output of S1(1) with 0000 1111. Thus, summer S1(2) output will correspond to the highest value within the field to which the analog signal belongs. This acts as the 'new V_R', which would become effective from the beginning of C2. S2 is a subtractor that subtracts S1(1) from the original V_{in}. The subtracted result acts as the 'new V_{in}' value.

At the beginning of C2, switches SW2, SW4 and SW6 become active. Thus, during this time, 'New V_R' and 'New V_{in}' come into the circuit by replacing V_R and V_{in} respectively. The top of the ladder is fed with a voltage which represents the highest value of the analog signal

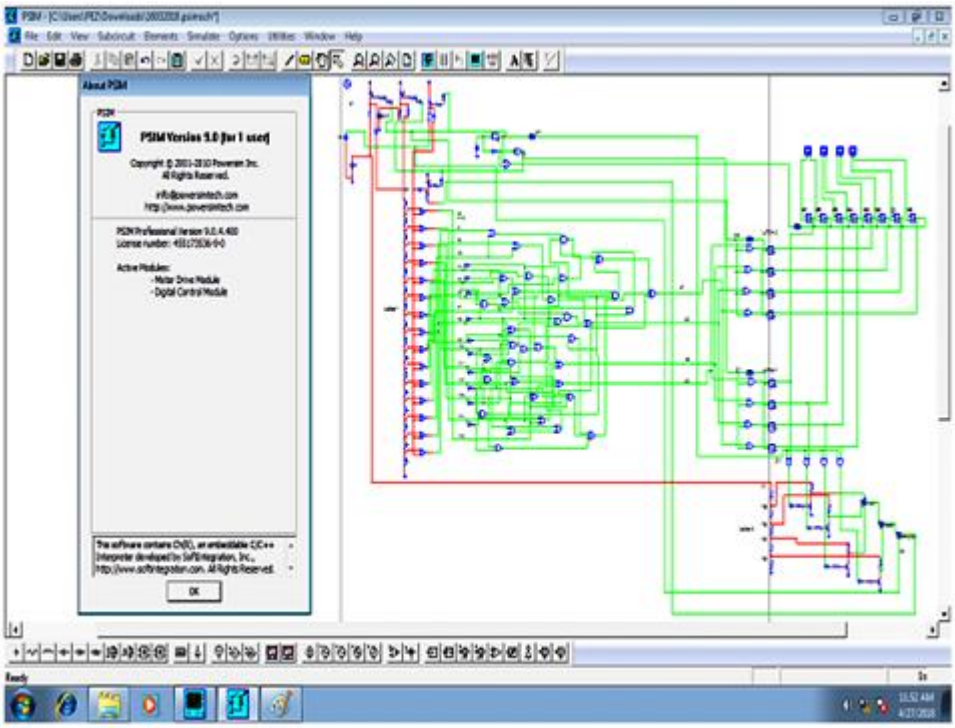


Fig. 3 Simulation of the circuit shown in Fig. 2a by PSIM P9

corresponding to the field in which the unknown analog signal belongs, while the lower end of the ladder is supplied with a voltage that corresponds to the analog voltage of the four MSB bits to which the unknown signal belongs. The circuit behaves in an identical manner as during C1 with priority encoder outputting a new set of four bits. These four bits are latched by latch 2, since it is active during C2. The outputs of Latch 2 are now stored in D3-D0 bits of the 1-byte register. The circuit is then reset so that it can accept the next new analog signal.

PSIM Professional 9 is used to simulate the circuit of Fig. 2a).

5. Experimental Results

Table 1-5 shows the input voltages and their corresponding outputs for reference voltages starting from 5V to 1V, with a gap of 1V between any two successive reference voltages. An interval of 0.25V is maintained between any two successive readings for any table. Each output voltage shown in any table corresponds to the average output voltage obtained for both increasing and decreasing input voltages. Error curves have been drawn for all reference voltage levels.

Table 1 I/P Vs. O/P for Ref. Voltage= 5V

Sr. No.	I/Ps (V)	Bit Pattern	O/Ps (V)	% Error
1	0.0	0000 0000	0.0	0.0
2	0.25	0000 1101	0.2549	1.96
3	0.5	0001 1001	0.4901	1.98
4	0.75	0010 0110	0.7451	0.65
5	1.0	0011 0100	1.0196	-1.96
6	1.25	0011 1111	1.2353	1.18
7	1.5	0100 1101	1.5097	-0.65
8	1.75	0101 1011	1.7647	-0.84
9	2.0	0110 0110	1.9804	0.98
10	2.25	0111 0011	2.2549	-0.22
11	2.5	0111 1111	2.4902	0.39
12	2.75	1000 1111	2.7647	-0.53
13	3.0	1001 1101	3.0784	-2.6
14	3.25	1010 1011	3.2745	-0.75
15	3.5	1011 0001	3.4706	0.84
16	3.75	1011 1110	3.7255	0.65
17	4.0	1100 1111	3.9804	0.49
18	4.25	1101 1010	4.2745	-0.58
19	4.5	1110 0111	4.5294	-0.65
20	4.75	1111 0110	4.7451	0.10
21	5.0	1111 1111	5.0	0.0

Table 2 I/P Vs. O/P for Ref. Voltage= 4V

Sr. No.	I/Ps(V)	Bit Pattern	O/Ps (V)	% Error
1	0.0	0000 0000	0.0	0.0
2	0.25	0000 1111	0.2510	-0.4
3	0.5	0010 0001	0.5020	-0.4
4	0.75	0011 0001	0.7529	-0.39
5	1.0	0100 0001	1.0196	-1.96
6	1.25	0101 0010	1.2549	-0.39
7	1.5	0110 0000	1.506	-0.4
8	1.75	0111 0000	1.7569	-0.39
9	2.0	0111 1111	1.9922	0.39
10	2.25	1000 1111	2.2431	0.31
11	2.5	1001 1111	2.4941	0.24
12	2.75	1010 1111	2.7451	0.18
13	3.0	1011 1111	2.9961	0.13
14	3.25	1100 1111	3.2471	0.09
15	3.5	1101 1111	3.4980	0.06
16	3.75	1110 1111	3.7490	0.03
17	4	1111 1111	4.0	0.0

Table 3 I/P Vs. O/P for Ref. Voltage= 3V

Sr. No.	I/Ps(V)	Bit Pattern	O/Ps(V)	%Error
1	0.0	0000 0000	0.0	0.0
2	0.25	0001 0011	0.2471	1.16
3	0.5	0010 1011	0.5059	-1.18
4	0.75	0011 1111	0.7412	1.18
5	1.0	0101 0110	1.0118	-1.18
6	1.25	0110 1011	1.2588	-0.70
7	1.5	0111 1111	1.4941	0.39
8	1.75	1001 0111	1.7765	-1.5
9	2.0	1010 1011	2.0118	-0.59
10	2.25	1011 1111	2.2471	0.13
11	2.5	1101 0111	2.5294	-1.18
12	2.75	1110 1111	2.7647	-0.53
13	3.0	1111 1111	3.0	0.0

Table 4 I/P Vs. O/P for Ref. Voltage= 2V

Sr. No.	I/Ps(V)	Bit Pattern	O/P(V)	% Error
1	0.0	0000 0000	0.0	0.0
2	0.25	0001 1111	0.2432	2.72
3	0.5	0011 1111	0.4941	1.18
4	0.75	0101 1111	0.7451	0.65
5	1.0	0111 1111	0.9961	0.39
6	1.25	1001 1111	1.2471	0.23
7	1.5	1011 1111	1.4980	0.13
8	1.75	1101 1111	1.7490	0.06
9	2.0	1111 1111	2.0	0.0

Table 5 I/P Vs. O/P for Ref. Voltage= 1V

Sr. No.	I/Ps(V)	Bit Pattern	O/Ps(V)	% Error
1	0.0	0000 0000	0.0	0.0
2	0.25	0011 1111	0.245	2.0
3	0.5	0111 1111	0.495	1.0
4	0.75	1011 1101	0.74	1.33
5	1.0	1111 1111	1.0	0.0

6. Error Curves

Fig. 4 shows five error curves for reference voltages starting from 5V to 1V. It is observed that for any curve, error percentage is more for low value of the input analog signal which is only to be expected. Series 1 corresponds to reference voltage 5V while Series 5 corresponds to 1V respectively.

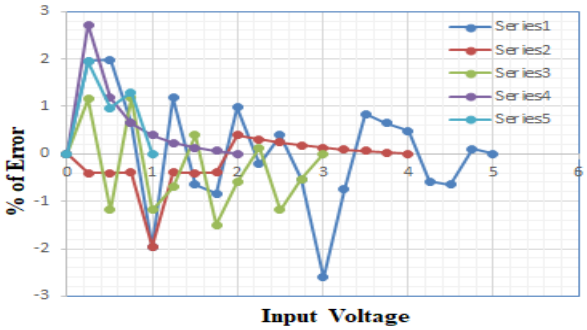


Fig. 4 Error curves for different input reference voltages

7. Comparison between Different Architectures

Number of comparators and clock cycles needed by different architectures, including the proposed one, is shown in Fig. 5a) for 8 and 16-bit resolutions, while the plot of comparator count versus resolution is depicted in Fig. 5b). The architectures of interest discussed in both the figures are flash or full flash, half flash, semi flash, simplified half flash, multi-step and the proposed one. For 8-bit resolution, number of comparators in the proposed scheme is slightly more than simplified half flash and multi-step types. But for 16-bit resolution, the proposed scheme requires fewer number of comparators compared to other architectures. From the point of view of the number of clock cycles required for 8-bit ADC, the proposed architecture requires same number of clock cycles as that of a flash ADC, but better than the other architectures. For 16-bit ADC, the proposed scheme is either

better (simplified half flash) or same as that of the other architectures, barring the full flash ADC which requires only one clock cycle.

Type of ADC	No. of comparators for		No. of cycles for	
	8-bit ADC	16-bit ADC	8-bit ADC	16-bit ADC
Full Flash [2]	255	65535	1	1
Half Flash (Conventional) [4]	30	510	2	2
Semi Flash [5]	15	255	2	2
Simplified Half Flash [14]	6	66	2	4
Multistep [10]	8	128	2	2
Proposed [1]	15	15	1	2

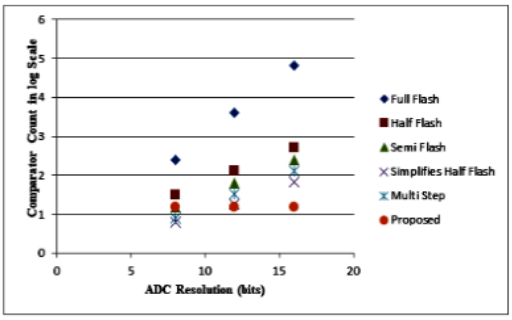


Fig. 5 a) Number of comparators and clock cycles needed for different architectures b) A plot of comparator count Vs. ADC resolution for different architectures

8. Conclusion

A variable resolution modified semi flash ADC design is presented in this paper. It achieved variable resolution by merely changing the required number of clock cycles. Design of a modified 8-bit semi flash ADC, based on BSS, is presented in hardware and simulated in PSIM P9. The idea of the presented technique is in a way based on flash ADC design. Higher order ADCs can be realized based on the presented technique. As an example, a 16-bit ADC can be designed and realized in only two clock cycles requiring only fifteen comparators. Extending the concept, a 24-bit ADC would require three clock cycles only. Thus, high resolution ADCs with very high speeds can be designed. Since the designed circuit requires drastically reduced number of comparators, hence it would require very low power and die area. The proposed design thus completely eliminates the need for an exponential increase in the number of comparators with increasing resolution, as it is the case with a flash ADC.

In the designed circuit, both the reference voltage to the ladder as also the input signal have been changed in the latter half of the clock cycle. It is different from pipeline or two step ADCs where only one or two bits are analyzed in a single clock cycle, while the presented method is based on BSS. In BSS, the whole bit pattern is divided into fields, which has been explained in text.

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