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INVESTIGATION ON CYLINDRICAL GATE ALL AROUND (GAA) TO NANOWIRE MOSFET FOR CIRCUIT APPLICATION

Biswajit Jena[1], Kumar Prasannajit Pradhan[2], Prasanna Kumar Sahu[2], Sidharth Dash[1], Guru Prasad Mishra[1], Sushanta Kumar Mohapatra[2]

[1]Device Simulation Lab, Institute of Technical Education & Research,
Siksha 'O' Anusandhan University, Khandagiri, Bhubaneswar, Odisha-751030, India
[2]Nano Electronics Laboratory, Department of Electrical Engineering,
National Institute of Technology (NIT), Rourkela, 769008, Odisha India.

Abstract. *Undoped cylindrical gate all around (GAA) MOSFET is a radical invention and a potential candidate to replace conventional MOSFET, as it introduces new direction for transistor scaling. In this work, the sensitivity of process parameters like channel length (Lg), channel thickness (t_{Si}), and gate work function (φ_M) on various performance metrics of undoped single material (SM) and double material (DM) cylindrical GAA (CGAA) to nanowire MOSFET are systematically analyzed. The electrical characteristics such as on current (I_{on}), subthreshold leakage current (I_{off}), the threshold voltage (V_{th}) and transconductance (g_m) are evaluated and studied with the variation of device design parameters. The discussion gives the direction towards low standby operating power (LSTP) devices as improvement in I_{off} is approaching 90% in nanowire MOSFETs. All the device performances of undoped SM and DM CGAA MOSFETs are investigated through Sentaurus device simulator from Synopsys Inc.*

Key words: *cylindrical gate all around, MOSFETs, SCEs, Analog and RF FOMs*

1. INTRODUCTION

To get low cost, high operational speed and better performance, the dimension of the conventional transistors need to be downscaled to sub-nanometer region. The reduction of MOSFET dimensions will degrade the gate control over the channel due to the close proximity between the source and drain. This leads to increase various short channel effects (SCEs) like hot carrier effect, threshold voltage roll-off, and substrate bias effect [1], [2]. Many new devices have been introduced in beyond Moore's era [3]–[5] to suppress the SCEs and enable further scaling down the device. Similarly, some multi-gate silicon on insulator (SOI) technology has also been proposed to replace the conventional

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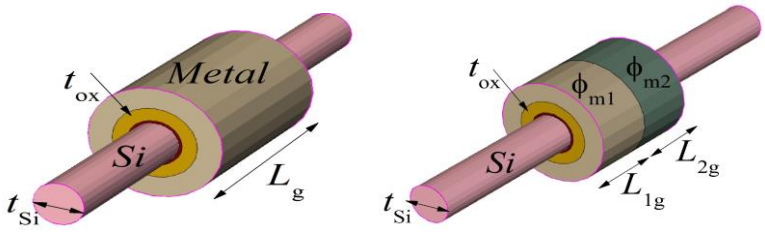
Corresponding author: K. P. Pradhan
Nano Electronics Laboratory, Department of Electrical Engineering, National Institute of Technology (NIT), Rourkela, 769008, Odisha India
(e-mail: skmctc74@gmail.com)

MOSFET [6]–[10]. However, the cylindrical gate all around (CGAA) MOSFET is one of the novel devices which further enables the scaling without hindering the device performance [11]. Because of the low characteristic length and higher drive current, CGAA MOSFETs can achieve higher packing density as compared to the double gate (DG) MOSFETs [12]–[16]. Also, CGAA MOSFET has excellent electrostatic control of the channel, robustness against SCEs, better scaling options, no floating body effect, larger Equivalent Number of Gates, ideal subthreshold swing as compared to other multiple-gate MOSFETs. Hence, the CGAA MOSFETs are a promising solution for nanoscale technology CMOS devices [17]–[21]. And the important device parameters like threshold voltage (V_{th}), and on-off ratio (I_{on}/I_{off}), are very much sensitive to the device geometry such as channel length (L_g), channel thickness (t_{Si}), and gate work function (φ_M). Thus, the authors have taken an attempt to present a detailed analysis of the performance dependency of SM and DM CGAA MOSFETs on device geometry variation.

In this paper, different performance metrics, like drain current (I_D), and transconductance (g_m) are systematically presented with the variation of L_g, φ_M, and t_{Si}. Along with the introduction, Section 2 describes the device structure description that includes all the dimensions, materials and doping concentrations of both SM and DM CGAA MOSFETs. This section also analyses the physics of the device using device numerical simulations and models activated for simulation. Section 3 comprises of all results and discussion. Finally, the concluding remarks are presented in section 4.

2. Device Description and Simulation Setup

The schematic diagram of the fully depleted single material (SM) and dual material (DM) Cylindrical GAA (CGAA) MOSFET structures used for modeling and simulation are shown in Fig. 1 (a) and (b) respectively. The radial and lateral directions of the channel are assumed to be along the radius and the *z*-axis of the cylinder as shown in Fig. 1. The source and drain of the device are uniformly doped with doping concentration of $N_D = 1\times 10^{20}$ cm^{-3}. The channel is kept undoped. The gate oxide thickness is t_{ox} = 1.1 nm. The metal gate work functions, φ_M=4.6 eV for SM and φ_{M1}=4.6 eV, φ_{M2}=4.6 eV for DM are considered.



(a) (b)

Fig. 1 Schematic Structure of Cylindrical Gate All Around (GAA) MOSFET (a) Single metal gate (b) Dual metal gate

The simulation is carried out by the device simulator Sentaurus, a 3-D numerical simulator from Synopsis Inc. [22]. To obtain accurate results for MOSFET simulation, we

need to account for the mobility degradation that occurs inside inversion layers. The default carrier transport model in Sentaurus is the Drift Diffusion model is activated.For the drift-diffusion model, the current densities for electrons and holes are given by:

$$\vec{J}_n = \mu_n(n\nabla E_C - 1.5nkT\nabla \ln m_n) + D_n(\nabla n - n\nabla \ln \gamma_n) \quad (1)$$

$$\vec{J}_p = \mu_p(p\nabla E_V + 1.5pkT\nabla \ln m_p) - D_p(\nabla p - p\nabla \ln \gamma_p) \quad (2)$$

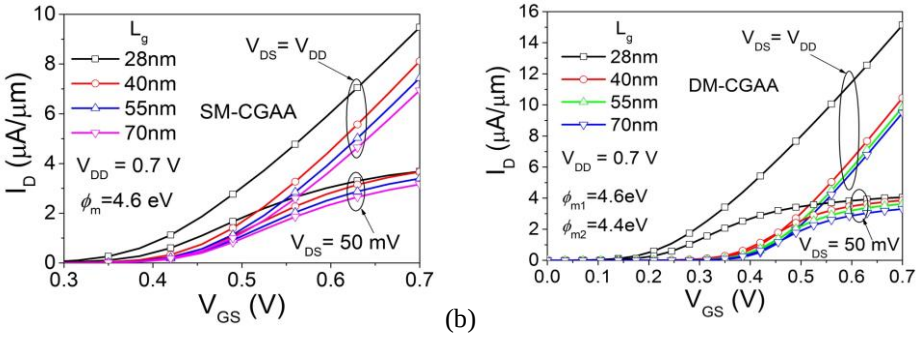
where, $\vec{J}_n$ and $\vec{J}_p$ are electron and hole current density. μ_n and μ_p represent electron and hole mobility. n and p describe electron and hole density. γ_n and γ_p are Fermi statistics constant, and m_n and m_p present spatial effective masses of electron and hole respectively. T and k describe temperature and Boltzmann constant. E_C and E_V are conduction and valance energy bands. D_n and D_p represent the diffusion constants for electron and holes respectively. In the simulation basic mobility a model is used that takes into account the effect of the doping dependence, high-field saturation (velocity saturation), and transverse field dependence. The silicon band gap narrowing model that determines the intrinsic carrier concentration is activated. Models for quantum mechanical effects have not been invoked when radius of the silicon pillar is changed from 10 nm to 5 nm.[23]. Uniform distribution of interface fixed charges $4x10^{11}$ cm^{-2} has been used in the simulation. The electron and hole surface recombination velocity are considered as $1x10^4$ cm/sec. The models activated in the simulation comprise of field dependent mobility, concentration dependent mobility and velocity saturation model. Model parameters used from the lookup table are carrier mobility μ_{no}=1076 cm^2/V.s, μ_{po}=460.9 cm^2/V.s, τ_n= τ_p= $1x10^{-7}$ s are the electron and hole lifetimes and suitable empirical parameters β_n, β_p are selected to calibrate the drift-diffusion transport model.

3. Results and Discussion

In order to analyze the impact of channel length (L_g), and channel thickness (t_{Si}), and gate work function (φ_M), on the device performance, the simulation is carried out by varying the above parameters. Fig. 2(a) and (b) show the drain current (I_D) in the linear scale as a function of the gate to source voltage (V_{GS}) for different L_g of both SM and CGAA MOSFETs. The DM-CGAA MOSFETs are showing a significant improvement in drive current as compared to SM-CGAA MOSFETs. In Fig. 2, L_g varies from 28 nm to 70 nm and we can observe from the figure that a decrease in L_g results a shift in the characteristics. The on-state current (I_{on}) increases dramatically as L_g decreases to below 30 nm in comparison to others. As channel length decreases, it gives rise to high drain current because of the relation $I_D \propto 1/L$.

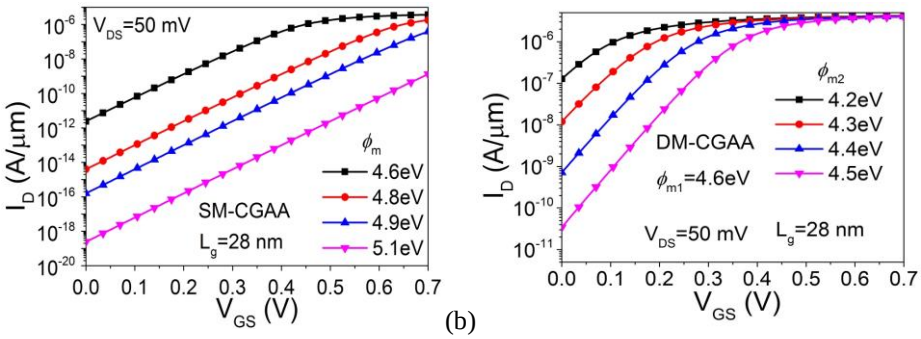
Fig. 3 represents the I_D-V_{GS} characteristic for different values of metal gate work function (φ_M) for both SM and DM-CGAA MOSFETs. The work function is varied from 4.6 eV to 5.1 eV for SM CGAA and φ_{M2} from 4.2 eV to 4.5 eV with φ_{M1}=4.6 eV at V_{DS}=50 mV (sub-threshold region of operation). In case of DM-CGAA, the φ_{M2} is varied in such a way that it has to satisfy the design condition, i.e., $\varphi_{M1}>\varphi_{M2}$. The results illustrate that the off-state leakage current (subthreshold performance) of the device improves for higher values of metal gate work function. Higher the the φ_M *increases*

threshold voltage that reduces leakage current and improves the subthreshold behavior of the device.



(a) (b)

Fig. 2 Drain current (I_D) in linear scale as a function of gate to source voltage (V_{GS}) for V_{DS}=50 mV with variation in L_g (28 nm to 70 nm) (a) SM-CGAA (φ_M=4.6 eV) (b) DM-CGAA (φ_{M1}=4.6 eV, φ_{M2}=4.4 eV)



(a) (b)

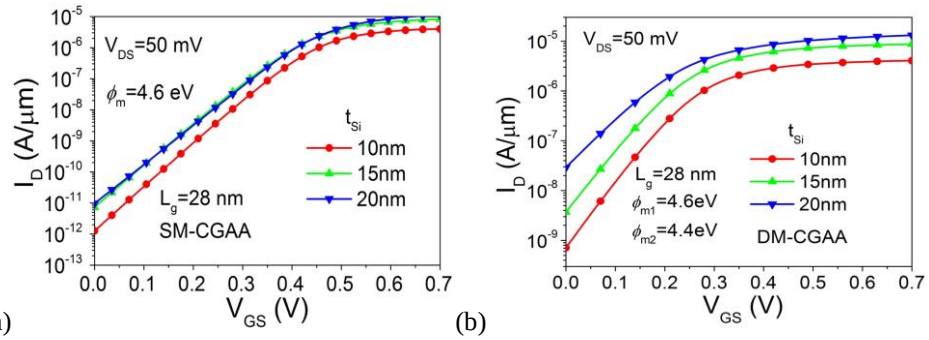
Fig. 3 Drain current (I_D) in log scale as a function of the gate to source voltage (V_{GS}) for V_{DS}=50 mV for different φ_M (a) SM-CGAA (b) DM-CGAA

Fig. 4 (a) and (b) reveal the I_D dependency on silicon body thickness (t_{Si}) of both SM and DM CGAA MOSFETs. The characteristic of I_{off} is also influenced by t_{Si}, which is cleared from Fig. 4. As the silicon film gets thinner, there is a significant improvement in leakage current because no further leakage path is available far from the gate. The DM devices show a little higher I_{off} than SM device cases, but they predict higher drive current (I_{on}) as compared to SM counterparts, which is verified from Fig. 2.

Transconductance (g_m) as a function of I_D for both SM and DM-CGAA MOSFETs are presented in Fig. 5(a) and (b) respectively. From the figure, it is clear that as the channel length decreases the g_m value is increasing because of high drain current. The high g_m will further enhance the transconductance generation factor ($TGF=g_m/I_D$) which is the requirement for the realization of circuits operating at low supply voltage. By comparing Fig. 5(a) and (b), the DM devices are superior to their SM counterpart.

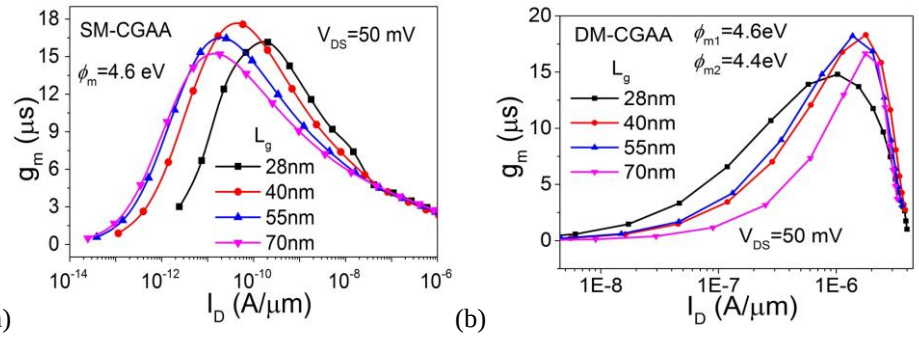
All the extracted and calculated values of DC performances are tabulated in Table 1, and Table 2, with the variation of silicon body thickness (t_{Si}), and channel length (L_g) of both SM and DM-CGAA MOSFETs. Table 1 compares and analyzes the sensitivity of t_{Si}

on various important parameters like I_{on}, I_{off}, and V_{th}. We can well control the V_{th} and SCEs like off state leakage current by reducing t_{Si} with a little compromise in on-state current. Hence, people always prefer a ultra-thin body (UTB) fully depleted (FD) SOI MOSFET as the body is completely controlled by the gate and there is no leakage path far from the gate. However, by considering two different gate metals, we can drastically enhance the drive current of the devices.



(a) (b)

Fig. 4 Drain current (I_D) in log scale as a function of gate to source voltage (V_{GS}) for V_{DS}=50 mV with variation in t_{Si} (10 nm to 20 nm) (a) SM-CGAA (φ_M=4.6 eV) (b) DM-CGAA (φ_{M1}=4.6 eV, φ_{M2}=4.4eV)



(a) (b)

Fig.5 g_m as a function of I_D at V_{DS}=50 mV with variation in L_g (a) SM-CGAA (φ_M=4.6 eV) (b) DM-CGAA (φ_{M1}=4.6 eV, φ_{M2}=4.4eV)

Table 2 summarizes the similar dc performances of both SM and DM devices for different values of channel lengths. It is clear from Table 2 that while the gate length is reduced the analog performance like transconductance (g_m) is increased because of high drain current for shorter gate length devices. However, the device having shorter L_g is more prominent towards SCEs due to high I_{off}.

Table 1 DC performance measures with t_{Si} variation at V_{DS}=50 mV

	SM-CGAA (φ_M=4.6eV)			DM-CGAA (φ_{M1}=4.6eV, φ_{M2}=4.4eV)		
t_{Si} (nm)	I_{on} (μA)	I_{off} (pA)	V_{th} (V)	I_{on} (μA)	I_{off} (nA)	V_{th} (V)
10	3.99	1.27	0.40	4.04	0.71	0.28
15	8.31	7.27	0.40	8.71	3.69	0.245
20	11.4	9.70	0.38	13.1	29.2	0.21

Table 2 Analysis of different parameters with L_g variation at V_{DS}=50 mV

	SM-CGAA (φ_M=4.6eV)			DM-CGAA (φ_{M1}=4.6eV, φ_{M2}=4.4eV)		
L_g (nm)	I_{on} (μA)	I_{off} (pA)	V_{th} (V)	I_{on} (μA)	I_{off} (pA)	V_{th} (V)
28	3.68	2.44	0.382	4.04	711	0.28
40	3.67	0.114	0.424	3.85	7.21	0.42
55	3.40	0.0386	0.431	3.63	0.838	0.45
70	3.16	0.0248	0.432	3.30	0.360	0.455

5. CONCLUSION

A cylindrical gate all around (GAA) with gate engineering, i.e., single gate material (SM) and two different gate electrode (DM) is explored and the performance evaluation is carried out with extensive device simulation by Sentaurus^{TM} simulator. The sensitivity of device parameters like t_{Si}, φ_M, and L_g on various DC performances are systematically presented. Improvement in device performance for low standby operating power (LSTP) applications can be achieved with reduced in body thickness and *higher gate work function*. The subthreshold leakage current is significantly improved when the device approaches to the nanowire, i.e., t_{Si}=10 nm, and for higher φ_M values. Similarly, continuous miniaturization of L_g is required for getting high I_{on} and g_m. The DM-CGAA shows a higher drive current as compared to SM counterpart with little compromise in off state leakage current. Hence, an appropriate selection of the silicon thickness, and metal gate work function give rise to an optimum threshold voltage at a given channel length and drain bias.

REFERENCES

[1] K. K. Young, "Short-channel effect in fully depleted SOI MOSFETs", *IEEE Trans. Electron Devices*, vol. 36, no. 2, pp. 399–402, 1989.

[2] S. Bangsaruntip, G. M. Cohen, A. Majumdar, and J. W. Sleight, "Universality of short-channel effects in undoped-body silicon nanowire MOSFETs", *IEEE Electron Device Lett.*, vol. 31, no. 9, pp. 903–905, 2010.

[3] T. Skotnicki, J. A. Hutchby, T. J. King, H. S. P. Wong, and F. Boeuf, "The end of CMOS scaling: Toward the introduction of new materials and structural changes to improve MOSFET performance", *IEEE Circuits Devices Mag.*, vol. 21, no. 1, pp. 16–26, 2005.

[4] J. P. Colinge, "Multiple-gate SOI MOSFETs", *Solid. State. Electron.*, vol. 48, no. 6, pp. 897–905, 2004.

[5] L. Chang, Y. C. Y. Choi, D. Ha, P. Ranade, S. X. S. Xiong, J. Bokor, C. Hu, and T. J. King, "Extremely scaled silicon nano-CMOS devices", In Proceedings of the IEEE, vol. 91, no. 11, pp. 1860–1873, 2003.

[6] V. M. Srivastava, K. S. Yadav, and G. Singh, "Design and performance analysis of double-gate MOSFET over single-gate MOSFET for RF switch", *Microelectronics J.*, vol. 42, no. 3, pp. 527–534, 2011.

[7] J. Colinge, "From gate-all-around to nanowire MOSFETs", In Proceedings of the International *Semiconductor Conference, CAS 2007*, vol. 1, pp. 11–17.

[8] K. P. Pradhan, S. K. Mohapatra, P. K. Sahu, and D. K. Behera, "Impact of high-k gate dielectric on analog and RF performance of nanoscale DG-MOSFET", *Microelectronics J.*, vol. 45, no. 2, pp. 144–151, 2014.

[9] S. K. Mohapatra, K. P. Pradhan, L. Artola, and P. K. Sahu, "Estimation of analog/RF figures-of-merit using device design engineering in gate stack double gate MOSFET", *Mater. Sci. Semicond. Process.*, vol. 31, no. 0, pp. 455–462, 2015.

[10] S. K. Mohapatra, K. P. Pradhan, and P. K. Sahu, "Resolving the bias point for wide range of temperature applications in high-k/metal gate nanoscale DG-MOSFET", *Facta Universitatis Series: Electronics and Energetics*, vol. 27, no. 4, pp. 613–619, 2014.

[11] T.-K. Chiang and J. J. Liou, "An analytical subthreshold current/swing model for junctionless cylindrical nanowire FETs (JLCNFETs) ", *Facta Universitatis Series: Electronics and Energetics*, vol. 26, no. 3, pp. 157–173, 2013.

[12] S. K. Gupta and S. Baishya, "Modeling of cylindrical surrounding gate MOSFETs including the fringing field effects", *J. Semicond.*, vol. 34, no. 7, pp. 1–6, 2013.

[13] M. R. Kumar, S. K. Mohapatra, K. P. Pradhan, and P. K. Sahu, "A simple analytical center potential model for cylindrical gate all around (CGAA) MOSFET", *J. Electron Devices*, vol. 19, pp. 1648–1653, 2014.

[14] H. Abd-Elhamid, B. Iñiguez, D. Jiménez, J. Roig, J. Pallarès, and L. F. Marsal, "Two-dimensional analytical threshold voltage roll-off and subthreshold swing models for undoped cylindrical gate all around MOSFET", *Solid. State. Electron.*, vol. 50, no. 5, pp. 805–812, 2006.

[15] R. Gautam, M. Saxena, R. S. Gupta, and M. Gupta, "Gate all around MOSFET with vacuum gate dielectric for improved hot carrier reliability and RF performance", *Electron Devices, IEEE Trans.*, vol. 60, no. 6, pp. 1820–1827, 2013.

[16] A. Cerdeira, M. Estrada, J. Alvarado, I. Garduño, E. Contreras, J. Tinoco, B. Iniguez, V. Kilchytska, and D. Flandre, "Review on double-gate MOSFETs and FinFETs modeling", *Facta Universitatis Series: Electronics and Energetics*, vol. 26, no. 3, pp. 197–213, 2013.

[17] Y. Pratap, P. Ghosh, S. Haldar, R. S. Gupta, and M. Gupta, "An analytical subthreshold current modeling of cylindrical gate all around (CGAA) MOSFET incorporating the influence of device design engineering", *Microelectronics J.*, vol. 45, no. 4, pp. 408–415, 2014.

[18] T. K. Chiang, "A compact model for threshold voltage of surrounding-gate MOSFETs with localized interface trapped charges", *IEEE Trans. Electron Devices*, vol. 58, no. 2, pp. 567–571, 2011.

[19] L. Zhang, C. Ma, J. He, X. Lin, and M. Chan, "Analytical solution of subthreshold channel potential of gate underlap cylindrical gate-all-around MOSFET", *Solid. State. Electron.*, vol. 54, no. 8, pp. 806–808, 2010.

[20] D. Sharma and S. K. Vishvakarma, "Precise analytical model for short channel Cylindrical Gate (CylG) Gate-All-Around (GAA) MOSFET", *Solid. State. Electron.*, vol. 86, pp. 68–74, 2013.

[21] I. Ferain, C. A. Colinge, and J. Colinge, "Multigate transistors as the future of classical metal–oxide–semiconductor field-effect transistors", *Nature*, vol. 479, pp. 310–316, 2011.

[22] http://www.synopsys.com/, "Sentaurus TCAD User's Manual", In Proceedings of the *Synopsys Sentaurus Device*, pp. 191–403.

[23] A. Tsormpatzoglou, D. H. Tassis, C. A. Dimitriadis, G. Ghibaudo, G. Pananakakis, and R. Clerc, "A compact drain current model of short-channel cylindrical gate-all-around MOSFETs", *Semicond. Sci. Technol.*, vol. 24, no. 7, p. 75017, 2009.