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CAPACITIVE METHODS FOR TESTING OF POWER SEMICONDUCTOR DEVICES

Vaclav Papež[1], Jiri Hájek[1], Bedrich Kojecký[2]

[1]Department of Electrotechnology, Faculty of Electrical Engineering,
Czech Technical University in Prague. [2]Prague, Czech Republic

Abstract. *Electrical capacity of power semiconductor devices is quite an important parameter that can be utilized not only for testing a component itself, but it can also be applied practically; e.g. in series-connected high voltage devices. This paper first analyzes the theoretical voltage distribution on the bases of the polarized p-n junction, as well as the size of capacity. The measurement of the voltage-capacity dependence using the resonance principle is illustrated on the samples of 4kV and 6kV thyristors. The correspondence between theoretical estimation of the capacity, measured voltage capacity dependence based on the resonance principle and experimentally determined by injected charge proves the correctness of the applied procedures and assumptions.*

Key words: *capacity, p-n junction, voltage dependence, series connection of devices.*

1. INTRODUCTION

Most of the world leading manufacturers of power semiconductor devices offer discreet rectifying elements (diodes/thyristors) with off-state and reverse voltage up to 6 kV or 7 kV. Thus, higher voltage converters must be constructed from serial-connected devices. The devices for a series connection (so called high voltage stack) must be chosen according to the following rules:

- For static processes, the components must have "consistent" *I-V* characteristics; distribution dissipation resistors are often used for uniform voltage,
- For dynamic loading (in a frequency application) a commutating charge of the components must also be considered; therefore resistor dividers are often supplemented with capacities.

Knowing the voltage dependence of the dynamic capacity of reverse polarized devices can help to design and optimize the series-connected high voltage stacks. In the following section, the distribution of charges and capacity between both bases of a polarized p-n junction will be theoretically described.

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Corresponding author: Vaclav Papež
Department of Electrotechnology, Faculty of Electrical Engineering, Czech Technical University in Prague, Czech Republic
(e-mail: mnet.ok1vvp@atlas.cz)

The evaluation of the voltage dependence of the dynamic capacity of a reverse polarized junction can also be a non-destructive measurement method enabling the evaluation of some physical and technological parameters of the device material. The same method can be used to evaluate the quality of the finished encapsulated devices, which allows verifying a real value of the electric field at the p-n junction or the resistivity of initial bulk silicon used for the wafer processing.

2. Basic Theoretical Analysis

The p-n junction of a high-voltage silicon semiconductor devices is generally created by sufficiently long high temperature (above 1200 °C) diffusion of acceptor atoms (Al, B) into a single crystal **N**-type Si wafer of typical resistivity in the order of 100 Ωcm. A p-n junction extends to the depth of 80 μm-120 μm; the concentration profile of dopants follows the Error function complement (erfc (x)) or Gaussian distribution.

In a reverse polarization and at a constant applied voltage, the structure is passed through by a constant reverse current formed by so called diffusion and recombination components [1], [2]. At a room temperature and a voltage in the order of 1.0 kV, the reverse current reaches the value in the order of 1 μA. This assumption holds for 2” devices (both for diodes or thyristors) used in experiments. The distribution of the electric field on individual layers is described by Poisson’s equation

$$\frac{dE}{dx} = \frac{qN(x)}{\varepsilon}, \tag{1}$$

where E is the electric field, N is the density of electrically charged dopants and ε is Si permittivity. In a wide **N** basis, the density of donors is constant and the voltage distribution V_N has a simple shape

$$V_N = \frac{qN_D}{\varepsilon_0 \varepsilon_r}\left(x d_N - \frac{x^2}{2} \right), \tag{2}$$

where d_N is the width of the space charge region (SCR) in the **N** basis. An exact solution of Poisson’s equation for the adjacent layer **P** is a lot more complicated. However, basically essential for further consideration is the voltage on the layer. The layer inherently determines a maximum allowable voltage on the layer **N**, and thus the total reverse voltage of the junction structure

$$V_T = V_N + V_P . \tag{3}$$

The requirement of equality of the charge Q on adjacent layers represents another output of Poisson’s equation

$$Q_N = Q_P = S\sqrt{2qN_D \varepsilon_0 \varepsilon_r V_N} . \tag{4}$$

Regarding low values of reverse currents in a stationary mode, practically applicable values of Q can be obtained only by numerical integration of the time current flows through the structure at a pulse loading by a sufficiently high (in the order of 100 Hz) frequency, or by a numerical integration of charging current of a parametric capacitor representing a monitored junction.

At a sinusoidal type of loading, the charge pumped during one half-cycle after the substitution into expression (4) determines the value of the relevant part of the total voltage on the layer **N**. After further substitution into expression (3), we can compute currently immeasurable value of the voltage V_P at the layer **P**

$$V_P = V_T - \frac{Q^2}{2S^2 q N_D \varepsilon_0 \varepsilon_r} . \quad (5)$$

For differential (measured) capacity of the layer **N** holds

$$C_N = S\sqrt{\frac{q N_D \varepsilon_0 \varepsilon_r}{2V_N}} . \quad (6)$$

From the formula for the total capacity C_T of the layers adjacent is series

$$C_T = \frac{C_N C_P}{C_N + C_P} , \quad (7)$$

we can determine the dependence of $C_{\mathbf{P}}$ as a function of voltage on individual layers.

If the dependence of the capacity C_T on the voltage V_T applied to the junction is measured, then the charge accumulated in the junction capacities can be expressed as

$$Q(\tau) = \int_0^{\tau} \frac{dV_T(t)}{dt} C_T(V_T) dt . \quad (8)$$

The result of the integration is not dependent on the course of the function $V(t)$. The voltage dependence of the charge accumulated in the junction capacities can be obtained by substituting the inverse function $t = f(V)$ into (8).

3. Description of the Samples

All the following experiments and measurements were carried out on two independent groups of thyristors. These groups have totally different technology processing, predicted for similar application (phase control rectifiers, “F” housing puck design). Each group of thyristors contained five samples. Samples were taken from one production batch.

First group contains samples of phase controlled rectifiers (PCR) with reverse and off-state voltage of 4 kV in diameter of 2". The PCRs were made by soldering technology, where Si wafer is soldered using a 30μm thick AlSi film on a molybdenum substrate of the same diameter (53 mm). The thickness of the Mo disk base is 1.2 mm; the thickness of the Si substrate is about 800 μm and soldering to the anode side takes place in vacuum at about 700 °C. The required off-state voltage of 4 kV allows using a simple two-layer positive and negative bevelling (at an angle of about 30°) from the cathode side. An acid etched bevelling (a solution of HF and HNO3) is protected by a conventional silicone gel

HIPAC Q1-9205. An active area of the blocking junction at the cathode side of the thyristor is about 1700 mm^2; an active area of the reverse junction at the anode side is about 2150 mm^2. The active area of the cathode is coated with a layer of vapor-deposited contact metal (aluminum). The design of PCR uses a built-in amplifying gate. A simplified cross-section of the thyristor (without housing) is shown in Fig. 1, left.

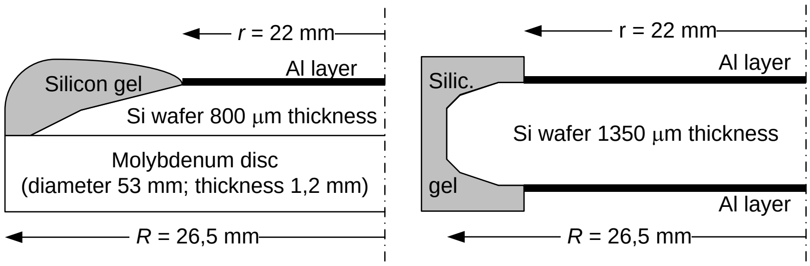

Fig. 1 Cross-section of non-symmetrical structure of a 4kV PCR (left) and 6kV structure processed by strictly symmetrical free-floating technology (right).

Second group of samples contains phase controlled rectifiers with reverse and off-state voltage of 6 kV in diameter of 2". This PCR uses free-floating technology and very thick (up to 1350 μm) Si wafer. The thyristor is loosely mounted between two dilatation Mo discs with a thickness of about 1 mm. The Si wafer is two-sided edged; two two-layer negative bevellings are used again. On the etched bevelling a high protective layer of the silicon rubber HIPAC Q1-9205 is applied. The thyristor also uses the design with the amplifying gate. Active areas of a thyristor blocking and reversed junctions are approximately the same, of 1600 mm^2, coated with a thin layer of vapor-deposited aluminum. A simplified cross-section of the thyristor (without housing) is shown in Fig. 1, right.

4. Provided Measurements

4.1 Measurement of voltage properties

The measurement of the DC reverse and off-state *I-V* characteristics was carried out by means of a DC method using a high voltage power supply SZ 10/2. The power supply was controlled by a computer program in a voltage range of 0-6 kV respective 8 kV, with a current limitation of 2 mA. DC voltage has been applied with the d*V*/d*t* rate of 1 kV/sec in both polarities. A gate port of the tested PCR has been opened. The characteristics were measured in a short time (of 6-8 seconds), thus the influence of temperature increase was negligible with respect to a low power loss.

Behaving of samples in both groups of thyristors was nearly identical with respect to achieved accuracy of measurement. Here and bellow presented results were obtained always for one current sample. Measured values were not deformed by means of any statistic processing.

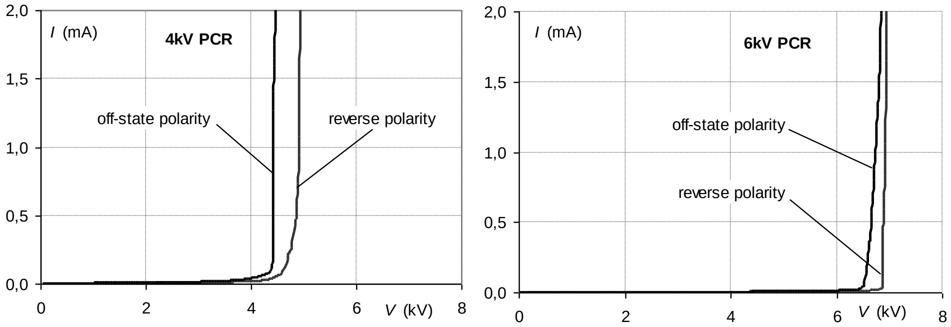

Fig. 2 Typical DC reverse and off-state *I*-*V* characteristics of both groups of samples.

4.2 Measurement of the charge

The first way of the measurement of the injected charge is based on the measurement at the voltage analyzer Schuster SML 698. The device utilizes a pulse method [3]. The measured waveforms of the reverse/off-state voltage (*V*) and the injected capacity current (*I*) are shown in Figure 3. There was chosen such a waveform which refers to a half period of 50Hz sinusoidal voltage. The applied voltage was lower than the breakdown voltage during the entire measurement. It was measured by a DC method, as described in the previous section.

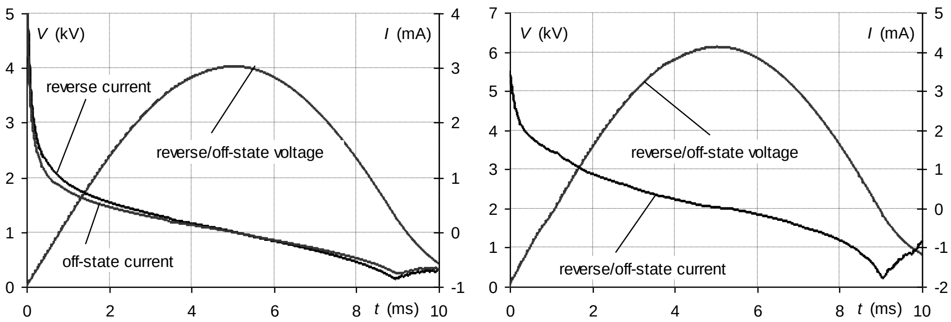

Fig. 3 Pulse measurement at the analyzer Schuster SML 698: Reverse and off-state voltage and current waveforms (4kV PCR left; 6kV PCR right).

From the measured values of the capacity current, a numerical integration was carried out. The interval from zero to the maximum applied voltage (5 ms) was considered. Thus the dependence of the injected accumulated charge from the area of an expanding p-n junction on the outer applied voltage was obtained. The injected charge is illustrated in Figure 4 as the waveform “SML 698”.

Another method of determining the injected charge is based on the dependence of the parametric p-n junction capacity on the applied voltage. This method is described below. Injected charge obtained using this method is illustrated in Figure 4 as the waveform “dynamic capacity”.

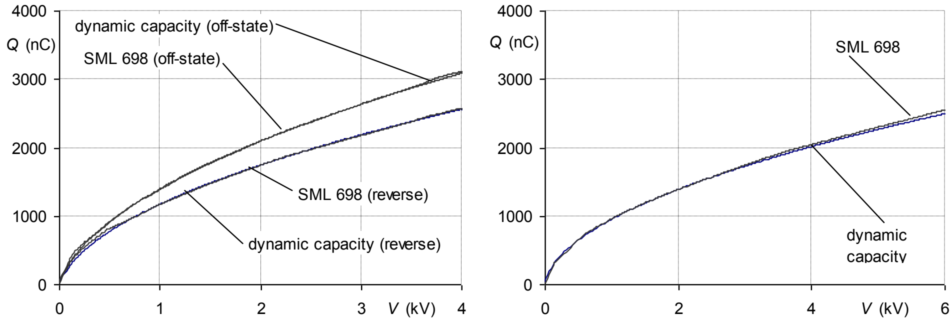

Fig. 4 Experimentally and numerically determined injected charges from a p-n junction area (4kV PCR left; 6kV PCR right).

4.3 Measurement of capacity of p-n junction under reverse bias voltage

The measurement of reverse polarized p-n junction semiconductor capacity is a methodology commonly used in the manufacture monitoring and testing of semiconductor devices. The measurement is very simple on principle, see Fig. 5. In an ideal case, to ensure the measurement, a capacitance meter (an AC RLC meter) and low power regulated DC power supply delivering required bias voltage is sufficient.

A measured p-n junction is biased by a reverse voltage from a DC power source through the impedance Z_1 which is chosen to be passed through by only a negligible part of the measuring current and, at the same time, a DC voltage drop between the source and the measured junction were small. In usual measurements at a higher frequency in units to tens of kHz and at a reverse current in units to tens of μA, the resistor with real resistance of the size of several hundreds of kΩ to the units of MΩ is used as decoupling impedance.

The RLC meter is separated from the DC bias circuit by the capacitor *C*. The capacity of the capacitor must be chosen much higher than the maximum measured capacity, without the need to correct the measurement results. The capacitor must also withstand the maximum DC voltage supply without being damaged. In case it is not possible to ensure the capacitor charging by the current passing through the RLC meter, the passage of the charging current is ensured by the impedance Z_2 that satisfies the same requirements as those for the impedance Z_1.

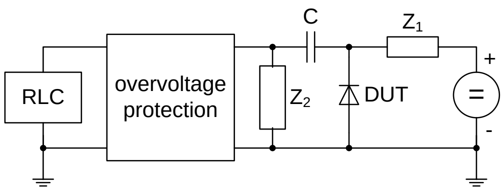

Fig. 5 Block diagram of the connection between an RLC analyzer and investigated p-n junction (DUT).

The measuring circuit can be supplemented with over voltage protection circuits that must be designed with regard to their minimum effect on the measured capacity and that will be able to prevent the penetration of the over voltage to the RLC meter. However, their protection effectiveness is not usually high. In case of breakdown at the measured p-n junction during high voltage measurements, the over voltage protection circuits are not usually able to ensure the RLC meter protection.

The most serious drawback of the measuring circuit is that the separation of the high voltage biasing circuit from the measuring part of the RLC circuit is only virtual. Any rapid change in voltage in a high voltage circuit part is transmitted to a measuring circuit part, and in the worst case, with a full voltage level. Breakdown, an avalanche process on the measured junction, or an imperfect contact in the circuit of the measured junction between the decoupling capacitor and impedance meter give rise to the over voltage at the RLC meter clips, which usually leads to the destruction of the RLC meter, when measured at voltages greater than several tens of volts.

For our measurements, we used a new measuring circuit design, where the p-n junction, whose capacity is being measured, was inserted into the resonance circuit. The circuit resonance frequency is evaluated and the searched p-n junction capacity is determined by its value. The circuit resonance frequency of the inductance *L* and capacitance *C* is expressed by formula

$$f = \frac{1}{2\pi\sqrt{LC}} . \tag{9}$$

It must be considered that the resonance circuit capacity is not determined exclusively by the measured p-n junction capacity C_M, but also by its coil self-capacity, connection capacity C_C, and capacity C_S of the decoupling capacitor that is connected in series with the measured capacity. Expression (10) holds for capacity *C*, which must be also considered when evaluating the measured capacity

$$C = C_C + \frac{C_M C_S}{C_M + C_S} . \tag{10}$$

The evaluation of the resonance circuit frequency is easily performed by adding the resonance circuit to the oscillator working as a control circuit, and by measuring the operating frequency of the oscillator, as shown in Figure 6.

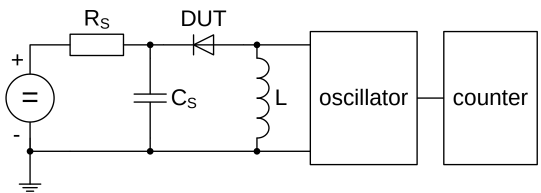

Fig. 6 Resonance method of measurement capacity of a biased p-n junction.

Both inductance and the resonance circuits can also be utilized for the construction of a special measuring circuit. The coil that shows minimum DC resistance can be used to mount an effective decoupling circuit that will reduce the penetration of the over voltage into the measuring circuit. The resonance circuit works as a narrowband filter which strongly inhibits the penetration of energy of potential avalanche processes and discharges in the high voltage circuit part to other circuits. In the resonance circuit, the coil itself or another decoupling capacitor are chosen to be high-voltage damage resistant.

The operating frequency of the oscillator is evaluated, and by its value, the searched p-n junction capacity is determined either by the computation according to expressions (9) and (10) or automatically. If the processor is used as a frequency meter, the measured capacity can be evaluated automatically. Such evaluation can be done easily, e.g., by reading the searched values from the table of the calculation results.

To reach the maximum over voltage protection of the measuring device, the oscillator can be designed by using a vacuum tube as an active element. The energy sufficient to damage the vacuum tube is much higher than the energy sufficient to damage the semiconductor element [4]. Block diagram of the system for measuring high-voltage semiconductor device capacity is shown in Fig. 7.

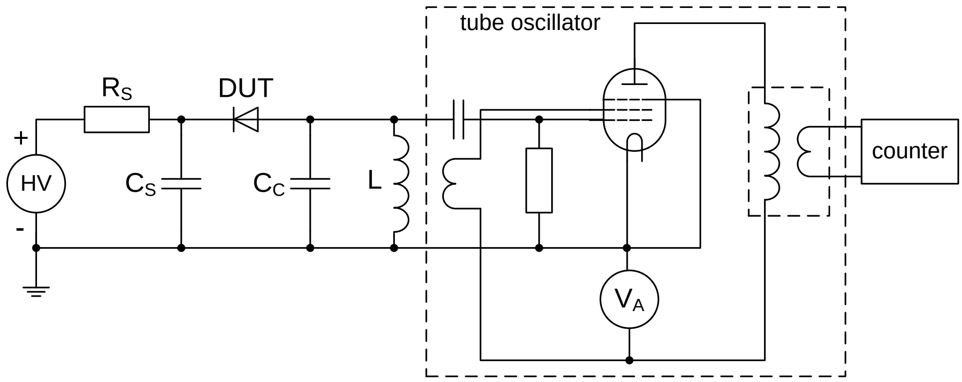

Fig. 7 Block diagram of an apparatus for capacity measurement.

Measured p-n junction is represented by a diode (DUT), see Figure 7. One lead of the diode (an anode) is connected to the coil L of the resonant circuit, whereas a second lead (a cathode) is connected to the separating capacitor C_S and separating resistor. The capacity of the separating capacitor is usually relatively high. It is greater than the highest measured capacity so that the sensitivity of the measuring device for highest measured capacity would not be diminished. The impedance of the resonance circuit transformed into a node between the measured p-n junction and separating capacitor is small. The separating resistor has a high resistance value not to attenuate the resonance circuit too much. Further, the resistor connects the high voltage supply (HV) to the measured p-n junction.

The capacitor C_C is not a physically existing component. Capacity C_C represents a self-capacitance of the coil and the capacity of connections that must be considered in evaluating the measured capacity. This design also allows the alternation of polarization voltage. Resonance circuit (consisting of DUT, C_C, L) is designed as a controlling resonance circuit of the vacuum-tube oscillator. Operating frequency of the oscillator determines the capacity of the measured p-n junction.

A high-impedance terminal of the resonant circuit serves as a node between the measured p-n junction and coil *L*. The terminal is connected to a control grid of the oscillating tube via the separating capacitor. The feed forward is created from the second grid of the tube by a coupling coil. The output signal from the oscillator is taken from a separating transformer in the anode circuit so that the oscillator operates as a three-point oscillator of a Meissner type with an electron coupling.

The operating frequency of the oscillator is evaluated by a simple digital frequency counter or a digital processor. This frequency can be eventually used even for the automatic evaluation of the measured capacity. The described device allows measuring of the capacity in the range of 10 pF to 10 nF with an accuracy better than 1 %. At the same time, a measured object (p-n junction) is polarized by DC voltage adjustable from a few tens of volts to 8 kV.

5. Results of the Measurements and their Discussion

The typical measured dependence of the thyristor capacities on the external applied voltage is shown in Figure 8. In theory, for the total junction capacity C_T, it is possible to use the following equation

$$C_T^2 V_N = S^2 \left(\frac{1}{2} q N_D \varepsilon \right), \tag{11}$$

where C_T is the total capacity of the diode and V_N is the voltage distributed on an **N** base. From the measured waveforms shown in Figure 4, there can be derived relatively accurately the experimental equation for the total capacity C_T

$$C_T^2 V_T = K\,, \tag{12}$$

where K is a general constant.

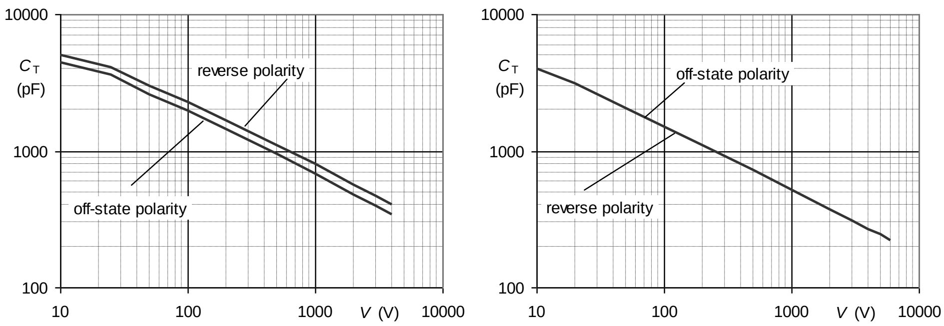

Fig. 8 Dependence of the sample capacities on the applied voltage (4kV PCR left; 6kV PCR right)

At the thyristor, there are generally two similar dependences generated under different conditions; in thyristor polarization by reverse or off-state voltages, which depends on the conditions whether the areas of cut-off junctions in the thyristor structure are the same or different for different polarities. Measured dependences *C-V* and *I-t* were used for creating the final (target) dependence *Q-V*. This final dependence was used also for mutual comparison. Searched *Q-V* dependence was obtained by three different approaches:

- In the first case, the dependence was obtained as the time integral of the charging current.
- In the second case inversion dependence was obtained. *V-Q* dependence was obtained as a dependence of voltage of polarized p-n junction on accumulated charge. We consider the measured voltage dependence of junction capacity, as it is given by Eq. (13).
- In the third case, when approximately evaluating the voltage dependence of the junction capacity, the total capacity of the junction was considered as a series connection of two capacities $C_{\mathbf{N}}$ and $C_{\mathbf{P}}$ according to Equation (7). Capacity $C_{\mathbf{N}}$ was simply approximated by Equation (6) as inversely proportional to the square root of V_{N} and capacity $C_{\mathbf{P}}$ as inversely proportional to the cube root of V_{P} (14).

$$V(n) = \sum_{1}^{n} \frac{Q(i)}{C(V_{(i)})} . \tag{13}$$

$$C_P = \frac{K}{\sqrt[3]{V_P}} . \tag{14}$$

The dependence of polarizing voltage of the device on the accumulated charge was determined similarly as in the second case. The only difference was that the total capacity of the device was approximated by Equation (15), for which optimum values of the constants were searched numerically.

$$C_T = \left[\frac{\sqrt[3]{V_P}}{K_1} + \frac{\sqrt{V_N}}{K_2} \right]^{-1} . \tag{15}$$

From the $C_{\mathbf{N}}$ capacity values (6) mentioned in the previous section some basic parameters of the samples can be calculated.

6. Conclusions

The main contribution of this paper is the description of newly developed measuring equipment. This equipment is designed for semiconductor p-n junction capacity measurement under high voltage bias. The use of standard RLC analyzer is exposed to the risk of equipment damage due to voltage penetration into the analyzer.

The principle of described technical solution is the connection of measured capacity (e.g. p-n junction) to a resonance circuit. Measured capacity is evaluated according to the resonance frequency of the circuit or according to the frequency of the oscillator.

The advantage of described solution is the usage of coil as a separation circuit element. The coil effectively prevents the penetration of surge voltage into the measuring circuit (RLC analyzer). Resonance circuit serves as a narrow band-pass filter heavily suppressing possible surge voltage. The coil and other separating capacities are designed to withstand high voltage peaks.

In previous works [5], only the properties of high voltage diodes were observed by described equipment. For the diode samples with their junction area $S = 18\ \mathrm{cm}^2$ for the applied voltage $V_T = 6$ kV and an accumulated charge 3 μC were determined $V_N = 5.3$ kV; $C_{\mathbf{N}} = 294$ pF; $C_{\mathbf{P}} = 2900$ pF. Space charge region extension in the **N** base and the maximum electric field intensity in the region can be specified as $x_{max} = 680$ μm and $E_{max} = 15.6$ kV/mm.

Similar voltage and capacitance distributions between the **P** and **N** bases were obtained for herein described samples of thyristors:

- For the samples of symmetrical thyristors with the junction area $S = 16\ \mathrm{cm}^2$, for the applied voltage $V_T = 6$ kV in reverse and off-state polarity and for accumulated charge 2.5 μC were determined: $V_N = 4.9$ kV; $C_{\mathbf{N}} = 257$ pF; $C_{\mathbf{P}} = 1400$ pF. Space charge region extension in the **N** base and the maximum electric field intensity in the region can be specified as $x_{max} = 630$ μm and $E_{max} = 15.8$ kV/mm.
- For the samples of soldered thyristors with the junction area $S = 17\ \mathrm{cm}^2$, for the applied voltage $V_T = 4$ kV in the reverse polarity and accumulated charge 3.1 μC were determined: $V_N = 3.4$ kV; $C_{\mathbf{N}} = 330$ pF; $C_{\mathbf{P}} = 4500$ pF. Space charge region extension in the **N** base and the maximum electric field intensity in the region can be specified as $x_{max} = 420$ μm and $E_{max} = 16.2$ kV/mm.
- For the samples of soldered thyristors with the junction area $S = 21\ \mathrm{cm}^2$ for the applied voltage $V_T = 4$ kV in the off-state polarity and accumulated charge 3.1 μC were determined: $V_N = 3.3$ kV; $C_{\mathbf{N}} = 410$ pF; $C_{\mathbf{P}} = 4500$ pF. Space charge region extension in the **N** base and the maximum electric field intensity in the region can be specified as $x_{max} = 400$ μm and $E_{max} = 16.5$ kV/mm.

These results correspond well to achievable Si material parameters (E_{max} 22 kV/mm), as well as to the technological parameters of components.

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