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ZTC BIAS POINT OF ADVANCED FIN BASED DEVICE: THE IMPORTANCE AND EXPLORATION

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Abstract. *The present understanding of this work is about to evaluate and resolve the temperature compensation point (TCP) or zero temperature coefficient (ZTC) point for a sub-20 nm FinFET. The sensitivity of geometry parameters on assorted performances of Fin based device and its reliability over ample range of temperatures i.e. 25 ^{0}C to 225 ^{0}C is reviewed to extend the benchmark of device scalability. The impact of fin height (H_{Fin}), fin width (W_{Fin}), and temperature (T) on immense performance metrics including on-off ratio (I_{on}/I_{off}), transconductance (g_m), gain (A_V), cut-off frequency (f_T), static power dissipation (P_D), energy (E), energy delay product (EDP), and sweet spot ($g_m f_T/I_D$) of the FinFET is successfully carried out by commercially available TCAD simulator Sentaurus^{TM} from Synopsis Inc.*

Key words: *FinFET, TCP or ZTC, H_{Fin}, W_{Fin}, static and dynamic performances.*

1. INTRODUCTION AND BACKGROUND CONCEPT

Between the two types of transistors, the bipolar devices (BJTs) are more temperature sensitivity and show large variations in the operating point with temperature fluctuations. The unipolar devices (FETs) are not so prone to instabilities due to temperature effects, but it is still needed to investigate the behaviour precisely the device performance when the transistor dimension enters in to nanometre scale. Because the physical, chemical, mechanical, thermal and optical properties of devices change significantly from those at larger scales.

From the basic operating principle point of view, a MOSFET is a voltage controlled majority carrier device. The movement of majority carriers is controlled by the voltage applied on the control electrode (called gate) which is insulated by a thin metal oxide layer from the bulk semiconductor body. The electric field produced by the gate voltage modulate the conductivity of the semiconductor material in the region between the main current carrying terminals called the Drain (D) and the Source (S) [1].

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Changes in temperature affect system speed, power, and reliability. This effect is caused by altering the threshold voltage (V_{th}), mobility (μ), and saturation velocity (V_{sat}) in the device. The resulting changes in device current can lead to failures [2]. V_{th}, μ, V_{sat} and supply voltage (V_{DD}) are all technology dependent parameters, with predicted values available down to the 22 nm node [ITRS]. Use of high-k dielectrics and metal gates to alleviate nanoscale gate leakage problems also alters V_{th}, μ and V_{sat}. The combination of these changes makes it difficult to determine the effect of temperature on the device performance [3]. The temperature effect is important to be considered because of thermal runaway. In the temperature dependence region, circuits continue to speed up as temperature increases. The higher temperatures could result in thermal runaway resulting from the exponential temperature dependence of leakage current, which may already be dominating the total power consumption in the nanoscale regime [4].

MOSFETs are widely used in the field of military, satellite communications, medical equipment, automobile, nuclear sectors, wireless and mobile communications, etc., as amplifier design, analog integrated circuits (ICs), digital CMOS design, mixed-signal ICs, power electronics and switching devices. As for demand in variety of applications and the use the nanoscale transistors, it is important to analyze the performances at a wide range of temperatures [5]. According to the literature, several technologies have been explored as an option for both low and high temperature operations. Few of them are Complementary Metal Oxide Semiconductor (CMOS), Silicon on Insulator (SOI) [6], and III-V semiconductors. The unwanted flow of high leakage current through the well junction and the presence of latch up puts a limit on the use of bulk CMOS devices at high temperatures. However, due to the absence of the well and latch up in SOI devices, it can be preferred for both low and high temperature operations [7]–[9].

Vadasz and Grove [10] reported the temperature dependence of bulk MOSFET at below saturation region. As for theoretical and experimental agreement, the variation of channel conductance with temperature is shown to be due to the variation of the threshold voltage and of the inversion layer mobility. Bipolar transistors are considered to be unusable at low temperatures as a consequence of strongly reduced current gain [11], [12]. Gaensslen et al. [13] presented an enhancement mode FET with a channel length of 1 μm suitable for operation at liquid nitrogen temperature. They claimed the performance of FET devices are significantly improved in terms of device turn-on time, 1.7 to 4 times higher transconductance, and an increasing threshold voltage at 77 K. Other advantages are a decrease of 1000 times inversion layer leakage currents, 6 times higher silicon thermal conductivity, and 6 times lower aluminium line resistance. There is no significant difference in temperature dependence of threshold voltage was observed between 'thick-film' SOI and bulk MOSFET's reported by Krull and Lee [14]. Groeseneken et al. [15] documented that, in thin-film SOI n-channel MOSFET's the device is fully depleted below a critical temperature and above**,** the device is no longer fully depleted.

The drain current I_D is influenced by two terms, i.e., channel mobility μ and threshold voltage V_{th} as [16]

$$I_D(T) \ \alpha \ \mu(T)[V_{GS} - V_{th}(T)] \tag{1}$$

The mobility term of (1) forces I_D to decrease, whereas the [V_{GS} - V_{th}] term increases I_D with increase in temperature. But the behaviour of I_D with temperature shows an opposite effect at a fixed gate bias voltage. The effect of two controlling terms of (4) is

nullified at a fixed value of bias voltage, which is defined as Zero Temperature Coefficient (*ZTC*) bias point. The so called *ZTC* point has been identified for bulk CMOS by Shoucair [17] and Prijic et al. [18], in both the linear and the saturation regions for temperatures between 27 ^{0}C and 200 ^{0}C. Later, Groeseneken et al. [15] and Jeon and Burk [9] demonstrated the existence of the *ZTC* point experimentally for thin and thick-film SOI MOSFETs, respectively [19]. Both experimental and analytical results for the *ZTC* point over a high temperature range (25^0 C-300^0 C) of a partially depleted (PD) SOI MOSFET has been introduced by Osman et al. [20]. They have identified two distinct temperature coefficient points, in the linear as well as in the saturation region. Tan et al. [16] have analysed the fully depleted (FD) and lightly doped enhanced SOI n-MOSFET over a wide range of operating temperature (300 K-600 K).

It is desirable to bias the digital and analog circuits meant for wide temperature applications at a point where the *V-I* characteristics show little or no variation with respect to temperature. This inflection point is typically known as temperature compensation point (*TCP*) or zero temperature coefficient (*ZTC*) [15], [18], [20]–[22].

2. ZTC BIAS POINT

There are two ZTC points for a transistor, one for the drain current and the other for the transconductance, and in general they have different values in linear and saturation regions. These ZTC points are defined as the points at which the drain current or the transconductance remains constant and independent of temperature. The ZTC points, are values of V_{GS} at which the reduction of the threshold voltage is counter-balanced by the reduction of the mobility, and as a result, the value of the drain current or the value of the transconductance remains constant as the temperature varies. For gate voltages lower than ZTC, the decrease of threshold voltage is dominant, as a matter of fact drain current increases with temperature, while for gate voltages higher than ZTC, the mobility degradation predominates and drain current decreases with temperature. The ZTC is a very important bias point for analog designers as it corresponds to a gate voltage at which the device DC performance remains constant with temperature [19], [23], [24].

3. SIGNIFICANCE OF ZTC BIAS

ZTC biasing is one of the important techniques in high temperature design especially for operational transconductance amplifier (OTA). The principal advantages of ZTC technique are [25]:

- It maintains a constant operating point over a wide range of temperatures so that no transistors operate out of saturation.
- It ensures stability of the circuit over a wide range of temperatures.
- Design simplicity and ensures reliable circuit operation when several stages are used.

It provides a bias point that is temperature independent. The main disadvantages of ZTC are: high overdrive voltage associated with *ZTC* bias results in reduced intrinsic gain due to the low g_m as well as reduced signal swing. The reduced g_m with temperature can affect the small signal performances of the amplifier like gain, bandwidth, etc., especially when the amplifier is required to operate over a wide range of temperatures.

The multi-gate structures like Double Gate (DG) MOSFET fabricated on SOI wafers is one of the most promising candidates due to its attractive features of low leakage current, high current drivability (I_{on}), transconductance (g_m), reduced short channel effects (SCEs), steeper subthreshold slopes, and suppression of latch-up phenomenon [26]–[31]. In a recent work [32]–[34], a detailed analysis of inflection point to examine its reliability issues over a wide range of temperature variations (100 K-400 K) for both analog and RF applications of DG MOSFET with HKMG technology was reported.

To pamper the market requisites, the density of transistors in a chip and the performance in terms of speed and power consumption are needed to be increased. The transistor miniaturization is one of the major concerns behind performance and cost. Undesirable short channel effects (SCEs) [35] and excessive V_{th} variation occurred beyond 32 nm technology node, hence there is searching for new technologies/methodologies. The new methodologies lead in two directions: one is the introduction of new materials into the classical single gate MOSFETs like develop uniaxial/biaxial strain in the channel region to enhance the carrier mobility in the channel region and implementation of high-k dielectric materials as gate oxide to minimize the gate leakage current. Second is the development of non-classical Multigate MOSFETs (Mug-FETs) which is a very good concept for further scaling of the device dimensions. So, the Integrated Device Manufacturer (IDM), foundries and electronic design automation (EDA) companies grant more investments with an emphasis on most promising 3-D FinFET technology. The advantages of FinFET technology are higher drain current and switching speed, less than half the dynamic power requirement with 90% less static leakage current [36], [37].

4. FINFET DESIGN

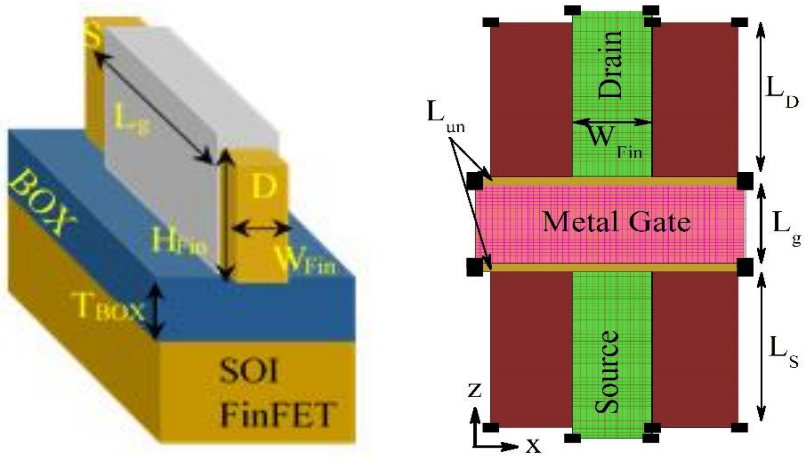

Fig. 1 (a) Perspective 3-D (b) 2-D cross sectional view of SOI FinFET

The geometrical process parameters of FinFETs are as:

- Gate length (L_g): the physical gate length of FinFETs.
- Fin height (H_{Fin}): the height of silicon fin.

- Fin width (W_{Fin}): the width of silicon fin.
- Gate oxide thickness (T_{ox}): the thickness of the gate oxide.
- Underlap channel length (L_{un}): the region under Si_3N_4 spacer.

Among all the parameters the H_{Fin} and W_{Fin} are the two which play a major role to be investigated. A tradeoff is required between the wider fin which results in unacceptable SCEs and narrower increases parasitic resistance and is hard to manufacture. Similarly from the manufacturing point of view, a taller fin achieves a better layout efficiency and higher current. So we have adopted various design parameters like W_{Fin}/L_g = 0.25, 0.5, 0.6, 0.8, 1 and H_{Fin}/L_g = 0.25, 0.6, 0.8, 1, 1.1, 1.3 in our simulation [38]–[40]. An n-channel MOSFET, having interfacial oxide as SiO_2 with high-k material (Si_3N_4) as spacer in the underlap regions (L_{un}) is modeled. The L_{un} is considered as 5 nm from both sides of the channel towards source and drain side. Fig. 1(a) and (b) show a three dimensional, as well as 2-D cross sectional view of the FinFET with Source/Drain length (L_S/L_D) as 40 nm. The source drain doping is Gaussian in nature with peak N_D at a density of 10^{20} cm^{-3}. The Equivalent Oxide Thickness (EOT) is 0.9 [39], [41], [42] nm and supply voltage V_{DD} = 0.7 V. The work function for the gate electrode is assumed to be 4.5 eV. The channel is undoped which augments the effective mobility, and hence the current density from the source [35].

5. Simulation Setup

The numerical simulation uses the drift diffusion approach [43], and the models activated in the simulation comprise a field dependent mobility, concentration dependent mobility and velocity saturation model. The technology parameters and the supply voltages employed for the device simulations are according to the analog ITRS roadmap [44] for below 50 nm gate length devices. The work functions of the metal gates are adjusted to achieve the desired V_{th} value. Physical models accounting for electric field dependence of mobility are invoked in the simulation. The inversion layer mobility models [45], along with Shockley–Read–Hall (SRH) [46], [47] and Auger recombination models are included. The inversion-layer Lombardi mobility model calculates the mobility degradation which normally occurs due to a higher surface scattering near the semiconductor to insulator interface which also includes Coulomb and phonon scattering. It deems the effect of transverse fields along with doping and temperature dependent parameters of mobility. The SRH and Auger recombination models are applied for minority carrier recombination. In addition, the basic mobility model is employed to consider the effect of doping dependence, high-field saturation (velocity saturation), and transverse field dependence. The impact ionization and band to band Augur recombination model are included in the simulation. The silicon band gap narrowing the model that sorts out the intrinsic carrier concentration is activated.

6. Effect of H_{FIN} and W_{FIN} on Scalability

In this section, the scalability of device is being discussed, the on-state drive current (I_{on}), and off-state leakage current (I_{off}). The variation of fin height (H_{Fin}) and fin thickness (W_{Fin}) on drain current is traced in Fig. 2(a) and (b) respectively. To analyze the immense improvement in g_m ($\partial I_D/\partial V_{GS}$) with increase in H_{Fin}/L_g ratio, we have appraised and studied the

I_D-V_{GS} curve. The Sub threshold Slope (*SS*) is an important parameter for calculating the off state current. Furthermore, SS is calculated as:

$$SS(mV/dec) = \frac{\partial V_{GS}}{\partial(\log I_D)} \tag{2}$$

$$I_D \alpha \exp(qV_{GS}/\eta kT) \tag{3}$$

Where, the logarithm is in base 10, I_D is the drain current, V_{GS} is the gate voltage, q is the charge of electron, k is the Boltzmann's constant, η is the body factor and T is the temperature. At room temperature (300 K) and ideal condition (η=1), the function $\exp(qV_{GS}/kT)$ changes by 10 for every 60 mV change in V_{GS}. The ideal value for the SS is 60 mV/decade.

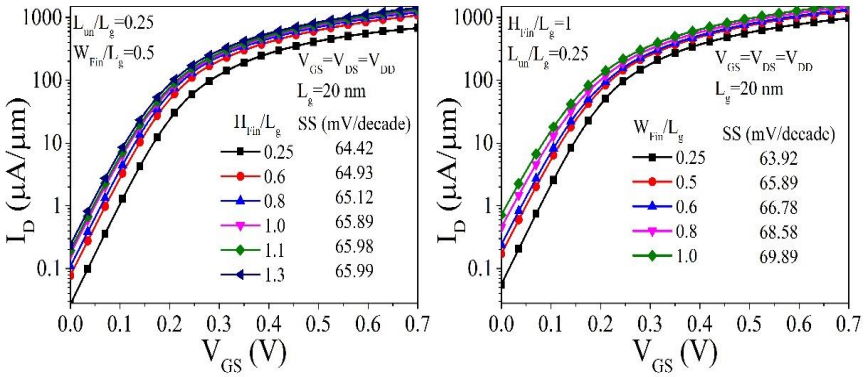

Fig. 2 Drain current (I_D) of the device in log scale as a function of gate to source voltage (V_{GS}) with variability of process parameter (a) H_{Fin} (b) W_{Fin}.

From Fig. 2(a), as H_{Fin}/L_g ratio increases, there is a lofty leakage current observed but with this SS also increases. However, with the same (high H_{Fin}/L_g ratio), parasitic resistance problem can be avoided, which further increases the drain current. Similarly, Fig. 2(b) demonstrates that the leakage current can be significantly reduced for lower W_{Fin}/L_g ratio cases. This is because by picking a smaller W_{Fin}, we can minimize the longitudinal electric field at the source side because of the precincts of multiple gates. From both figures, it can be noticed that SS augments with the increment in both ratios, i.e. H_{fin}/L_g and W_{fin}/L_g, although its value is very close to the ideal one, i.e. 60 mV/decade. The I_{on} and I_{off} are very much dependent on vital device geometry parameters, i.e. H_{Fin} and W_{Fin}. So, there is always an accord between I_{on} and I_{off} for the device design and device engineers can choose the optimum parameter dimensions as their requirement for specific applications.

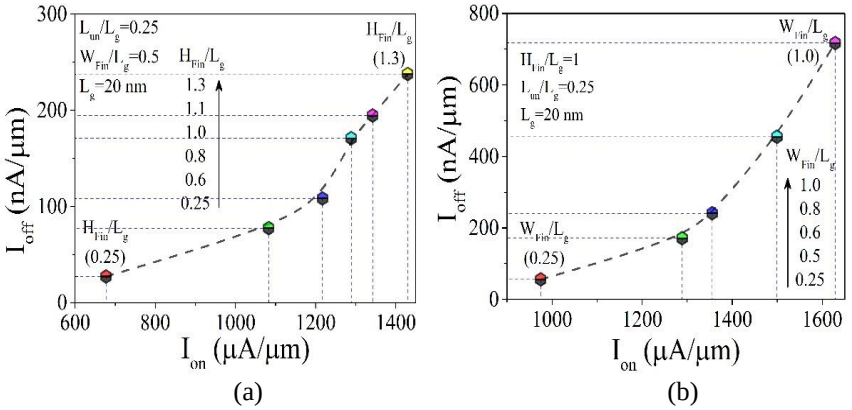

Fig. 3 On current (I_{on}) and leakage current (I_{off}) with variation of (a) H_{Fin} (b) W_{Fin} at V_{GS}= V_{DS}= V_{DD}.

The important figure of merit for digital application, i.e. I_{on} versus I_{off} for different H_{Fin}/L_g and W_{Fin}/L_g ratios is presented in Fig. 3(a) and (b). As for our previous discussion, both I_{on} and I_{off} increase with the increase in H_{Fin}. This is to confirm that for high drive current with matching the current drivability, taller fins are required, whereas narrow fins give better SCE immunity. This is because an increase in H_{Fin} results in decrease of the electric field in the silicon region which enhances carrier mobility and further the on state current. By comparing I_{on} and I_{off} for all H_{Fin}/L_g cases, we can say that H_{Fin} = 0.6 x L_g is the optimum one as it endues a moderate value for both I_{on} and I_{off}. Fig. 3(b) discussed the same I_{on} versus I_{off} benchmark for different W_{Fin}/L_g ratios. From the figure, a wider fin width (W_{Fin} = 1 x L_g) gives unacceptable SCEs, whereas a narrower fin width (W_{Fin} = 0.2 x L_g) is more difficult to fabricate. So, we can take the moderate one, i.e. W_{Fin} = 0.6 x L_g as the optimized W_{Fin}/L_g ratio.

6. Investigation of Analog Performance with Variation of Temperature

Temperature dependency of the I_D is influenced by V_{th} as (1), the mobility term (which is hampered due to scattering effects at high T) of (1) forces I_D to decrease, whereas the [V_{GS} - V_{th}] term (improves at higher T as V_{th} decreases) increases I_D with increase in temperature. But the behaviour of I_D with T shows just adverse response at a fixed gate bias voltage. The effects of two controlling terms of (1) are nullified at a fixed value of bias voltage, that the inflection point is called temperature compensation point (*TCP*). Fig. 4(a) shows the variations of I_D with V_{GS} at different bias temperatures. As for equation (1) at high gate bias, $\mu(T)$ dominates because of the heavy lattice scattering at higher T. It leads to a reduction in the channel mobility which further reduces I_D. At low gate bias, [V_{GS} - V_{th}] term influences I_D to raise because of the shrinking nature of V_{th} with an increase in T. These two opposite effects cancel out each other at a value of V_{GS} where I_D shows minimal fluctuation with T. This inflection point as shown in Fig. 4(a) is imminent in between V_{GS} = 0.34 V. This creates an opportunity to use multigate MOSFETs for integrated circuit applications.

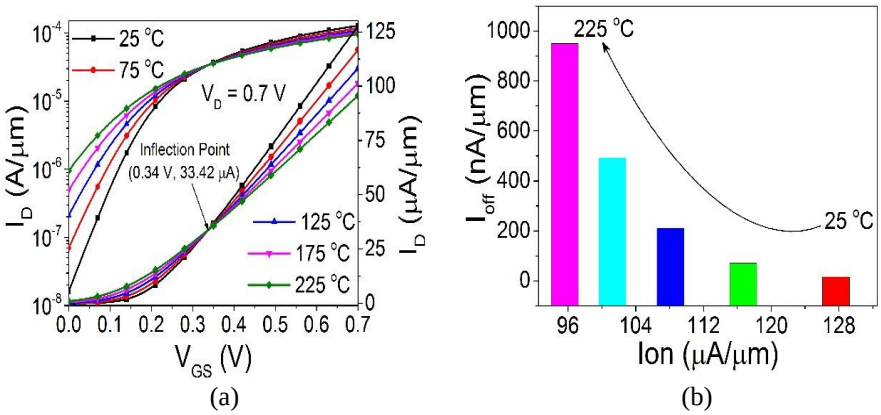

Fig. 4 (a) Drain current (I_D) as function of Gate Voltage (V_{GS}) both in linear and log scale (b) leakage current (I_{off}) versus On current (I_{on}) with variation of temperature.

Fig. 4(b) presents a plot for the important parameters which includes the variation of I_{on}, I_{off} for different temperatures. From the figure, it can be observed that the behaviour of I_{on} and I_{off} is absolutely opposite to each other with temperature variation. For high T values, the device shows a fairly large I_{off} and low I_{on}, which is just reverse in the case of low T. This is because, as temperature increases, the mobility of carrier's decreases due to scattering effects which further reduce I_{on}. Again the degradation in I_{off} at high temperatures is due to the lattice vibration and the phonon scattering phenomena play a significant role as T increases.

The g_m-V_{GS} plot can simply be obtained by taking the derivative of I_D with respect to V_{GS}. At $V_{GS} < V_{th}$, the channel is weakly inverted and I_D is due to diffusion. The diffusion current increases with T because of the increase in intrinsic carrier concentration as in Einstein's relation: $D = \mu k_B T$, where D is the diffusion constant, μ stands for mobility, k_B is Boltzmann's constant and T represents temperature. At $V_{GS} > V_{th}$, the value of g_m decreases with T due to the mobility degradation. The reduction in V_{th} with temperature enhances g_m, however the degradation of mobility reduces g_m. These two phenomena influence each other to give rise for a temperature compensation point for g_m. From Fig. 5 (a), we can conclude that the value of transconductance *ZTC* point (0.14 V) is lower than the drain current *ZTC* bias point (0.34 V). The inflection point for I_D and g_m are two important FOM in analog circuit design for both high and low temperature applications. In OPAMP (operational amplifier) based circuit design and transistors used in biasing string can be biased at inflection point for drain current to maintain a constant DC current level. The input devices may be biased at an inflection point for transconductance to achieve stable circuit parameters. The above said points are obtained for constant bias conditions in case of floating body or body tied configuration MOSFETs. Hence there is only one possibility to bias the transistor, i.e. either at inflection point for I_D or g_m. Moreover, this point is usually affected by process variations. Hence, depending upon the nature of applications, the bias conditions are picked accordingly.

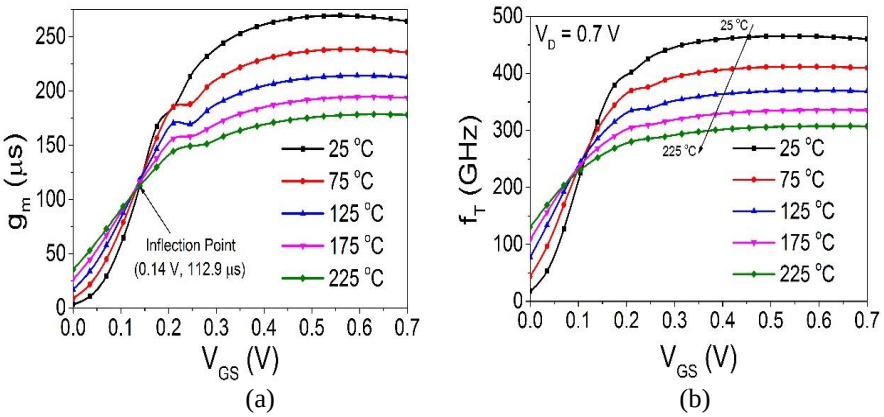

Fig. 5 (a) Transconductance (g_m) and (b) Cut off frequency (f_T) as a function of Gate Voltage (V_{GS}) with variation of temperature.

Cut-off frequency (f_T) plays a vital role in evaluating the RF performance of the device plotted in Fig. 6. Generally, f_T is the frequency at which the current gain is unity [42].

$$f_T = \frac{g_m}{2\pi C_{gg}} \tag{4}$$

Where g_m, and C_{gg} are the transconductance, total gate capacitance respectively. The enhancement in f_T occurs at higher drive current and lower T values. This improvement in f_T is partially due to the increment in g_m and merely because of the low values of intrinsic capacitance. At low temperature, the improvement of cut-off frequency f_T is due to a steep increase in mobility and in turn g_m. In addition, it reveals the advantage of the multigate technology which exhibits *ZTC* bias points over a wide range of temperatures (T=25 °C to 225 °C).

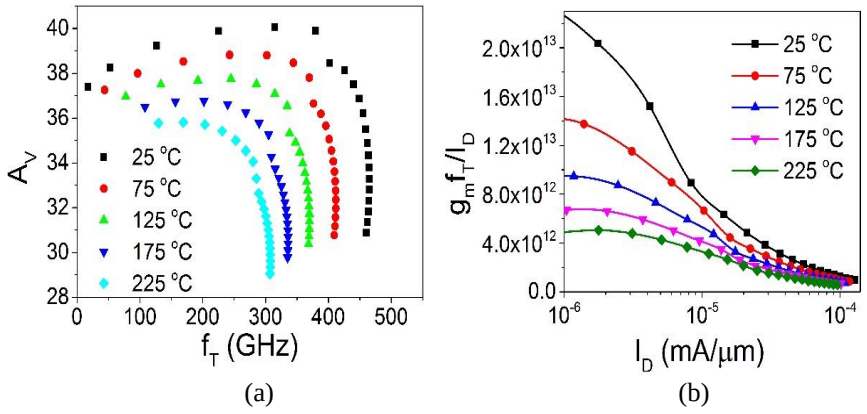

Fig. 6 (a) Intrinsic Gain (A_V) versus Cut off frequency (f_T) (b) Sweet Spot as a function of Drain Current (I_D) with variation of temperature.

The intrinsic gain ($A_V = g_m/g_d$) is a valuable FOM for operational transconductance amplifier (OTA) and is shown in Fig. 6 (a). From the graph, a similar type of analysis can be made as in the case of g_m and g_d. From the figure, a high gain can be obtained for high temperatures in the subthreshold region and the reverse effect in super threshold region. Fig. 6(b) presents one crucial parameter for analog/RF application, i.e. the 'sweet spot' (settlement among power, speed of operation and linearity), which is signified by the peak of transconductance to the current ratio (g_m/I_D) and cut-off frequency (f_T) product. The variation of the 'sweet spot' with I_D for a broad range of T (25 ^{0}C to 225 ^{0}C) is well examined from Fig. 6(b). The device predicts pretty higher $g_m f_T/I_D$ values at low T and gradually starts decaying with the increase in T.

The extracted static parameters like I_{on}, I_{off}, I_{on}/I_{off}, and power dissipation ($P_D=I_{off}*V_{DD}$) for a wide range of T variation are arranged in Table 1. All the parameters predict significant improvements in the lower range of T values. The performances start deteriorating as T increases. There is a 77.04% enhancement in I_{off}, 79.01% improvement in on-off ratio, and 77.04% in P_D, while T steps down from 75 ^{0}C to 225 ^{0}C.

Table 1 Static performance of FinFET with T variation

Temp. (^{0}C)	I_{on} (μA)	I_{off} (nA)	I_{on}/I_{off}	PD ($I_{off}*V_{DD}$) (W) x10^{-8}
25	128	16.03	7961.96	1.122
75	117	69.83	1670.96	4.888
125	108	211.01	512.33	14.77
175	101	492.53	205.52	34.47
225	95.6	950.03	100.64	66.50

In a similar fashion, Table 2 reveals the dynamic analysis of FinFET towards temperature sensitivity. The performances like f_T, 'sweet spot', energy, and *EDP* are exported and compared for different temperatures. Alike the above discussed static performances, the dynamic parameters are also depict numerous enhancements at detrimental temperatures.

Table 2 AC/Dynamic performance of FinFET for different values of T

Temp. (^{0}C)	C_{gg} (F) x10^{-18}	Peak f_T (GHz)	Sweet Spot (THz/V)	Delay (CV/I_{eff}) (ps)	Energy (CV^2) (J) x10^{-18}	EDP (Js) x10^{-29}
25	92.236	465	23.5	0.506	45.195	2.29
75	92.178	412	13.8	0.553	45.167	2.5
125	92.217	370	9.47	0.597	45.186	2.7
175	92.325	336	6.7	0.638	45.239	2.89
225	92.422	308	5.05	0.677	45.286	3.06

7. CONCLUSION

The DC characteristics of a 20 nm n-channel FinFET for variation in fin width and fin height are carried out using Sentaurus device simulator. From the results obtained by geometrical parameter variation, we can say that taller fins are required for higher current

drivability and narrower fins are required for higher immunization to SCEs. W_{Fin} = 0.6 x L_g and H_{Fin} = 0.8 x L_g cases show the desired device performances in terms of I_{on}, I_{off}. When developing novel architectures to enable further miniaturization to meet the ITRS requirements, the evaluation of *ZTC*/*TCP* is one of the key analysis for optimal device operation and reliability. We have systematically analyzed the sensitivity of various FinFET performances towards temperature variation. From the presented outcomes of this work, it is evident that there exist different inflection points for I_D, and g_m, which should be seriously taken into consideration for FinFET based circuit operation.

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