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FLASH MEMORY DEVICES WITH METAL FLOATING GATE/METAL NANOCRYSTALS AS THE CHARGE STORAGE LAYER: A STATUS REVIEW

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Abstract. *Traditional flash memory devices consist of Polysilicon Control Gate (CG) – Oxide-Nitride-Oxide (ONO - Interpoly Dielectric) – Polysilicon Floating Gate (FG) – Silicon Oxide (Tunnel dielectric) – Substrate. The dielectrics have to be scaled down considerably in order to meet the escalating demand for lower write/erase voltages and higher density of cells. But as the floating gate dimensions are scaled down the charge stored in the floating gate leak out more easily via thin tunneling oxide below the floating gate which causes serious reliability issues and the whole amount of stored charge carrying information can be lost. The possible route to eliminate this problem is to use high-k based interpoly dielectric and to replace the polysilicon floating gate with a metal floating gate. At larger physical thickness, these materials have similar capacitance value hence avoiding tunneling effect. Discrete nanocrystal memory has also been proposed to solve this problem. Due to its high operation speed, excellent scalability and higher reliability it has been shown as a promising candidate for future non-volatile memory applications. This review paper focuses on the recent efforts and research activities related to the fabrication and characterization of non-volatile memory device with metal floating gate/metal nanocrystals as the charge storage layer.*

Key words: *Metal oxide semiconductor (MOS), non-volatile memory (NVM), nanocrystal (NC), dielectrics, interpoly dielectric (IPD), floating gate (FG)*

1. INTRODUCTION

Flash memory is the extensively used non-volatile information-storage device today because of its multi-bit per cell storage property and lesser cost per bit. Moreover its fabrication process is consistent with the present CMOS process and is a relevant solution for embedded memory applications. The qualitative comparison of various non-volatile MOS memory devices in the flexibility-cost plane [1] is shown in Fig.1. NOR flash memory and NAND flash memory are the two main types of flash memory used today. The key difference between the two is that NOR flash memory allow a single byte

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to be written to an erased location or read independently where as NAND flash memory is written in blocks or pages. The other contrast is that the former uses channel hot electron (CHE) for programming and has slower program-erase speed while the later uses fowler-nordheim tunneling for programming and has fast program-erase speed.

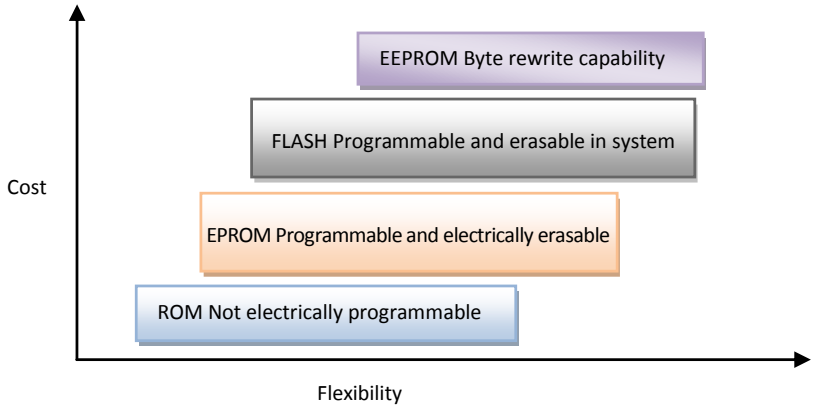

Fig. 1 Non-volatile MOS memory qualitative comparison in the flexibility-cost plane [1]

NAND flash memory finds use in data storage devices like mobile phones, pen drives, digital cameras etc. and the NAND flash based solid state drive (SSD) is used as a replacement for hard disk drive (HDD) in modern computers and laptops. The growing demand for this technology is the key driving force to increase the data storage capacity and decrease the cost per bit in flash memories by scaling down the flash cell to smaller and smaller dimensions. In continual scaling the major roadblocks are being faced by both NOR and NAND flash memories. The scaling projection for floating-gate NOR and NAND flash memory by International Technology Roadmap for Semiconductors (ITRS) [2] is shown widely in Table 1 and 2. MOS memory devices rely on the charge stored in the floating gate to cause a shift in the threshold/flatband voltage. The schematic cross section of a floating-gate MOS memory cell is shown in Fig.2.

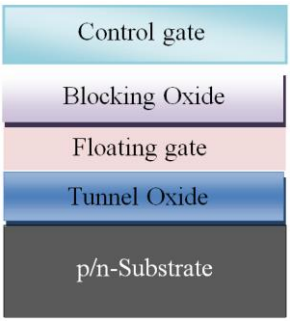

Fig. 2 Schematic cross section of MOS memory cell

Conventionally, the floating gate and control gate are usually made of Polysilicon. The tunneling barrier and the blocking oxide are typically composed of SiO_2 and oxide-nitride-oxide (ONO) respectively. Floating gate acts as a potential well and once the charges are injected into the potential well, it cannot move without external electric field. The programming and erasing of the memory cell is carried out by applying positive and negative electric field to the control gate respectively. Si has been used in MOS technology for many decades because of the better qualities of its native oxide [3]. In advanced semiconductor technology, the transistor gate length will continue to shrink in order to achieve faster switching speed and high device density. This results in reduction of gate length and gate oxide thickness to 1.5nm and oxide scaling down to EOT of approx. 0.5nm is required [4]. As the thickness of SiO_2 shrinks below 1.5nm, it is facing its physical limitations because of gate dielectric leakage current and reliability requirements [5]. Thus there is a need for alternate channel materials that can enhance channel mobility beyond the physical limits of Si based MOS devices [6]. With the decrease in thickness of tunnel dielectric, the interface between Si and SiO_2 plays a very important role in retaining the charge for the long time. However, for a very thin SiO_2, it is impossible to have a defect free oxide and even a single defect can cause leakage of charge stored in floating gate through the tunnel oxide. Thus, thinner tunnel dielectric would degrade the charge retention. For instance, with 2.3 nm SiO_2 tunneling oxide shows reasonable programming efficiency with fairly low programming voltage, but loose 25% of its stored charges in several tens of seconds [7]. To overcome these issues, SiON (Silicon oxynitride) and other high dielectric constant materials with higher physical thickness are being used to limit the leakage current while maintaining the higher capacitance values of the scaled devices. SiON has been used as a substitute for SiO_2 because of its high dielectric permittivity and low density of surface states. In addition, by differing O/N ratio the band energy of SiON can be tailored between 5 and 9 eV [8, 9]. The tunnel oxide has the most strict requirements in a flash cell with properties summarized as under: a) It must provide a good interface to the silicon channel for reliable transistor operation b) It should provide efficient charge transport either through tunneling or hot carrier injection during the programming and erase operations which allow the data to be changed in the memory cell c) It should enable years of charge retention on the floating gate [10]. The conventional polysilicon floating gate structure suffers from various disadvantages like cell to cell interference when optimized for high density, high leakage current through tunneling dielectric, programming current become increasingly ballistic and loss of gate coupling factor. The thickness of ONO is to be reduced to compensate for the loss of gate coupling factor. But when it is reduced below 10nm, it would cause increase in the unwanted gate to gate tunneling and degrade the retention characteristics of memory devices. The possible route to eliminate this problem is to use high-k based interpoly dielectric and to replace the polysilicon floating gate with a metal floating gate. The added benefits of incorporating a metal floating gate include work function tunability, higher density of states and most importantly the lower ballistic transport. The lower ballistic transport in case of metals is a beneficial factor in scaling down the floating gate thickness to realize a lower cell-to-cell interference [11]. Hf based high-k dielectrics in combination with metal floating gate demonstrated excellent memory characteristics [12]. Therefore, the ultra-thin metal floating gate is a promising candidate for future scaled NOR and NAND FLASH memories.

Table 1 Scaling projections for floating-gate NOR flash by International Technology Roadmap for Semiconductors (ITRS) [2]

NOR Flash	NOR Flash Technology node-F (nm)	Gate length Physical (nm)	Tunnel oxide thickness (nm)	Interpoly Dielectric material	Interpoly dielectric thickness EOT (nm)	Gate Coupling Ratio	Retention (years)
2011	40	100	8-9	ONO	13-15	0.6-0.7	10-20
2012	35	100	8-9	ONO	13-15	0.6-0.7	10-20
2013	32	90	8	High-k	8-10	0.6-0.7	20
2014	28	90	8	High-k	8-10	0.6-0.7	20
2015	25	90	8	High-k	8-10	0.6-0.7	20
2016	22	(?)	(?)	High-k	8-10	0.6-0.7	20
2017	20	(?)	(?)	High-k	8-10	0.6-0.7	20
2018	28	(?)	(?)	High-k	7-9	0.6-0.7	20
2019	16	(?)	(?)	High-k	6-8	0.6-0.7	20
2020	14	(?)	(?)	High-k	6-8	0.6-0.7	20
2021	12	(?)	(?)	High-k	6-8	0.6-0.7	20
2022	10	(?)	(?)	High-k	6-8	0.6-0.7	20
2023	10	(?)	(?)	High-k	6-8	0.6-0.7	20
2024	10	(?)	(?)	High-k	6-8	0.6-0.7	20

Table 2 Scaling projections for floating-gate NAND flash by International Technology Roadmap for Semiconductors (ITRS) [2]

NAND Flash	NAND Flash Technology node-F (nm)	Tunnel oxide thickness (nm)	Interpoly Dielectric material	Interpoly dielectric thickness EOT (nm)	Control gate material	Gate Coupling Ratio	Retention (years)
2011	28	6-7	ONO	10-13	n-poly	0.6-0.7	10-20
2012	25	6-7	High-k	9-10	Poly/metal	0.6-0.7	10-20
2013	22	6-7	High-k	9-10	Poly/metal	0.6-0.7	10-20
2014	20	6-7	High-k	9-10	Poly/metal	0.6-0.7	10
2015	19	6-7	High-k	9-10	metal	0.6-0.7	5-10
2016	18	4	High-k	9-10	metal	0.6-0.7	5-10
2017	16	4	High-k	9-10	metal	0.6-0.7	5-10
2018	14	4	High-k	9-10	metal	0.6-0.7	5-10
2019	13	4	High-k	8-10	metal	0.6-0.7	5-10
2020	12	4	High-k	8-10	metal	0.6-0.7	5-10
2021	11	4	High-k	8-10	metal	0.6-0.7	5-10
2022	9	4	High-k	8-10	metal	0.6-0.7	5-10
2023	8	4	High-k	8-10	metal	0.6-0.7	5-10
2024	8	4	High-k	8-10	metal	0.6-0.7	5-10

Initially in 1967, Charge-trapping memory (CTM) was introduced to illustrate some eminent advantages over the conventional floating-gate counterpart [13]. Recently, floating gate memory devices consisting of discrete metal nanocrystals have received huge attention due to their excellent memory performance and high scalability. Memory devices with nanocrystal floating-gate offer faster write/erase speeds, lower power

consumption, and more powerful endurance characteristics compared to conventional continuous floating-gate nonvolatile memory devices. During the last few years, Si and Ge nanocrystals embedded in gate oxide layers have been studied as the charge storage nodes in Silicon-based memory devices. But it has been found that during the device fabrication their retention characteristics are very sensitive to the thermal process because of the existence of defects and traps inside or at the surface of the nanocrystals. The presence of these defects and traps limits the application of Si and Ge nanocrystals in nonvolatile memory. Thus the use of metal nanoparticles has been proposed to prolong the retention characteristics and to overcome the limits of semiconductor nanocrystals [14]. The fabrication of a discrete non volatile memory (NVM) cell requires a perfect control of four main parameters: (a) the tunnel oxide thickness (b) the nanocrystal density (c) the nanocrystal diameter and (d) the control oxide thickness. The most commonly used methods to fabricate nanocrystals are self-assembly, precipitation and chemical reaction. In self assembly procedure, a trapping layer of 1 – 5 nm is deposited and then the film is annealed at a temperature close to its eutectic temperature in an inert gas ambient to transform the trapping layer into a nanocrystal structure. The diameter of the nanocrystal depends on the thickness of the trapping layer as well as the temperature and duration of the thermal treatment. However this method cannot make sure that the trapping layer is completely discrete. In precipitation method, an oversaturated or mixed trapping layer is prepared by ion implantation into a deposited insulator layer or co-deposit system to form nanocrystals by further thermal annealing. However, this method has also some limitations due to use of high energy ion implantation for formation of nanocrystals. The chemical reaction method is most widely used to form a nanocrystal trapping layer. Initially, a binary or tertiary mixed layer is co-deposited by different material systems and then the layer is oxidized by RTA under an oxygen flow. But the control of the oxygen concentration in the mixed layer is an important issue. A low oxygen concentration causes insufficient oxidation of the mixed layer and higher leakage current and a high oxygen concentration can result in the oxidation of the nanocrystal. The memory property can be lost if either of these two conditions occur. A metallic nanocrystal storage layer has several advantages over the semiconductor nanocrystal storage layer due to their high density of states and work function engineering. The large work function difference between the metal and the Si substrate creates a deep potential well that ensures a lesser charge loss ultimately resulting in enhancement of the retention characteristics. Blocking layers comprised of high-k dielectrics allow the use of relatively thick films which prevent leakages while maintaining a thin equivalent oxide thickness (EOT) and prevent any charge leakage to the top gate. Moreover, the increased capacitance density offered by high-k films enlarges the charge storage density. Fig. 3 shows the schematic diagram enlightening the motivation and challenges in transitioning from conventional memory structure to a novel high-k MOS memory structure.

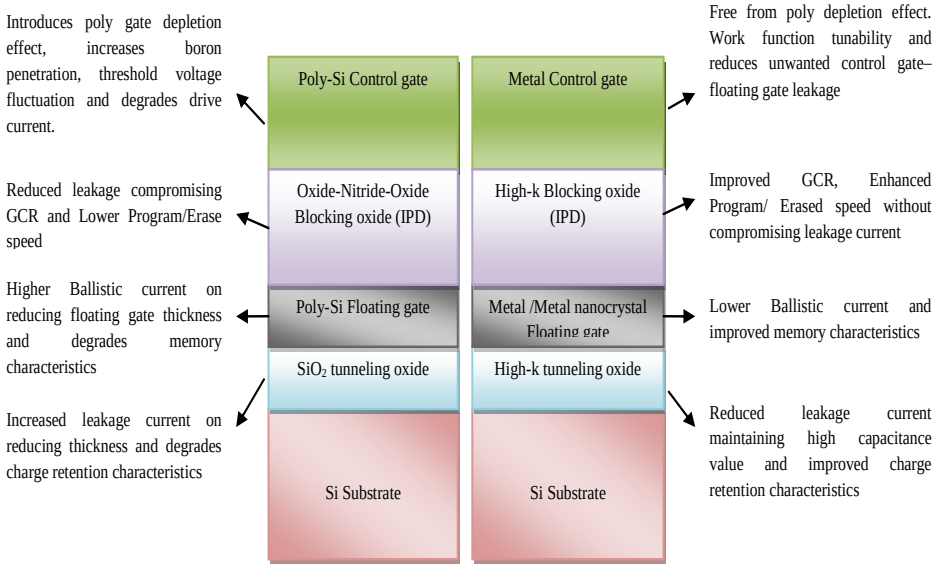

Fig. 3 Schematic diagram showing the comparison between conventional and novel high-k MOS memory structure

2. Related Work to Non-Volatile Memory Structures Using Different Metal Nanocrystals/Metal Floating Gate

Self-assembly of metal nanocrystals including Au, Ag, and Pt on ultrathin oxide for nonvolatile memory applications were investigated [15] and it was observed that for non volatile memory cells spherical nanocrystals are preferred because the three dimensional symmetry results in the best charge confinement and physical stability from surface energy minimization. The shallow potential well in case of semiconductor nanocrystals (Si nanocrystals paired with a Si substrate) can only hold charges for a relatively short time because of direct-tunneling back to the substrate [16]. However, metal nanocrystals due to their large work functions can make use of the deep potential wells to hold electrons for longer time and thus the memory effects of Au and Pt are better than the Ag. Chungho Lee et. al. [17] in 2005 fabricated and characterized the heterogeneous-stack devices consisting of metal nanocrystals (Au) and silicon nitride (Si_3N_4). The metal nanocrystals at the lower stack allow the direct tunneling mechanism during program/erase to achieve low-voltage operation and good endurance while the nitride layer at the upper stack acts as an additional charge trap layer to increase the memory window and significantly improve the retention time. Semiconductor nanocrystal (Si) and nitride heterogeneous stacks have been first proposed in metal–nitride–oxide–silicon (MNOS) structure by Yamazaki et al. [18, 19] and SONOS structure by Steimle et al. [20, 21]. The nanocrystal/nitride heterogeneous stack shows enlarged charge storage capacity, longer retention, low voltage and fast P/E by additional nitride traps as compared to Au nanocrystals. Ch Sargentis et. al [22] in 2005 fabricated a novel MOS memory device with platinum (Pt) nanoparticles embedded in the HfO_2 /SiO_2 interface which exhibits

clear hysteresis behavior and is attributed to the charge storage in the nanoparticles. Jong Jin Lee and Dim-Lee Kwong [23] in 2005 proposed a nonvolatile memory using nickel nanocrystal (NC) embedded in HfO_2 tunneling/control dielectrics to overcome the fundamental tradeoff between programming and data retention characteristics. Nickel has not only suitable work function (4.5–4.6 eV) [24] for such applications but it also exhibits a low anneal temperature for NC formation which is advantageous to the quality of underlying tunneling HfO_2 dielectrics (5.1nm). Hei Wong and Hiroshi Iwai in 2006 [25] suggested that the conventional oxide can be scaled down to two atomic layers of about 7A ˚ but this is not viable in practice because of the non-scalabilities of interface, trap capture cross-section, leakage current and the statistical parameters of fabrication processes. Physically thicker high-k material can help to solve most of the problems but high-k gate dielectric film still give rise to several reliability problems and degrades the performances of the MOS devices to a great extent. Bulk oxynitride/high-k stack could be a secure solution to this problem. The major benefits of oxynitride are that most of its material characteristics are second to SiO_2 but with a larger value of dielectric constant (3.9-7.8), band gap within 5.9–8.9 eV, conduction band offset greater than 2.1 eV, thermally stable structure with high crystallization temperature and stable on silicon. It also has a comparatively better dielectric/Si interface when compared to other high-k competitors. These properties are sufficient for MOS device applications. But the two atomic-layer oxynitride will not be synthesized and the leakage current will be too large as well. Therefore, a better solution is to make use of the bulk oxynitride/high-k stack to make it physically thicker and thus reduce the gate tunneling current and the sensitivity to thickness fluctuation. Due to the fabrication methods, most of the defects in oxynitride are tied to the hydrogen and hydroxyl groups and are the major sources for hot-carrier induced related trap generation in nitrided oxide films [26-29]. Hence it is very important to minimize the hydrogen incorporation for a highly reliable oxynitride film for advanced MOS device applications. S. Hwang et. al [30] in 2007 studied the effect of the presence of high concentration of nitrogen in silicon-oxide layer. The results reveal the suitability of oxynitride films in high quality ultra-thin-film transistors and non volatile memory device. P.H. Yeh et. al. [31] in 2007 review the memory effects of the Ni, $NiSi_2$, $CoSi_2$ and $NiSi_2$ with SiO_2/HfO_2 tunneling dielectrics. It was found that the memory effects of the metal nanocrystals have strong relationship with the work function and the work function can be modulated by changing the metal species. The memory window of the samples with HfO_2 as tunnel dielectric is larger than the samples with SiO_2 due to the smaller voltage drop with the same physical thickness(=3nm). The physical thickness of HfO_2 tunnel oxide is sufficient for the small operation voltage but not satisfactory for the retention requirement because the equivalent oxide thickness (1.5 nm) being too thin so that the electrons can tunnel back easily. The tunneling probability of electron is interrelated with the thickness and the barrier of the tunnel dielectric. Weihua Guan et. al. [32] in 2007 proposed that metal nanocrystal (MNC) shows better retention performance than SNC (semiconductor nanocrystals) for the same nanocrystal size because of the higher electron barrier height from MNC to the substrate and the weaker quantum confinement effect of MNC. A tunneling oxide of 3.6 nm is thick enough to guarantee 10 years retention for Au nanocrystal. It is also observed that high-k tunneling barrier combined with high work function MNC (e.g.NC- Au) can further enhance the retention performance. Therefore, metal nanocrystal memory devices employing high–k gate dielectric is a promising

candidate for the application of non-volatile memories. Again, Weihua Guan et. al. [33] in 2007 fabricated MOS capacitor structure with metal nanocrystals (including Au, Ni and Co formed by self-assembling process) embedded in the gate oxide for nonvolatile memory (NVM) application. Due to high work function (5.0 eV) Au nanocrystals can provide enhanced retention performance which confirms the high capacity of Au nanocrystals for NVM applications with respect to semiconductor counterparts. Jae-Young Choi et. al. [34] in 2007 fabricated nonvolatile memory (NVM) MOS capacitors with a structure of Si/SiO_2/Ni NCs/SiO_2/Al_2O_3. The MOS memory structures with the Ni-NC floating gates showed a relatively large memory window of 3 – 5 V for 10 ms – 1 s under ±19 V and excellent endurance characteristics. Byoungjun Park et. al. [14] in 2008 studied the electrical characteristics of titanium (Ti) nanoparticles embedded metal-oxide-semiconductor (MOS) capacitors and metal-oxide-semiconductor field effect transistors (MOSFETs) with blocking Al_2O_3 layer(~20 nm) and tunneling SiO_2 (~6.3 nm)layer. Due to work function of 4.3 eV Ti nanoparticles shows potential for charge storage nodes in floating gate devices because during their formation their surfaces are natively covered with a titanium dioxide (TiO_2) layer which are known as a high-k dielectric material (ε = 80~110) and it can avert the lateral transportation of charge carriers between the Ti nanoparticles and blocking oxide layers and the charge loss through the tunneling barrier. Yingtao Li and Su Liu [35] in 2009 used the different work function NC materials (Au~5.0ev, W~4.6ev and Si~4.05ev) in NVM devices and observed that Au-NC as floating gates exhibit better retention characteristics due to its larger work function which induces a higher barrier height and a deeper well at the interface of the floating gate and the tunneling dielectric. The work function values for some important transition metals are listed in Table 3. Ni Henan et. al. [36] in 2009 fabricated and characterized the MOS structure with double-layer heterogeneous nanocrystals (Si nanocrystals and Ni nanocrystals) embedded in a gate oxide (SiO_2) matrix for nonvolatile memory applications. The additional metal nanocrystals layer allows the direct tunneling mechanism to raise the flat voltage shift and prolong the retention time. Coulomb blockade and energy level quantization limits the leakage mechanism that is tunneling to the closest lower nanocrystals [37]. Zs. J. Horvath and P. Basa [38] in 2009 created MNOS structures with semiconductor nanocrystals at the Si_3N_4/SiO_2 interface and summarized that the formation of nanocrystals in nitride based memory structures can enhance both the charging and retention behaviour due to direct tunneling to nanocrystals and creating deep energy states respectively [39,40]. Jeng Hwa Liao et. al. [41] investigated the relationship between the physical and the electrical characteristics of silicon oxynitride (SiON) films and the refractive index. It was found that the charge-trap density of the SiON film is inversely proportional to the oxygen concentration in the SiON layers and the dielectric constant is directly proportional to the refractive index. S. Raghunathan et. al. [11] in 2009 investigated that during programming ultra-thin metal FG shown three orders of magnitude lesser ballistic current than poly-Si of same thickness because the metal has high density of states and larger the density of states the larger is the scattering. It was also observed that the deeper work-function metal FG device erases slower but shows better retention compared to a shallower work-function FG device. Srikant Jayanti et. al. [12] in 2010 investigated ultrathin TaN metal floating gate with Hf based high-k IPD for NAND Flash applications. The results indicate that high-k based interpoly dielectric in combination with ultra-thin TaN metal FG can enable further scaling of NAND Flash memory beyond

conventional oxide-nitride-oxide (ONO) based IPD technology. Jang-Sik Lee [42] in 2010 reviewed gold nanoparticles are chemically stable and have a high work function, they have been shown to be a promising candidate for use as the charge trapping element in non-volatile memory devices employing nanoparticles. Shiqian Yang et. al. [43] in 2010 fabricated MOS capacitor (p-Si/SiO_2/TiW NCs/Al_2O_3/Al) and illustrate that high-k blocking oxide play vital role in the low-voltage operation and increases the coupling ratio to the NC layer which results in good charge storage feature. V. Mikhelashvili et. al. [44] in 2010 proposed and demonstrated a double-layer memory capacitor comprising of two Au nanoparticle layers separated by HfO_2 film. HfO_2 was also used for the tunneling layer whereas the blocking insulator was based on a HfN/HfTiO multilayer stack having a dielectric constant larger than 35. The structure exhibits excellent performance in terms of the hysteresis window, the stored charge density, the leakage current, the EOT and its retention properties. G. Gay et. al. [45] in 2010 fabricated the devices with TiN NCs embedded in SiN and observed that the devices were erased 10^2 faster and shows large memory window (10 V) as compared to devices with pure SiN trapping layer. Larysa Khomenkova et. al. [46] in 2011 demonstrated the application of pure HfO_2 and HfSiO layers fabricated by RF magnetron sputtering as alternative tunnel layers for high-k/Si-NCs-SiO_2/SiO_2 memory structures and indicates the utility of these stack structures for low-operating-voltage NVM devices with specific deposition conditions and annealing treatment. G. X. Li [47] et. al. in 2011 demonstrated that Hf-rich films tend to form thicker interfacial layer due to the stability of HfO_2 whereas Ti-rich films usually demonstrate higher leakage current owing to the low band gap of TiO_2. Overall, the 20-nm-thick films with Hf/Ti ratio of 46/54 exhibit high permittivity up to 50 while maintaining the relatively low leakage current of 1.2×10^{-8} A/cm^2 at 1 V bias which would be the promising candidate to replace HfO_2 for the next generation technology. Minseong Yun [48] et. al. in 2012 demonstrated high density multi-layer Pt nanoparticle embedded memory device with enhanced memory window and better retention property. Chih-Ting Lin et. al. [49] in 2013 revealed that the memory window becomes larger at elevated annealing temperatures due to the high density of Au-NCs. The optimized annealing condition was 700^0C because of the large space between NCs. Jun-Hyuk Seo et. al. [50] in 2013 fabricated a MOS capacitor containing Au nanocrystals in a stepped HfO_2 and SiO_2 tunneling oxide matrix. Memory window effects were observed due to the successive charge trapping in Au nanocrystals by controlling the electric field distribution via the tunneling oxide. Wen-Chieh Shih et. al. [51] in 2013 studied MYTOS device i.e metal-yttrium oxide-tantalum oxide-silicon oxide-silicon (Al/Y_2O_3/Ta_2O_5/SiO_2/Si) and showed that the large conduction band offset at the Ta_2O_5/SiO_2 and the Y_2O_3/Ta_2O_5 interfaces is expected to give better blocking efficiency which will improve memory window and programming speed and can also relieve over erase problem. Guoxing Chen et. al. [52] in 2014 demonstrated that metal floating gate capacitor Si/SiO_2-2.7/HfO_2-8/TaN-8/Al_2O_3-15/Au-150 presents favorable performance with lower operation voltage as well as enhanced program/erase speed and improvement of data retention compared to Si/SiO_2-4.5/TaN-8/Al_2O_3-15/Au-150 floating gate cell. Thus, the program/erase speed can be enhanced using a high-k blocking layer. Metal oxides shows potential for the high-k gate materials because of chemical stability at Si interface. Table 4 shows the contrast of a few main properties of high-k dielectric materials [53]. High-k dielectrics proportionally reduced the electric field across the blocking oxide with its dielectric constant and therefore,

electron injection from the gate during erase can be effectively suppressed which will generally in turn enhance the erase speed [54]. From the above discussion it can be concluded that HfO_2 and its aluminates, silicates are now the most accepted candidates. Chengyuan Yan et. al. [55] in 2019 fabricated a nonvolatile memory with a floating gate structure using ZnSe@ZnS core–shell quantum dots as discrete charge-trapping/tunneling centers. The fabricated device demonstrates a large memory window, stable retention, and good endurance. S. Wang et. al. [56] in 2019 fabricated a dual gate structure floating gate non –volatile memory device based on heterostructure of MoS_2 and hexagonal boron nitride. The newly introduced device exhibit long retention time, ultra low leakage current (~10^{-13}A) and low operation voltage (~5V).

Table 3 Work function values of various transition metals

Element	Work function (eV)
Pt	5.35
Au	5.1
Al	4.08
Ag	4.0
Ti	4.35
Cr	4.5
Fe	4.5
Co	5.0
Ni	5.01
Cu	4.65
Mg	3.68
Nb	4.3

Table 4 Comparison of some main properties of high-k dielectric material [53]

Material	Energy Gap (eV)	Conduction Band offset to Si	Dielectric Constant	Crystal Structure
SiO_2	8.9	3.2	3.9	Amorphous
Si_3N_4	5.1	2	7	Amorphous
SiON	5.1-8.9	2-3.2	3.9-7.1	Amorphous
Al_2O_3	8.7	2.8	9	Amorphous
HfO_2	5.7	1.5	25	Monoclinic, Tetragonal, Cubic
ZrO_2	7.8	1.4	25	Monoclinic, Tetragonal, Cubic
TiO_2	3.5	1.2	80	Tetragonal
Ta_2O_5	4.5	1-1.5	26	Orthorhombic
Y_2O_3	5.6	2.3	15	Cubic
La_2O_3	4.3	2.3	30	Hexagonal, Cubic

4. CONCLUSION

To overcome the problem of stored charge leakage back to the channel due to local defects, memory-cell structures employing discrete traps as charge storage nodes have been proposed in the past few years. Extensive researches have been conducted on non volatile memories employing metal nanocrystals/metal floating gate. Metal floating gate in combination with high-k results in good electrical characteristics even at low thicknesses and also lowers the interpoly dielectric leakage (IPD) due to larger work function. The metal nanocrystal with high work function shows enhanced charge retention time as compared to semiconductor nanocrystals and thus the high potentiality of nanocrystals for NVM applications is confirmed. The advantages of both metal NC and a high-tunneling barrier results in excellent data retention characteristic without compromising the programming efficiency and it resolve the tradeoff between programming and retention characteristic. The heterogeneous floating-gate stack of metal nanocrystals and nitride can take the better tradeoff between the programming and retention characteristics as compared to single layer of metal nanocrystals or nitride. The multilayer nanoparticle embedded nonvolatile memory contributes to additional charge storage capability and ultimately enhanced memory window. The high-k blocking oxide play vital role in the low-voltage operation and increases the coupling ratio between the control gate and metal floating gate/ metal NC layer which results in good charge storage feature. However with decrease in nanocrystal size the density of nanocrystals increases but it also faces some limitations such as high leakage density and fluctuation from device to device and isolation concept is violated. Therefore, it is indispensable to solve the scaling problem with suitable requirements in nonvolatile memory industry.

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